I²C/SPI 36-Channel RGB LED Driver

ADVANCED INFORMATION

Description

The AL5887 is comprised of 36 programmable LED current channels each with internal 12-bit PWM for color and brightness control through SPI or I2C digital interface. AL5887 is ideal for up to 12 RGB LED modules lighting applications with 3 programmable banks (A B C) for software control of each color. The global output current of all 36 channels can be set up by an external resistor. Each channel current can digitally be configured up to 70mA under the thermal limitation of the package.

Features of the AL5887 are controlled via programmable SPI/I2C digital interface. Using a dedicated pin INT_SEL, one of the SPI or I2C protocols can be selected. The AL5887 has a 30 kHz, 12-Bit PWM generator for each channel, as well as channel/module independent color mixing and brightness control registers to enable vivid LED effects with zero audible noise. Users can benefit from the device's ultra-low shutdown I_Q Power Saving Mode and easy software programming.

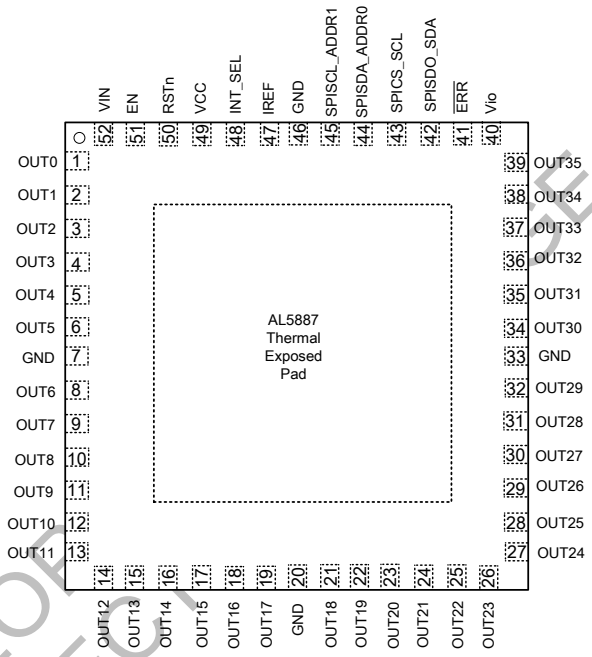
The device operates over –40°C to 85°C ambient temperature range. The AL5887 is available in Wettable W-QFN6060-52(SWP) package.

Features

- Input voltage: 2.7V to 5.5V
- 36 Precision LED Current Sinks
  - OUT pins voltage Max. 5.5V
  - A maximum of up to 70mA per channel current
  - Device to device and channel to channel current accuracy: <2% at 7mA to 70mA, and <3.5% at 1mA to 7mA
  - 12-Bit (4096 steps), 30-kHz PWM Generator integrated for each channel
  - PWM Phase shifting
  - 6-Bit global current dimming
  - Independent Color-Mixing Register Per Channel
  - Independent Brightness Control Register Per RGB Module
  - Optional Logarithmic- or Linear-Scale Brightness Control
  - 3 programmable banks (A, B, C)
- Interface
  - Support 400kHz I2C Interface (Default)
  - 2 External Hardware Address Pins Allow Connecting up to 4 Devices (I2C only)
  - 2MHz SPI compatible Digital Interface (INT_SEL pin = HIGH)
  - Broadcast Slave Address Allows Configuring Multiple Devices Simultaneously
  - Auto-Increment Allows Writing or Reading Consecutive Registers Within One Transmission
- Diagnosis and protection status read through digital interface
  - Open Drain $\overline{ERR}$ pin for Fault Indication
  - Individual LED channel open/short detection
  - Pre-UVLO Warning & Under Voltage Lock-out (UVLO)
  - Pre-OTP Warning & Over Temperature Protection (OTP)
  - Digital POR indicator
  - Individual channel Fault Masking
- Ultralow Quiescent Current:
  - Shutdown Mode: 1μA (Max.) When EN Low >25ms
  - Power Saving Mode: 15μA (Max.) When EN High and All LEDs Off for > 30ms
- Totally Lead-Free & Fully RoHS Compliant (Notes 1& 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact your local Diodes representative.

Pin Assignments

(Top View)



W-QFN6060-52(SWP)

Applications

- RGB LED Lighting
- Architectural Lighting
- Industrial LED Lighting
- Smart Home Appliances
  - Smart Speaker
  - Video Doorbell
  - Electric Smart Lock
  - Smoke Detector
  - Smart Router
  - Set-Top Box
- Wearable &Handheld Devices

Device Information

Part Number	Package	Body-Size
AL5887JAZW52-13	W-QFN6060-52(SWP)	6 mm x 6 mm

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green", and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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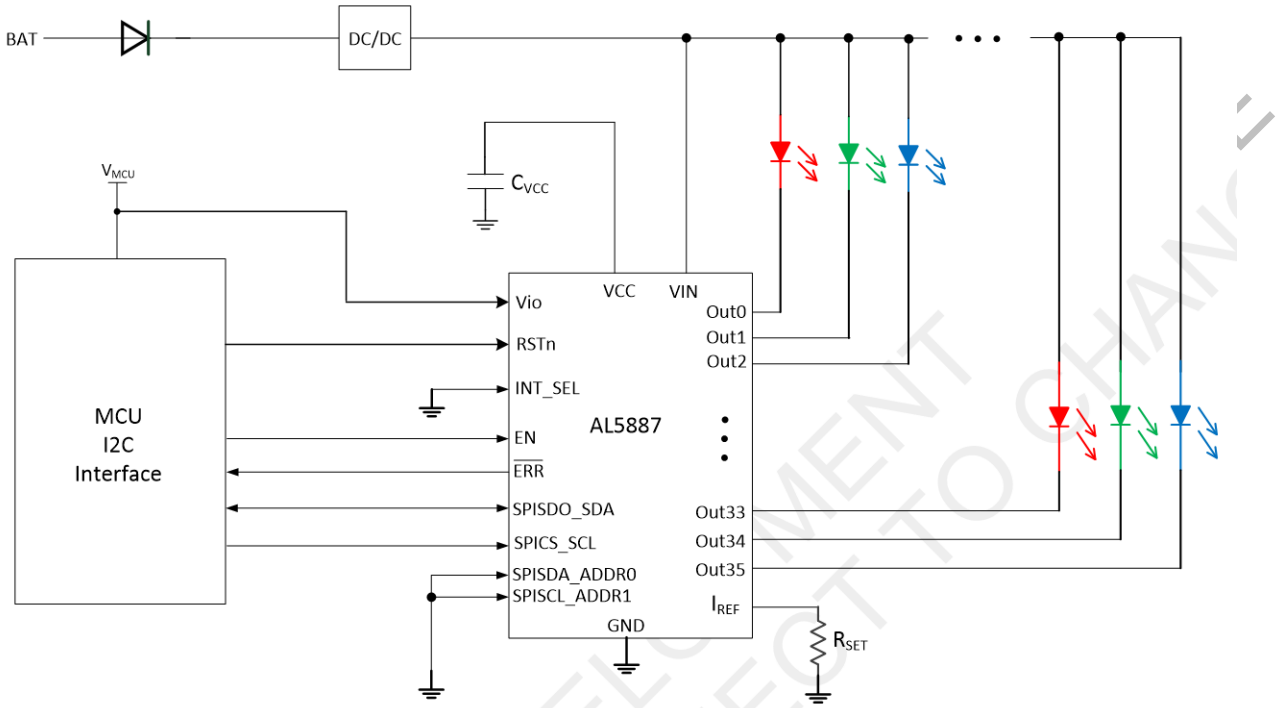
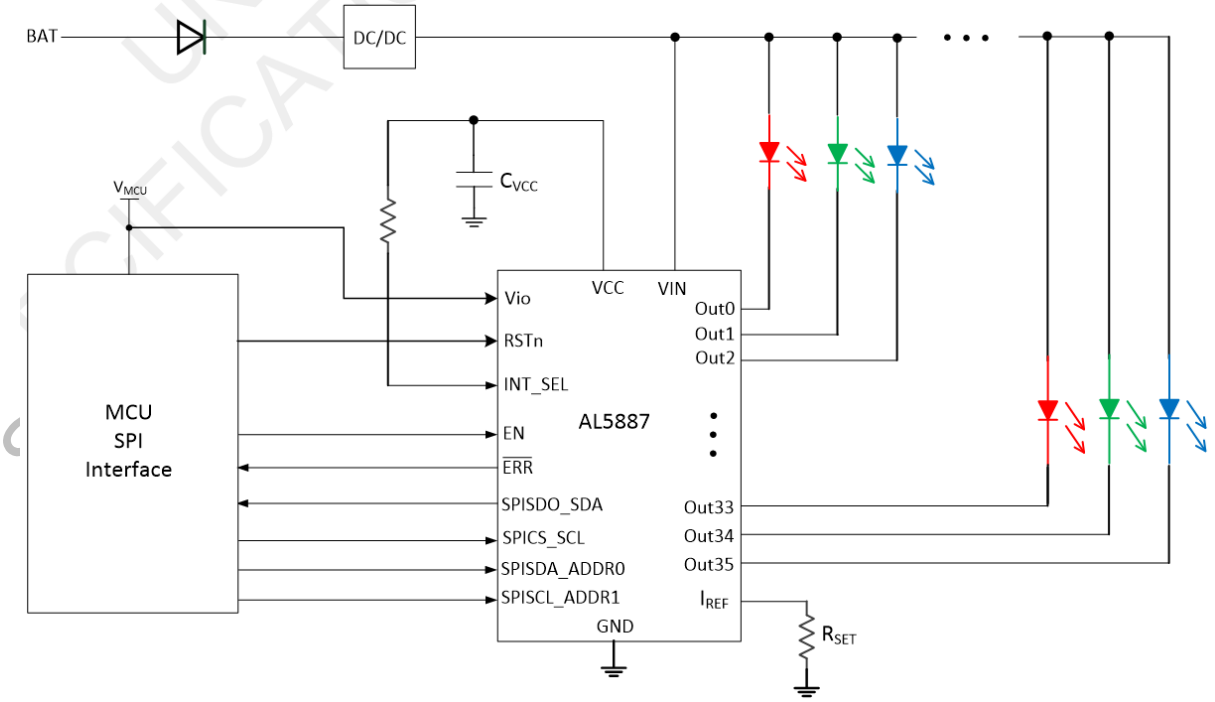
Typical Applications Circuit

1) For I2C Interface



2) For SPI Interface



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Pin Descriptions

Pin Name	W-QFN-52EP	Type	Function
OUT0 ~ OUT5	1 ~ 6	O	Current sink output for LED 0 ~ LED 5
OUT6 ~ OUT17	8 ~ 19	O	Current sink output for LED 6 ~ LED 17
OUT18 ~ OUT29	21 ~ 32	O	Current sink output for LED 18 ~ LED 29
OUT30 ~ OUT35	34 ~39	O	Current sink output for LED 30 ~ LED 35
Vio	40	I	Input power from MCU power rail
$\overline{ERR}$	41	O	Analog output with open drain internal pull up 5MΩ resistor to VLDO for fault indication
SPISDO_SDA	42	I/O	INT_SEL=HIGH, SPI Master input slave output, serial data line INT_SEL=LOW, I2C Data line If not used, this pin must be connected to GND or VIN. (Default = HIGH for I2C)
SPICS_SCL	43	I	INT_SEL=HIGH, SPI Active low chip select. INT_SEL=LOW, I2C bus clock line If not used, this pin must be connected to GND or VIN. (Default = HIGH)
SPISDA_ADDR0	44	I	INT_SEL=HIGH, SPI Master output slave input, serial data line INT_SEL=LOW, I2C slave-address selection pin This pin must not be left floating.(Default = LOW)
SPISCL_ADDR1	45	I	INT_SEL=HIGH, SPI Serial clock line from SPI master(FPGA) INT_SEL=LOW, I2C slave-address selection pin This pin must not be left floating.(Default = LOW)
IREF	47	O	Connect an external resistor to regulate all channel output current.
INT_SEL	48	I	Selects the required communication interface INT_SEL=LOW selects I2C and INT_SEL=HIGH selects SPI (Default = LOW)
VCC	49	O	Internal LDO output pin, this pin must be connected to a 1-μF capacitor to GND.
RSTn	50	I	Resets interface registers only but retains other register values if pulled down for time between 1ms to 20ms. Resets all register values if pulled down for time more than 20ms. Needs to be pulled high for powering up the internal digital block. (Default=HIGH)
EN	51	I	Active low to shut down the chip (Default = LOW)
VIN	52	Power	Power Supply
GND	7, 20, 33, 46	GND	Ground
-	Exposed Thermal Pad	GND	Exposed thermal pad also serves as a ground for the device

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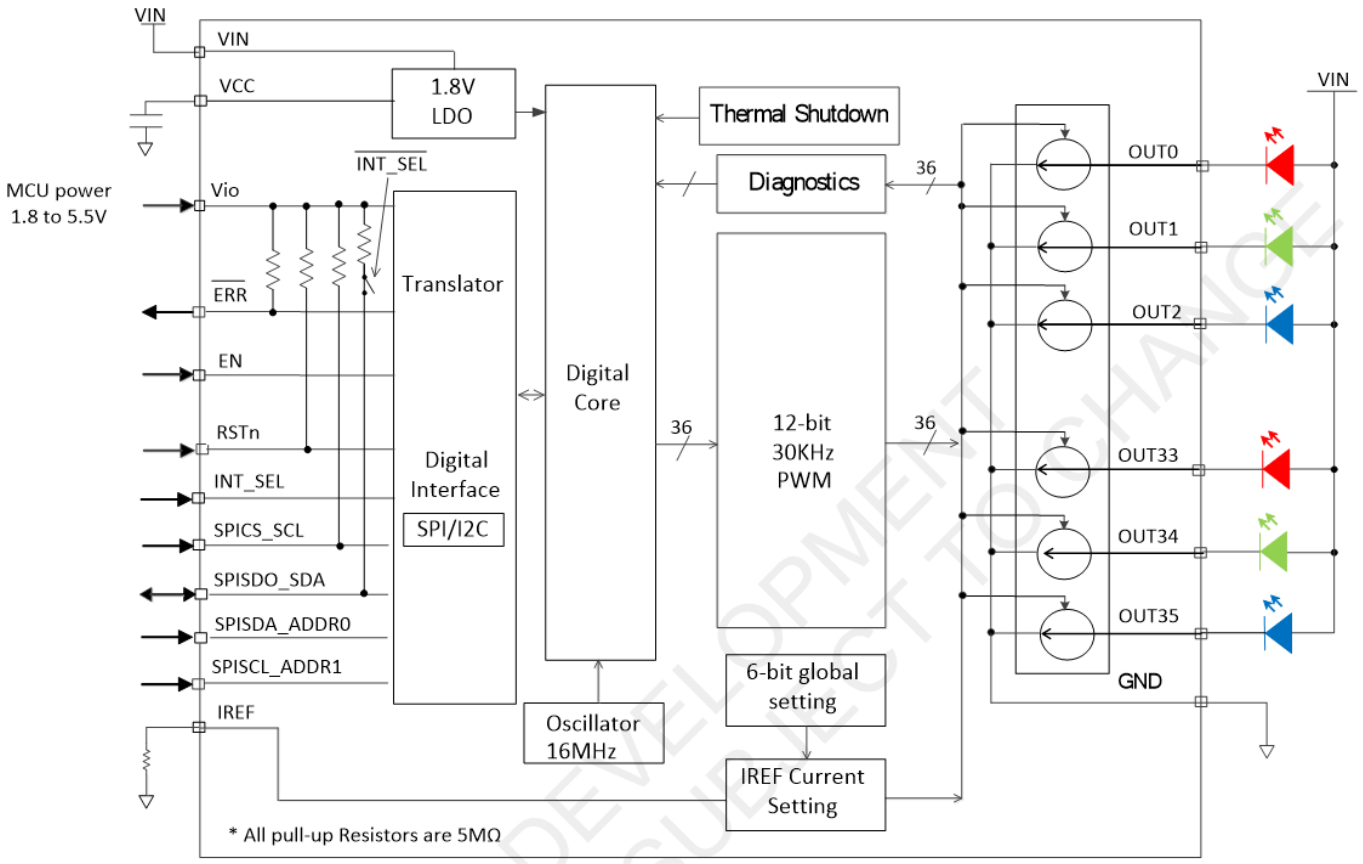
Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage, Voltage Relative to GND	-0.3 to 6	V
I_{OUTx}	OUTx Output Current	160	mA
V_{OUTx}, EN, $\overline{ERR}$, RSTn, Vio, INT_SEL, SPICS_SCL, SPISDO_SDA, SPISDA_ADDR0, SPISCL_ADDR1, IREF	High-voltage pins	-0.3 to 6V	V
VCC	Low-voltage pins	-0.3 to 2V	V
T_J	Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
ESD	HBM	3000	V
	CDM	1000	V

Note: 4.Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Package Thermal Data (Note 5)

Package	θ_{JC} Thermal Resistance Junction-to-Case (°C/W)	θ_{JA} Thermal Resistance Junction-to-Ambient (°C/W)	P_{DIS} T_A = +25°C, T_J = +105°C
W-QFN6060-52(SWP)	4.13	19.45	4.12W

Notes: 5. Test condition: Device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heat-sink is needed
6. Stresses greater than the Absolute Maximum Ratings specified above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

SYMBOL	Parameter	MIN	NOM	MAX	UNIT
VIN	Device supply voltage	2.7		5.5	V
Vio	Input power from MCU rail	1.8	3.3	5.5	V
I_{OUTx}	OUTx Output Current (Note 7)		39	70	mA
$I_{(VCC)}$	LDO external current load			10	mA
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

Note: 7. Consider package thermal limitation and PCB layout

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Electrical Characteristics (V_{IN}=3.3V, -40°C <T_A<85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{IN}	Supply Voltage		2.7	3.3	5.5	V
VCC	Internal 1.8V LDO output	Iload = 10mA	1.76	1.8	1.84	V
I_{VIN}	Shut down supply current	V_{EN}= 0V	0.05	0.2	5	μA
	Standby supply current	V_{EN}= 3.3V, Chip_EN=0 (bit)	7	12	25	μA
	Normal-mode supply current	With 39mA LED current per OUTx	5	7	9	mA
	Power-save mode supply current	V_{EN}= 3.3V, Chip_EN=1 (bit), Power_Save_EN = 1 (Bit), All LEDs turned off for time > 30ms	7	12	25	μA
Pre UVLO+	VIN pre-UVLO rising			2.32		V
Pre UVLO-	VIN pre-UVLO falling			2.21		V
Pre UVLO Hys				0.11		V
UVLO+	VIN UVLO rising		2	2.36	2.5	V
UVLO-	VIN UVLO falling		2	2.16	2.5	V
UVLO_Hys				0.2		V
V_{IREF}	Output Voltage of IREF pin		0.696	0.7	0.704	V
CURRENT SINK (Note 8)						
I_{MAX}	Maximum Global Output Current (Channel average current, Color Register=FF, Brightness Register=FF)	V_{IN} in full range, R_{SET} = 2.1kΩ, *Max_Current_Option=0, #G5:G0=000000			29.25	mA
		V_{IN} in full range, R_{SET} = 2.1kΩ, *Max_Current_Option=1, #G5:G0=100000			7	mA
		V_{IN} in full range, R_{SET} = 2.1kΩ, *Max_Current_Option=1 #G5:G0=000000			39	mA
		V_{IN} in full range, R_{SET} = 2.1kΩ, *Max_Current_Option=1 #G5:G0=011111			70	mA
I_{LIM}	Internal Current Limit	V_{IN}=3.3V,*Max_Current_Option=1, V_{IREF}=0V #G5:G0=011111			136	mA
I_{D2D} (Note 9)	Device to device (Iavg-Iset)/Iset*100	V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=2.1kΩ, All Channel currents set to PWM=100%, #G5:G0=000000 (I_{MAX}=39mA)			±2	%
		V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=14.7kΩ, All Channel currents set to PWM=100%, #G5:G0=000000 (I_{MAX}=5.57mA)			±3.5	%
		V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=36.5kΩ, All Channel currents set to PWM=50%, #G5:G0=000000 (I_{MAX}=1.12mA)			±5.5	%
I_{C2C} (Note 10)	Channel to channel (IOUTx-Iavg)/Iavg*100	V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=2.1kΩ, All Channel currents set to PWM=100%, #G5:G0=000000(I_{MAX}=39mA)			±1.5	%
		V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=14.7kΩ, All Channel currents set to PWM=100%, #G5:G0=000000(I_{MAX}=5.57mA)			±3	%
		V_{IN} = 2.7V, 3.3 V, 5.5V, R_{SET}=36.5kΩ, All Channel currents set to PWM=50%, #G5:G0=000000(I_{MAX}=1.12mA)			±5	%
I_{lkg}	LEDx leakage current	PWM=0%		0.01	0.04	μA

* DEVICE CONFIG1 Register

LED_GLOBAL_DIMMING Register

Note: 8. For understanding of PWM generation process, please refer to the Application Note.

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Electrical Characteristics (V_{IN}=3.3V, -40°C <T_A<85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT SINK (cont'd)						
V_{SAT}	Output saturation voltage	V_{IN} in full range, *Max_Current_Option =0 (bit), R_{SET}=2.1kΩ, PWM=100%, the voltage when the LED current has dropped 5%, #G5:G0=000000		0.15	0.25	V
		V_{IN} in full range, *Max_Current_Option =1 (bit), R_{SET}=2.1kΩ, PWM=100%, the voltage when the LED current has dropped 5%, #G5:G0=000000		0.2	0.3	V
$V_{OPEN\_th\_rising}$	LED open threshold	V_{IN}=3.3V, V_{OUTx} < $V_{OPEN\_th\_rising}$	0.12	0.2	0.34	V
$V_{SC\_th\_rising}$	LED short threshold (V_{IN} - V_{OUTx})	V_{IN}=3.3V, V_{IN} - V_{OUTx} < $V_{SC\_th\_rising}$	0.31	0.62	0.78	V
PWM Group Dimming						
PWM_{FREQ}	PWM Frequency		26	30	35	kHz
Fosc	Internal oscillator frequency		13.5	15.5	17.5	MHz
PWM_{on_min}	PWM on time minimum **			65.1		ns
IOUTx_trise	IOUTx rise time **	Time for 0% to 90% rise of IOUTx		8		ns
Digital Input Logic Levels (EN, RSTn, INT_SEL)						
V_{IL}	Input Logic Low	Vio = 1.8V			0.4	V
V_{IH}	Input Logic High		1.4			V
Internal Pull-up Resistor at $\overline{ERR}$ pin						
$R_{pull-up}$	Internal Pull-up Resistor between $\overline{ERR}$ pin to Vio			5		MΩ
Digital Interface Logic Levels(SPISCL,SPISDA,SPICS,SPISDO, SPISDA_ADDR0, SPISCL_ADDR1)						
V_{IL}	Input Logic Low	Vio = 1.8V			0.4	V
V_{IH}	Input Logic High		1.4			V
V_{SDA}	SDA output low level	I_{PULLUP} = 5 mA			0.4	V
Protection						
$T_{(PRETSD)}$	Pre-thermal warning threshold			145		°C
$T_{(PRETSD\_HYS)}$	Pre-thermal warning hysteresis			20		°C
TSD	Thermal shutdown temperature			160		°C
T_{hys}	Thermal shutdown temperature hysteresis			20		°C

* DEVICE CONFIG1 Register
# LED_GLOBAL_DIMMING Register

** Guaranteed by Design

Notes: 9. ID2D: Accuracy of average of all 36 channels current with respect to design target.
10. IC2C: Accuracy of individual channel current with respect to average of all 36 channels current within a device. Channel current: Average, or mean, current (not RMS current) on a channel.

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Electrical Characteristics (V_{IN}=3.3V, -40°C <T_A<85°C, unless otherwise specified.)

TIMING Requirements for I2C interface:

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I2C Clock Frequency			400	KHz
t_{EN_H}	EN first rising edge until first I2C access			500	us
t_{EN_L}	EN first falling edge until first I2C reset			3	us
1	Hold time(repeated) START condition	0.6			us
2	Clock low time	1.3			us
3	Clock high time	600			ns
4	Setup time for a repeated START condition	1.3			us
5	Data hold time	600			ns
6	Data setup time	600			ns
7	Rise time of SDA and SCL	20 + 0.1 Cb			ns
8	Fall time of SDA and SCL	15 + 0.1 Cb			ns
9	Setup time for STOP condition	0			ns
10	Bus free time between a STOP and a START condition	100			ns
Cb	Capacitive load parameter for each bus line. Load of 1 pF corresponds to one nanosecond	10		200	pF

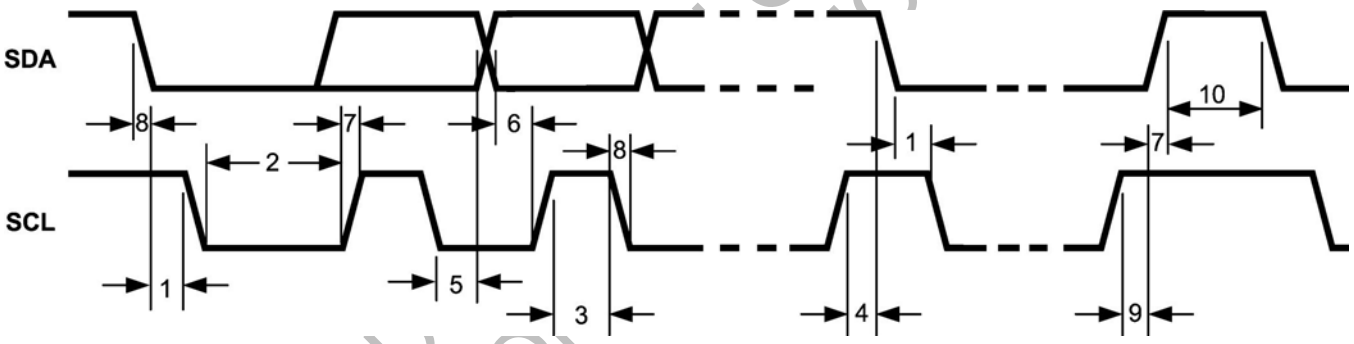

Figure 1. I²C Timing Parameters

ADVANCED INFORMATION

Electrical Characteristics (V_{IN}=3.3V, -40°C <T_A<85°C, unless otherwise specified.)

TIMING Requirements for SPI interface:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCLK}	SPI Clock Frequency				20	MHz
t_{CSS}	The time from SPICS_SCL low to SPISCL_ADDR1 high		25			ns
t_{CSH}	The time from SPISCL_ADDR1 low to SPICS_SCL high		50			ns
t_{DS}	Data set-up time		10			ns
t_{DH}	Data hold time		0			ns
t_{CS_HI}	Minimum chip select de-asserted HIGH time		25			ns
$td_{(SDO)}$	SDO delay time	CL=50pF			20	ns
t_{LOW}	LOW period of SCLK clock		25			ns
t_{HIGH}	HIGH period of SCLK clock		25			ns

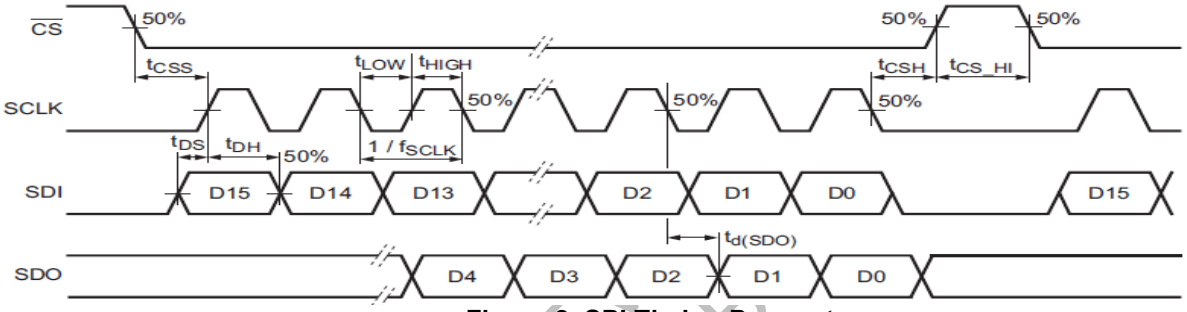

Figure 2. SPI Timing Parameters

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Functional Descriptions

1. General Operation

Either the I2C or SPI protocol can be selected using INT_SEL pin.

Using I2C/ SPI interface, AL5887 controls LED's color and brightness through 4 primary mechanisms:

1. Use Rset to set full range for LED current I_{MAX} (up to 70mA).
2. Set I_{MAX} by using 6-bit global dimming register, which is termed as LED GLOBAL DIMMING in the registers map.
3. Set color/brightness registers for LED color and brightness (see Registers Map Description).
4. Further select various dimming and protection features described in Registers Map Description.

2. Feature Description

2.1 Each Channel PWM Control

The AL5887 device is designed with independent color mixing and brightness control, which makes the RGB LED effects fancy and the control experience straightforward. With the inputs of the color-mixing register and the brightness-control register, the final PWM generator output for each channel is 12-bit resolution and 30-kHz dimming frequency, which helps achieve a smooth dimming effect and eliminates audible noise. See Figure 3.

For example, yellow color has the red, green and blue components as 255,255 and 0 respectively. So to get the color yellow for the first RGB LED module, the color registers at the addresses 14h, 15h and 16h need to be configured with the values 255, 255 and 0 respectively. The brightness register for the first RGB LED module at the address 8h can be configured based on the amount of brightness needed, 255 being the maximum brightness.

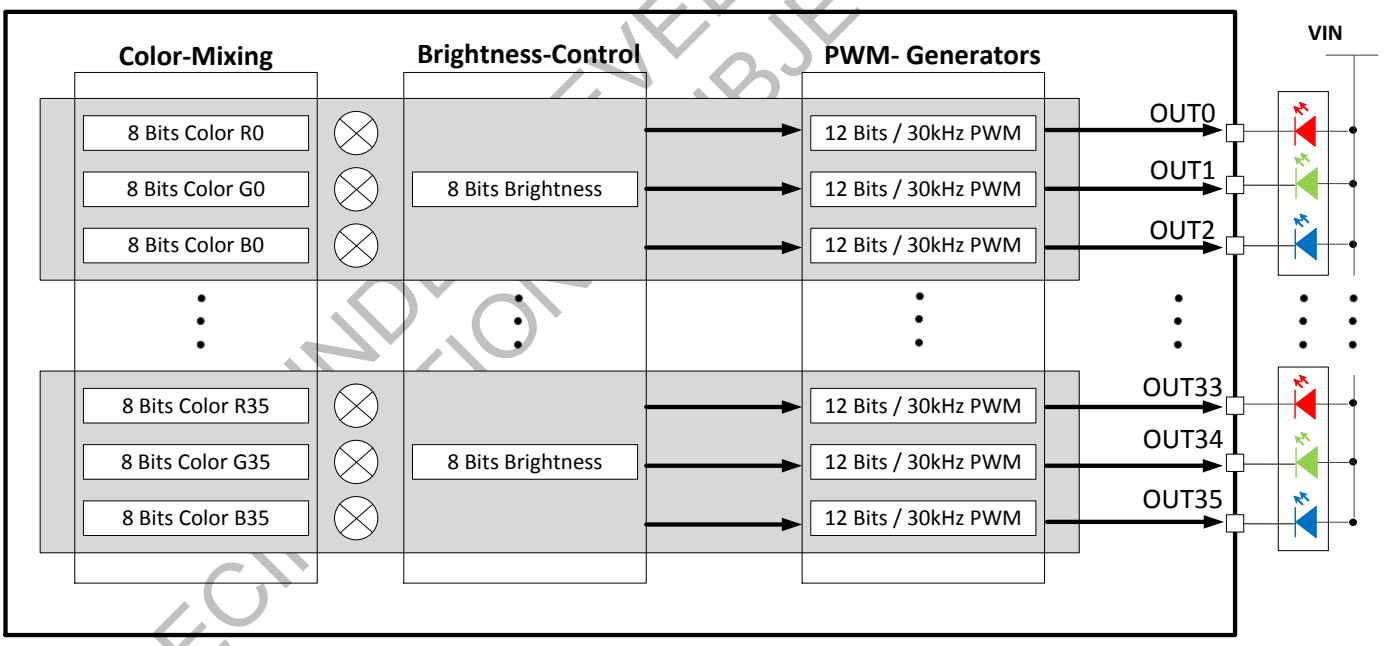

Figure 3. PWM Control Scheme for Each Channel

Functional Description (Cont'd)

2.1.1 Independent Color Mixing Per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUTx_COLOR). The device allows every RGB LED module to achieve >16 million (256 × 256 × 256) color-mixing.

2.1.2 Independent Brightness Control per RGB LED Module

When color is fixed, the independent brightness-control is used to achieve accurate and flexible dimming control for every RGB LED module.

2.1.2.1 Brightness-Control Register Configuration

Every three consecutive output channels are assigned to their respective brightness-control register (RGBx_BRIGHTNESS). For example, LED0, LED1, and LED2 are assigned to RGB0_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in Table 1. The AL5887 device allows 256-step brightness control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the RGB0_BRIGHTNESS register results in 100% dimming brightness. With this setting, the users can just configure the color mixing register by channel to achieve the target dimming effect in a single-color LED application.

2.1.2.2 Logarithmic- or Linear-Scale Brightness Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. However, for RGB LEDs, if using a single register to achieve both color mixing and brightness control, color distortion can be observed easily when using a logarithmic scale. The AL5887 device, with independent color-mixing and brightness-control registers, implements the logarithmic scale dimming control inside the brightness control function, which solves the color distortion issue effectively (See Figure 4). Also, the AL5887 device allows users to configure the dimming scale either logarithmically or linearly through the global Log_Scale_EN register bit. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach. See Figure 5.

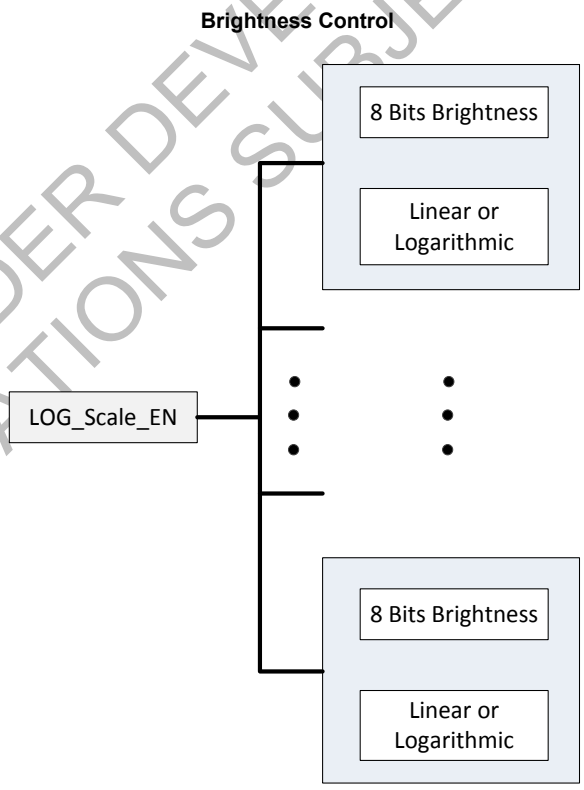

Figure 4. Logarithmic or Linear Scale Brightness Control

Functional Description (Cont'd)

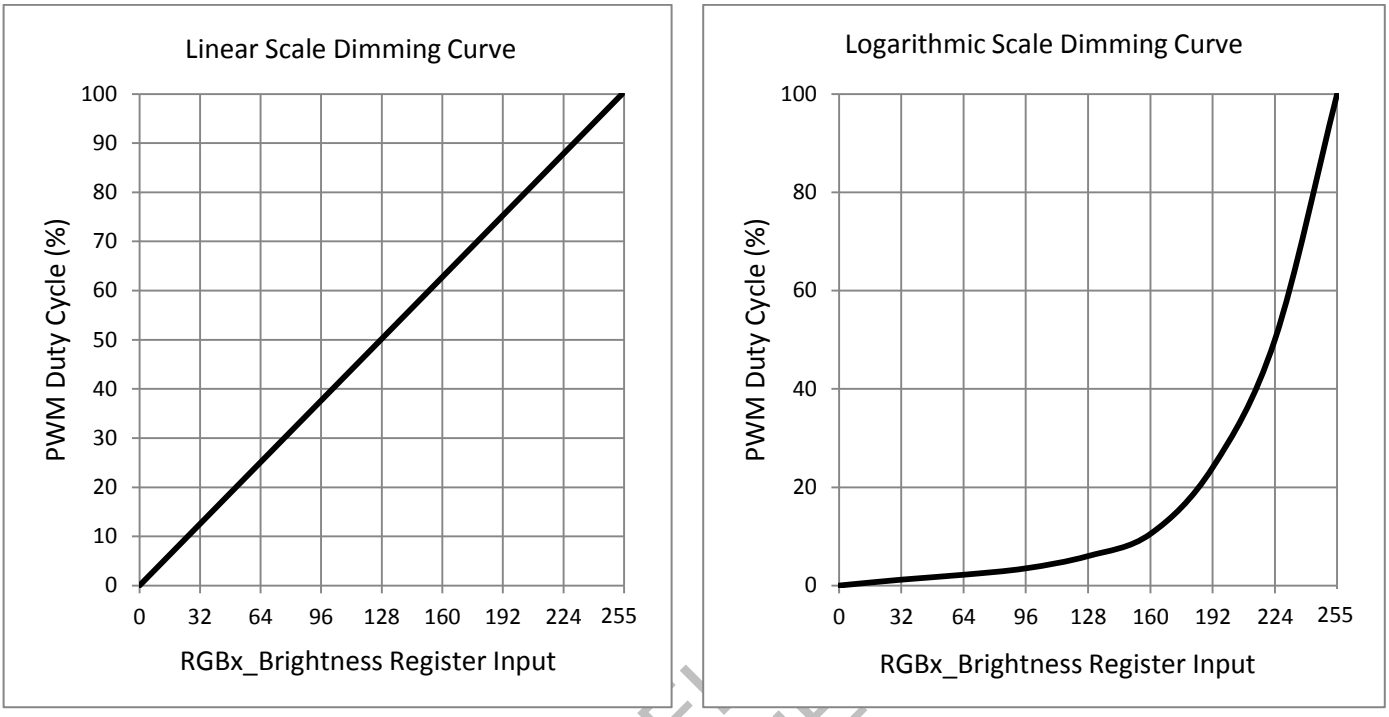

Figure 5. Logarithmic vs Linear Dimming Curve

2.1.3 12-Bit, 30-kHz PWM Generator per Channel

With the inputs of the color mixing and the brightness control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related brightness-control register value. The final output PWM duty cycle has 12 bits of control resolution, which is achieved by a 9 bits of pure PWM resolution and 3 bits of dithering digital control. For 3-bit dithering, every eighth pulse is made 1 LSB longer to increase the average value by 1 / 8th. The AL5887 device allows the users to enable or disable the dithering function through the PWM_Dithering_EN register. When enabled (default), the output PWM duty-cycle resolution is 12 bits. When disabled, the output PWM duty-cycle resolution is 9 bits. More details about dithering is mentioned in the following paragraph.

When 3-bit dithering is enabled, dither effect is generated with 8 (2^3=8) possible dither values: "0", "1", "2",…"7". "0" means no dithering; "1" means every 8th PWM pulse is made 1 LSB longer to increase the final average duty cycle by 1 LSB/8 (duty cycle is termed as DT); "2" means that in every group of 8 PWM pulses, the 7th and 8th PWM pulses are both made 1 LSB longer to increase DT by 2 LSB/8; etc. AL5887 uses 512 clocks in a 100% PWM DT period to achieve 9-bit pure PWM resolution (2^9=512), thus 1 LSB PWM DT is 1/512. Therefore dither value "1" adds 1/(8*512)=0.0244% additional DT to pure PWM DT. For example, combining with dither value "1", the pure PWM DT of 25% will actually generate DT=25.0244% for LED current regulation; while with dither value "2", pure PWM DT of 25% will actually generate DT=25.05%. Though AL5887 pure PWM resolution is 1/512=0.195%, the 3-bit dither scheme enhances PWM resolution to 0.0244%.

2.1.4 PWM Phase-Shifting

A PWM phase-shifting scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases.

- Phase 1- The rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, …, LED[3 × (n – 1)].
- Phase 2- The middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, …, LED[3 × (n – 1) + 1].
- Phase 3 - The falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, …, LED[3 × (n – 1) + 2].

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Functional Description (Cont'd)

2.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily; the AL5887 device provides an easy coding approach, the LED bank control. Each channel can be configured as either independent control or bank control through the LEDx_Bank_EN register. When LEDx_Bank_EN = 0 (default), the LED is controlled independently by the related color-mixing and brightness-control registers. When LEDx_Bank_EN = 1, the AL5887 device drives the LED in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM scheme of each channel. When a channel configured as LED bank-control mode, the related color mixing and brightness control is governed by the bank control registers (BANK_A_COLOR, BANK_B_COLOR, BANK_C_COLOR, and BANK_BRIGHTNESS) regardless of the inputs on its own color-mixing and brightness-control registers.

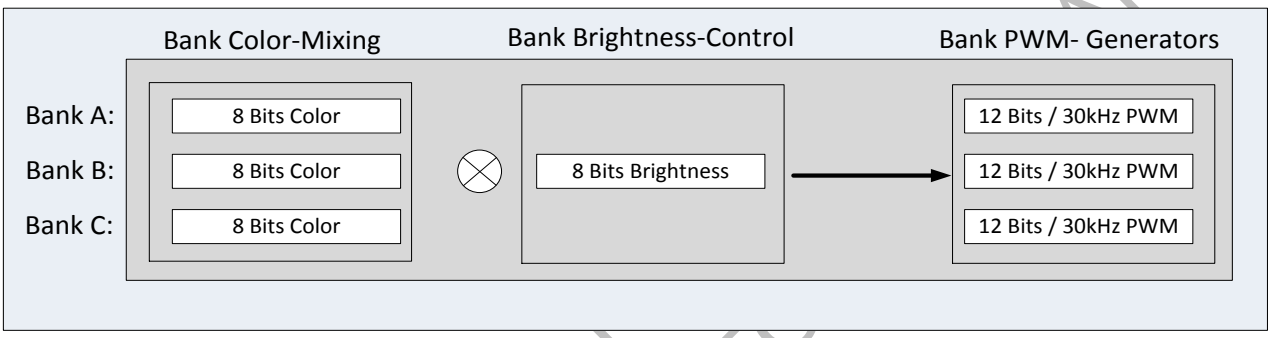

Figure 7. Bank PWM Control Scheme

Table 1. Bank Number and RGB Number Assignment

OUT NUMBER	BANK NUMBER	RGB MODULE NUMBER	OUT NUMBER	BANK NUMBER	RGB MODULE NUMBER
OUT0	Bank A	RGB0	OUT18	Bank A	RGB6
OUT1	Bank B		OUT19	Bank B	
OUT2	Bank C		OUT20	Bank C	
OUT3	Bank A	RGB1	OUT21	Bank A	RGB7
OUT4	Bank B		OUT22	Bank B	
OUT5	Bank C		OUT23	Bank C	
OUT6	Bank A	RGB2	OUT24	Bank A	RGB8
OUT7	Bank B		OUT25	Bank B	
OUT8	Bank C		OUT26	Bank C	
OUT9	Bank A	RGB3	OUT27	Bank A	RGB9
OUT10	Bank B		OUT28	Bank B	
OUT11	Bank C		OUT29	Bank C	
OUT12	Bank A	RGB4	OUT30	Bank A	RGB10
OUT13	Bank B		OUT31	Bank B	
OUT14	Bank C		OUT32	Bank C	
OUT15	Bank A	RGB5	OUT33	Bank A	RGB11
OUT16	Bank B		OUT34	Bank B	
OUT17	Bank C		OUT35	Bank C	

With the bank control configuration, the AL5887 device enables users to achieve smooth and live LED effects globally with an ultra-simple software effort.

For an example (as shown in Figure 8), say if we want to configure RGB0 in independent mode and rest of RGB1 to RGB11 in BANK mode, we can do that by configuring LED_CONFIG0 register to FEh and LED_CONFIG1 register to 0Fh. By doing this, the RGB0 module operating in independent mode will be using RGB0_BRIGHTNESS for brightness and R0_COLOR, G0_COLOR and B0_COLOR for R, G and B colors respectively. While the other RGB modules in bank mode would use BANK_BRIGHTNESS for brightness and BANK A, BANK B and BANKC for R, G and B colors respectively.

Functional Description (Cont'd)

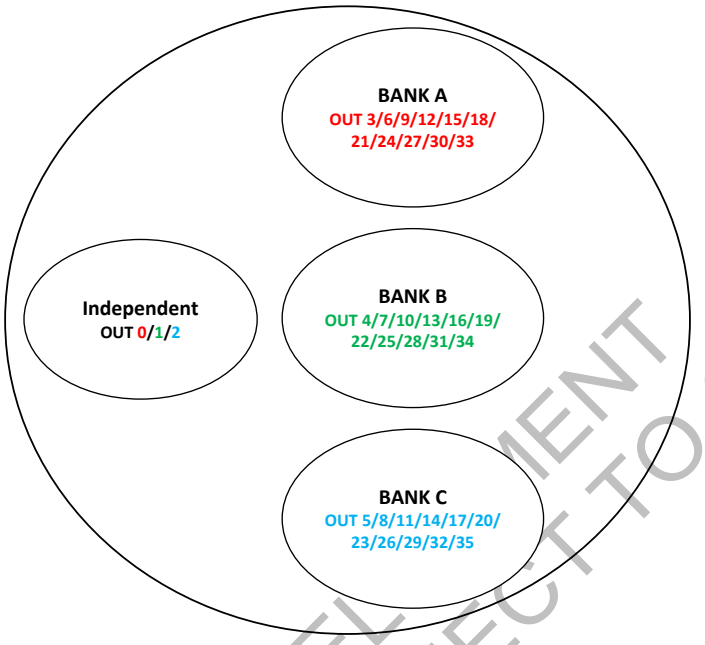

Figure 8. Bank PWM Control Example

2.3 Automatic Power-Save Mode

When all the LED outputs are inactive, the AL5887 device is able to enter power-save mode automatically, thus lowering idle-current consumption down to 15μA (maximum). Automatic power-save mode is enabled when register bit Power_Save_EN = 1 (default) and all the LEDs are off (both color and brightness registers = 00H) for a duration of >30 ms. Almost all analog blocks are powered down in power-save mode. If any I²C/SPI command to the device occurs, the AL5887 device returns to NORMAL mode.

2.4 Protection Features

2.4.1 LED Open-Circuit Diagnostics

The AL5887 integrates LED open-circuit diagnostics to allow users to monitor LED status real time. The device monitors OUTx voltage to determine if there is any open-circuit failure.
If the voltage V_{OUTx} for any of the channels goes below threshold $V_{OPEN\_th\_rising}$ and if the open persists for more than t_{FAULT_WAIT}, the AL5887 pulls the $\overline{ERR}$ pin down to report fault and also sets flag register Open_Fault_CHx and FLAG_OPEN to 1. Once the open-circuit failure is removed, the controller needs to send CLR_FAULT to clear the FLAG_OPEN after fault removal. The fault delay is decided based on below table.

When the PWM duty cycle is smaller than 3%, the LED open-circuit diagnostics will be disabled.

Table 1b. FAULT WAIT TIME

FW1	FW0	t_{FAULT_WAIT}
0	0	8 PWM clock count
0	1	16 PWM clock count
1	0	24 PWM clock count
1	1	32 PWM clock count

Functional Description (Cont'd)

2.4.2 LED Short-circuit Diagnostics

AL5887 monitors voltage difference between SUPPLY (VIN) and OUTx to determine if there is any short-circuit failure. If the difference voltage (V_{IN} - V_{OUTx}) for any of the channel falls below threshold ($V_{SC\_th\_rising}$) and if the short persists for more than t_{FAULT_WAIT}, the AL5887 pulls the $\overline{ERR}$ pin low to report fault and also sets flag register Short_Fault_CHx and FLAG_SHORT to 1. Once the short-circuit failure is removed, the controller needs to send CLR_FAULT to clear the FLAG_SHORT after fault removal.

When the PWM duty cycle is smaller than 3%, the LED short-circuit diagnostics will be disabled.

2.4.3 Pre-OTP Warning &Thermal Shutdown

The AL5887 has pre-thermal warning threshold of 145°C (typical) and thermal shutdown threshold of 160°C (typical)

When the AL5887 junction temperature rises above pre-thermal warning threshold of 145°C (typical) and if it persists for more than 33us, the device reports pre-thermal warning by pulling $\overline{ERR}$ pin low, and sets the flag register FLAG_PREOTP to 1.The device releases pre-OTP warning once the temperature goes below 125°C. Once the fault is removed, the controller needs to send CLR_FAULT to clear the flag register after fault removal.

The AL5887 device also implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature further rises to 160°C (typical), the device shuts down all output drivers and pulls the $\overline{ERR}$ pin low. The AL5887 device releases thermal shutdown when the junction temperature of the device is reduced to 140°C (typical).

2.4.4 Pre-UVLO Warning

The AL5887 provides Pre-UVLO feature that warns the MCU about supply (VIN) being low and soon UVLO might be triggered.
When VIN goes below Pre-UVLO- threshold and if it persists for more than 33us, $\overline{ERR}$ pin is pulled low and the flag register FLAG_PREUVLO is set to 1.The device releases pre-UVLO warning once the VIN goes above Pre-UVLO+ threshold. Once the fault is cleared, the controller needs to send CLR_FAULT to clear the flag register after fault removal.

2.4.5 UVLO

The AL5887 device has an internal comparator that monitors the voltage at VIN. When VIN is below UVLO-, reset is active and the AL5887 device is in the INITIALIZATION state. When VIN supply goes below the UVLO- threshold, $\overline{ERR}$ pin is pulled low to indicate the fault.

2.4.6 Digital POR Indicator

The AL5887 device has a digital bit FLAG_POR to indicate the power on reset. The default value of this bit is high to indicate the power reset of digital block. The controller can set CLR_POR during the start of the operation to reset FLAG_POR so that the next power reset to digital block can be captured.

Functional Description (Cont'd)

2.4.7 Fault Masking

Open_Mask_CHx prevents the output open-circuit fault of individual channels from being reported to $\overline{ERR}$ pin while Open_Mask prevents any of the channels open fault being reported to $\overline{ERR}$ pin.

Short_Mask_CHx prevents the output open-circuit fault of individual channels from being reported to $\overline{ERR}$ pin while Short_Mask prevents any of the channels open fault being reported to $\overline{ERR}$ pin.

Pre_OTP_Mask prevents the Pre_OTP fault from being reported to $\overline{ERR}$ pin.

Pre_UVLO_Mask prevents the Pre_UVLO fault from being reported to $\overline{ERR}$ pin.

POR_Mask prevents the POR event from being reported to $\overline{ERR}$ pin.

2.4.8 $\overline{ERR}$ Output

The $\overline{ERR}$ pin is a fault indicator pin. It can be used as an interrupt output to master controller in case of any fault. The $\overline{ERR}$ pin is an NMOS open drain output with an internal 5MΩ pull-up resistor, pulled to Vio and if additionally, this pin can also be pulled up externally to MCU supply using a smaller resistor like 10kΩ, as shown in figure below. When one or any of the faults is triggered such as UVLO, OTP, pre-UVLO, pre-OTP, channel open, channel short is detected, $\overline{ERR}$ pin is pulled low continuously. Once the $\overline{ERR}$ pin output is triggered, the controller needs to take necessary action and to deal with the fault and reset the fault flag. AL5887 takes action only for UVLO and OTP faults. For any other fault, AL5887 only reports the fault and controller needs to take the action.

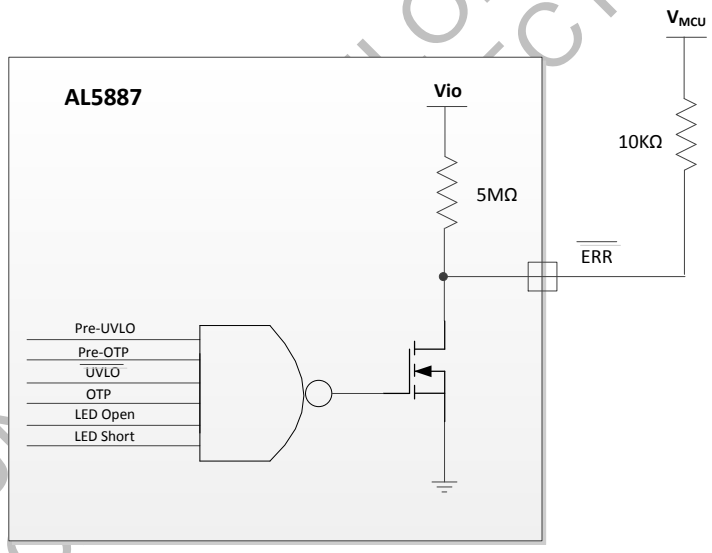

Figure 9. $\overline{ERR}$ Internal Block Diagram

Functional Description (Cont'd)

2.5 Interface Selection

Interface selection between SPI and I2C is done using an external pin INT_SEL. When tied low, I2C is selected while when connected to high, SPI is selected.

2.6 Digital Communication Enhancements

Pulling the external pin RSTn high enables the internal digital block. Pulling down for time duration between 1ms to 20ms resets only the interface related register value and would keep other register values unaltered. If pulled down for time duration more than 20ms would reset all the registers. There is an internal pull up resistor that would by default pull up this pin to HIGH.

2.7 Current Setting for all channels

The maximum global output current for all 36 channels can be adjusted by the external resistor, R_{SET}, as described below.

$I_{MAX} = K_{IREF} * V_{IREF} / R_{SET} * [(Max\_Current\_Option/4)+(3/4)]$ ……..(1)

where ,

I_{MAX} = Channel average current, Color Register=FF, Brightness Register=FF

V_{REF}= 0.7 V

R_{SET} = External dimming resistor (2.1kΩ recommended)

Max_Current_Option = 1 (default)

K_{IREF} = 21 + (N* 3), is the current multiplication factor which can be programmed using 6-bit global dimming register G5:G0 (Address = 66H), which is analog dimming register and N is the decimal equivalent of G5 G4 G3 G2 G1 G0.

For example, if all global dimming register bits are 0, the N will be decimal equivalent of 100000 which is 32. Hence, K_{IREF} = 21 + (32 * 3) = 117

Using equation (1) above, for R_{SET} = 2.1kΩ and Max_Current_Option = 1, below is the table that shows I_{MAX} variation with respect to the global dimming register bits. From table 1c, we can see that the default value = 39mA, minimum value = 7mA and maximum value = 70mA.

Table 1c. I_{MAX} v/s Global Dimming @ R_{SET} = 2.1kΩ

G5	G4	G3	G2	G1	G0	I_{MAX}(mA)	K_{IREF}
0	0	0	0	0	0	39 (Default)	117 (Default)
0	0	0	0	0	1	40	120
0	0	0	0	1	0	41	123
0	0	0	0	1	1	42	126
‘	‘	‘	‘	‘	‘	‘	‘
‘	‘	‘	‘	‘	‘	‘	‘
0	1	1	1	0	0	67	201
0	1	1	1	0	1	68	204
0	1	1	1	1	0	69	207
0	1	1	1	1	1	70 (max)	210 (max)
1	0	0	0	0	0	7 (min)	21 (min)
1	0	0	0	0	1	8	24
1	0	0	0	1	0	9	27
1	0	0	0	1	1	10	30
‘	‘	‘	‘	‘	‘	‘	‘
‘	‘	‘	‘	‘	‘	‘	‘
1	1	1	1	0	1	36	108
1	1	1	1	1	0	37	111
1	1	1	1	1	1	38	114

Functional Description (Cont'd)

Similarly, using equation (1) above, for global dimming register setting of 000000H and Max_Current_Option = 1, below is the table that shows I_{MAX} variation with respect to the R_{SET}.

Table 1d. I_{MAX} v/s R_{SET} @ G5:G0 = 000000

R_{SET}(kΩ)	I_{MAX}(mA)	K_{IREF}
2.1 (Recommended)	39	117
14.7	5.57	117
36.5	2.24	117

Table 1e shows IMAX range using global dimming at different R_{SET} values

Table 1e. I_{MAX} v/s global dimming bits @ various R_{SET}

R_{SET}(kΩ)	I_{MAX}(mA)		
	MIN	Default	MAX
2.1 (Recommended)	7	39	70
14.7	1	5.57	10
36.5	0.4	2.24	4

2.7.1 Thermal Considerations

As Vinmax increases to 5.5V, the voltage on OUTx nodes can go as high as 3V for RED leds and 2V for GREEN and BLUE leds. In such situation if the user configures G0:G5 or Rext for higher currents, the device would get over heated and might hit the thermal shutdown voltage.

Hence the Vin and IOUTx for the channels should be chosen in such a way that the device junction temperature does not exceed its thermal shutdown temperature. Below is the formula relating the power dissipation and θ_{JA} that can be used to avoid device thermal shutdown.

$$T_J = T_A + (\theta_{JA} * P_{TOTAL})$$

Where,
T_J is the junction temperature
T_A is the ambient temperature
θ_{JA} is the junction to ambient thermal resistance
P_{TOTAL} is the device's total power dissipation

Example: If all the 36 channels are turned on and carry same current Imax, then the device total power dissipation is given by,

$$P_{TOTAL} = (12 * V(OUT0) * Imax) + (12 * V(OUT1) * Imax) + (12 * V(OUT2) * Imax)$$

2.8 MCU Supply

AL5887 can recognize interface logic levels from 1.8V to 5.5V. So MCU interacting with AL5887 can operate in the range 1.8V to 5.5V. However, the information of the supply used by MCU is required to be shared with AL5887 by connecting the MCU supply to Vio pin of AL5887.

Functional Description (Cont'd)

2.9 Device Functional Modes

- **INITIALIZATION**: The device enters into INITIALIZATION mode when EN = H. In this mode, all the registers are reset. Entry can also be from any state, if the RESET (register) = FFh or UVLO is active.
- **NORMAL**: The device enters the NORMAL mode when Chip_EN (register) = 1. I_{CC}is5 mA (typical).
- **POWER SAVE**: The device automatically enters the POWER SAVE mode when Power_Save_EN (register) =1 and all the LEDs are off for a duration of >30 ms. In POWER SAVE mode, analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I²C/SPI. I_{CC} is 15 µA (maximum). In case of any I²C/SPI command to this device, it goes back to the NORMAL mode.
- **SHUTDOWN**: The device enters into SHUTDOWN mode from all states on VIN power down or when EN = Low >25ms .I_{CC} is < 1 µA (max).
- **STANDBY**: The device enters the STANDBY mode when Chip_EN (register bit) = 0. In this mode, all the OUTx are shut down, but the registers retain the data and keep it available via I²C/SPI. STANDBY is the low-power-consumption mode, when all circuit functions are disabled. I_{CC} is 15 µA (maximum).
- **THERMAL SHUTDOWN**: The device automatically enters the THERMAL SHUTDOWN mode when the junction temperature exceeds 160°C (typical). In this mode, all the OUTx outputs are shut down. If the junction temperature decreases below 150°C (typical), the device returns to the NORMAL mode.

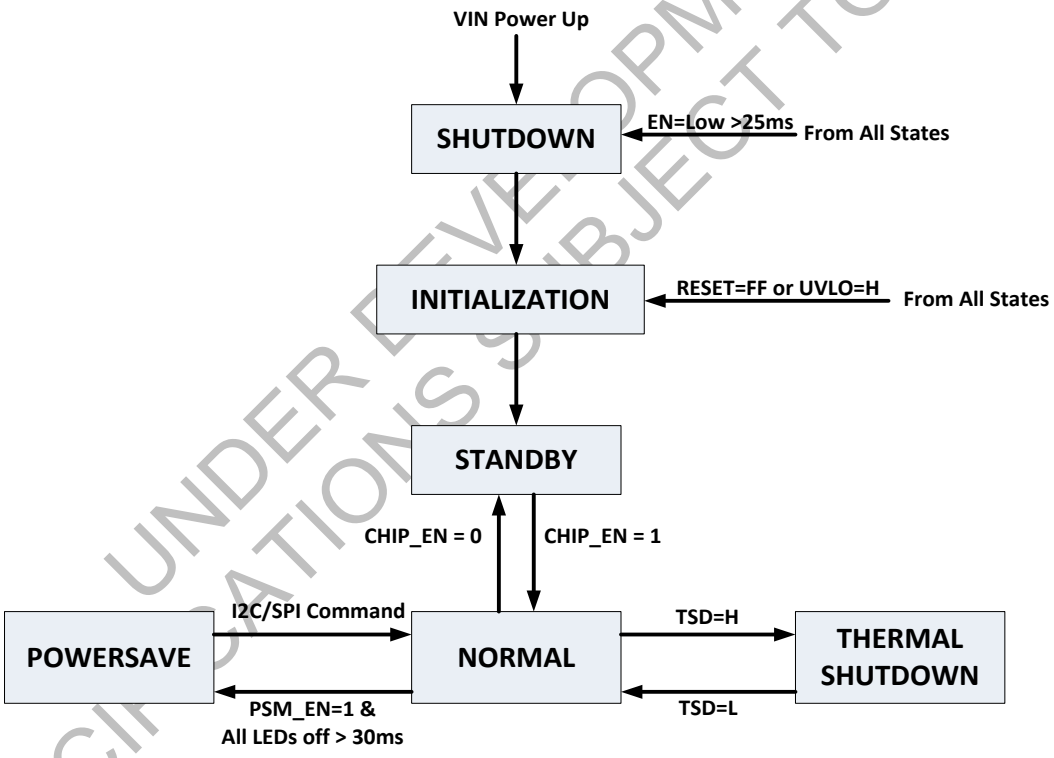

Figure 10. Functional Modes

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Functional Description (Cont'd)

3. Programming (SPI)

3.1 SPI-compatible Interface

3.1.1 SPI INITIALIZATION

Upon the release of power-on-reset (RESETn), the SPI slave in Digital Block waits for the chip selection signal (SPICS_SCL) from the SPI master. The output SPI_OUT of the chip top is at high impedance until the reception of an active low on the select line.

The duration of the select line (SPICS_SCL) should be compliant with the lead and lag time requirements.

Lead time: 1) The time from SPICS_SCL low to SPISCL_ADDR1 high
2) Least lead time is half clock period

Lag time: 1) The time from SPISCL_ADDR1 low to SPICS_SCL high
2) Least lag time is one clock period

3.1.2 Write operation

A '1' on bit (R/W) of the SPI request frame indicates a write request from the SPI Master. Bits A6 to A0 provide the address of the register to which the data is to be written. The contents of the frame from bit D7 to D0 is written into the respective register with last positive edge of the SPISCL_ADDR1 in the current SPI frame.

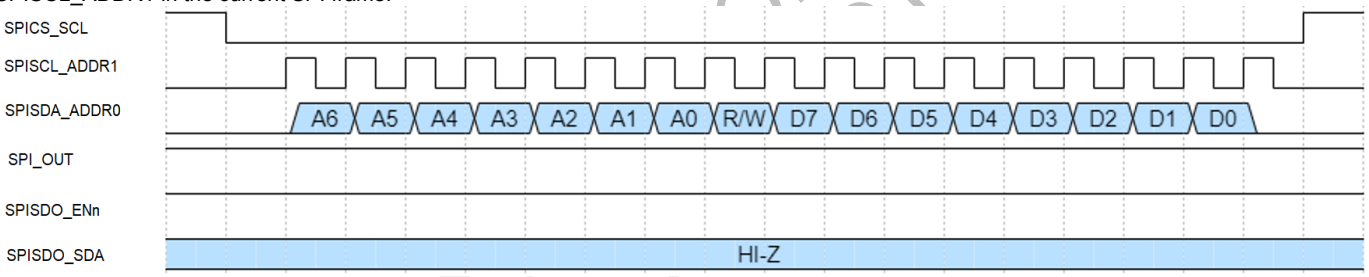

Figure 11. SPI write transaction

3.1.3 Read operation

A read request from the SPI master is decoded with the read/write enable bit (R/W). A '0' on bit (R/W) of the frame indicates a read request from the master.
Bits A6 to A0 provide the address of the register. For a valid address, the 8-bit contents of the respective register is read out. For invalid addresses (out-of range/unused addresses) the response will be a default value (zero).

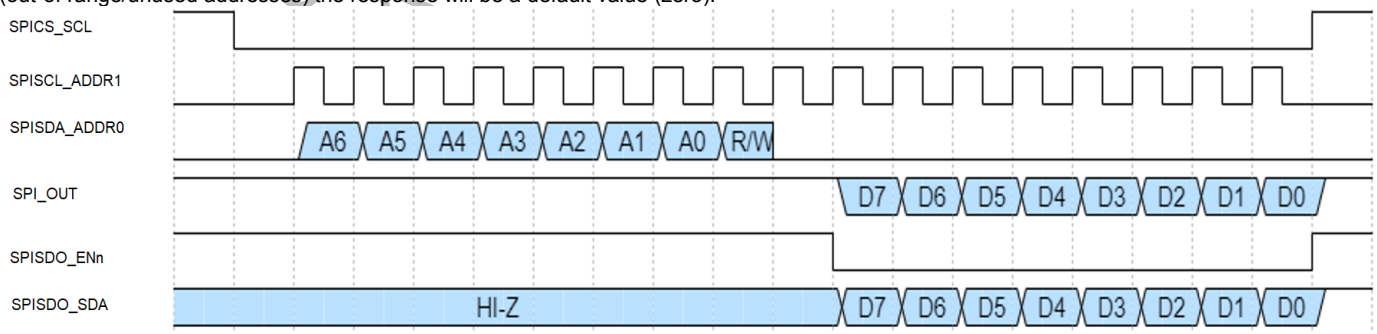

Figure 12. SPI read transaction

Functional Description (Cont'd)

4. Programming (I2C)

4.1 I2C Interface

The I2C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a peripheral depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle.

4.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

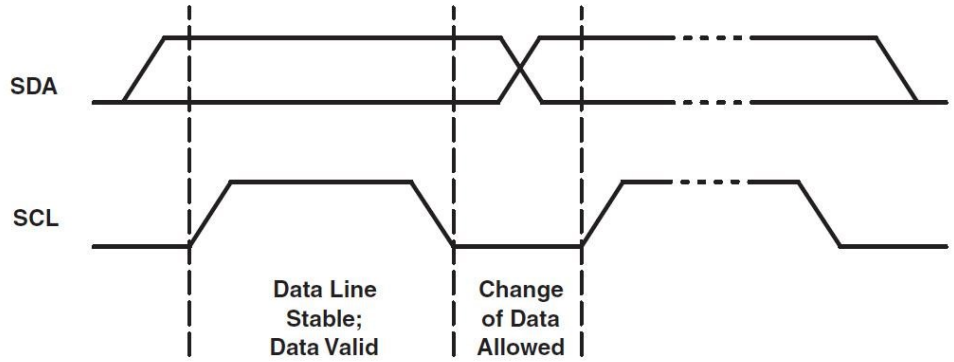

Figure 13. Data Validity

4.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus controller always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus controller can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

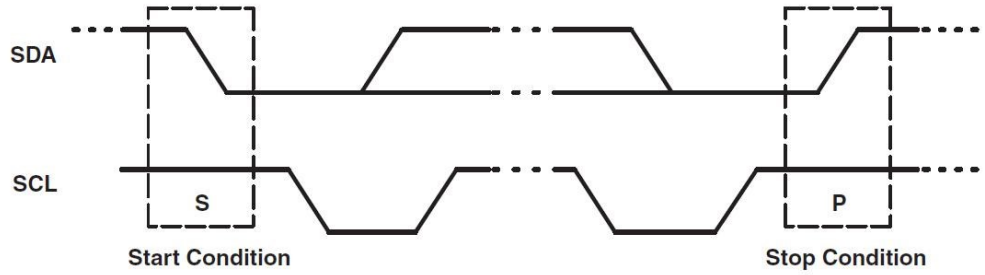

Figure 14. Start and Stop Conditions

Functional Description (Cont'd)

4.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most-significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the controller. The controller releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge-after-every-byte rule. When the controller is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the peripheral. This negative acknowledge still includes the acknowledge clock pulse (generated by the controller), but the SDA line is not pulled down.

After the START condition, the bus controller sends a chip address. This address is seven bits long followed by an eighth bit, which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

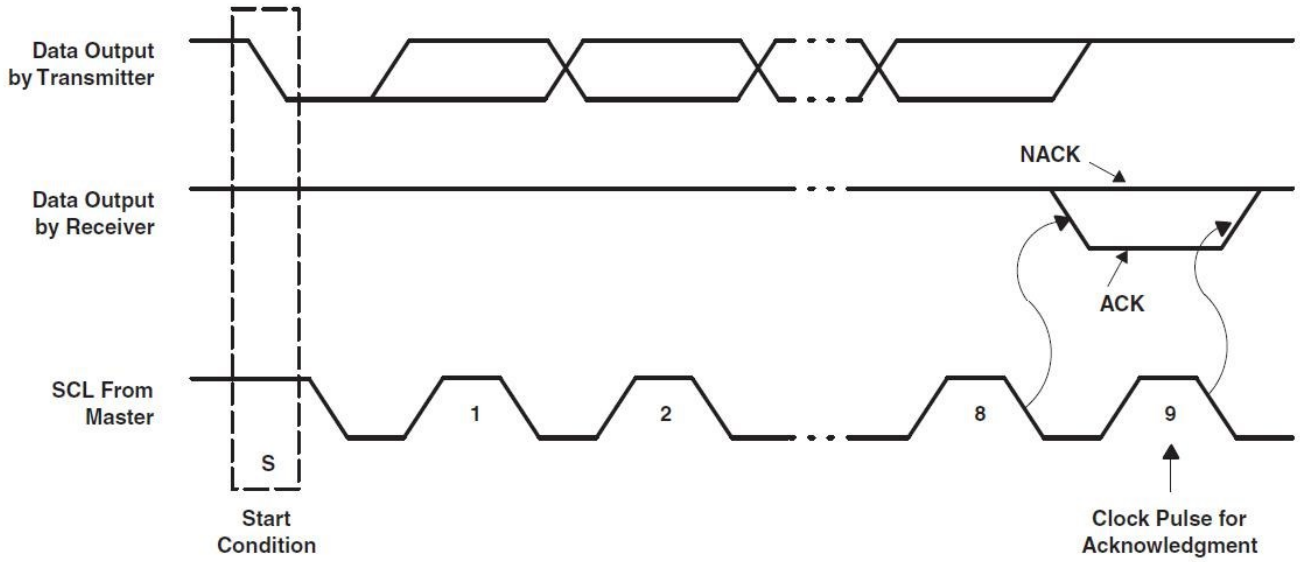

Figure 15. Acknowledge and Not Acknowledge on I²C Bus

Functional Description (Cont'd)

4.1.4 I2C Peripheral Addressing

The device peripheral address is defined by connecting GND or VIO to the SPISDA_ADDR0 and SPISCL_ADDR1 pins. A total of 4 independent peripheral addresses can be realized by combinations when GND or VIO is connected to the SPISDA_ADDR0 and SPISCL_ADDR1 pins (see Table 2 and Table 3).

The device responds to a broadcast peripheral address regardless of the setting of the SPISDA_ADDR0 and SPISCL_ADDR1 pins. Global writes to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I²C bus contain the same value in the addressed register.

Table 2. Slave-Address Combinations

SPISCL_ADDR1	SPISDA_ADDR0	PERIPHERAL ADDRESS	
		INDEPENDENT	BROADCAST
GND	GND	011 0000	001 1100
GND	VIO	011 0001	
VIO	GND	011 0010	
VIO	VIO	011 0011	

Table 3. Chip Address

	PERIPHERAL ADDRESS							R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	0	1	1	0	0	SPISCL_ADDR1	SPISDA_ADDR0	1 or 0
Broadcast	0	0	1	1	1	0	0	1 or 0

4.1.5 Control-Register Write Cycle

- The controller device generates a start condition.
- The controller device sends the peripheral address (7 bits) and the data direction bit (R/W = 0).
- The peripheral device sends an acknowledge signal if the peripheral address is correct.
- The controller device sends the control register address (8 bits).
- The peripheral device sends an acknowledge signal.
- The controller device sends the data byte to be written to the addressed register.
- The peripheral device sends an acknowledge signal.
- If the controller device sends further data bytes, the control register address of the peripheral is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The write cycle ends when the controller device creates a stop condition.

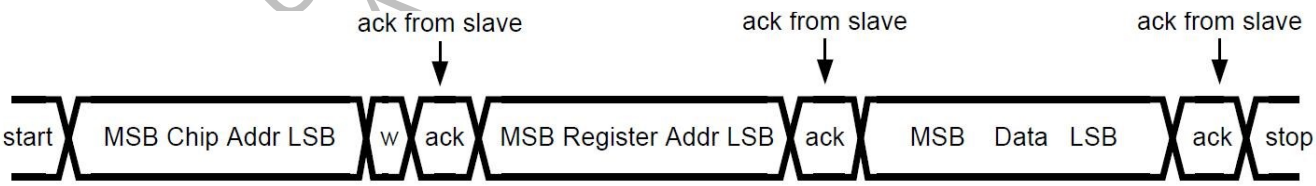

Figure 16. Write Cycle

Functional Description (Cont'd)

4.1.6 Control-Register Read Cycle

- The controller device generates a start condition.
- The controller device sends the peripheral address (7 bits) and the data direction bit (R/W = 0).
- The peripheral device sends an acknowledge signal if the slave address is correct.
- The controller device sends the control register address (8 bits).
- The peripheral device sends an acknowledge signal.
- The controller device generates a repeated-start condition.
- The controller device sends the peripheral address (7 bits) and the data direction bit (R/W = 1).
- The peripheral device sends an acknowledge signal if the peripheral address is correct.
- The peripheral device sends the data byte from the addressed register.
- If the controller device sends an acknowledge signal, the control-register address is incremented by 1. The peripheral device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the controller device does not generate an acknowledge signal after a data byte and generates a stop condition.

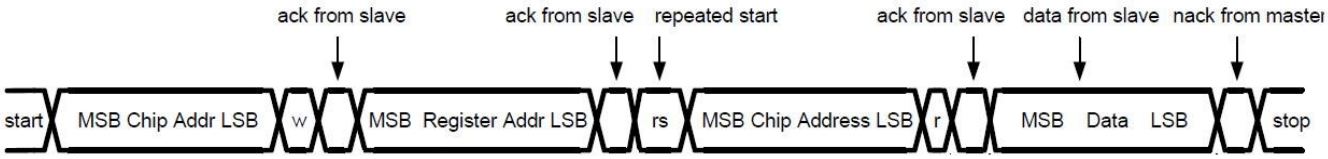

Figure 17. Read Cycle

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Registers Map Description

5.1 Registers Map:

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
00h	DEVICE_CONFIG0	RESERVED	CHIP_EN	RESERVED						00h
01h	DEVICE_CONFIG1	Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current_Option	LED_Global_Off	AEh
02h	LED_CONFIG0	LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN	00h
03h	LED_CONFIG1	RESERVED				LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN	00h
04h	BANK_BRIGHTNESS	Bank_Brightness								FFh
05h	BANK_A_COLOR	Bank_A_Color								00h
06h	BANK_B_COLOR	Bank_B_Color								00h
07h	BANK_C_COLOR	Bank_C_Color								00h
08h	RGB0_BRIGHTNESS	RGB0_Brightness								FFh
09h	RGB1_BRIGHTNESS	RGB1_Brightness								FFh
0Ah	RGB2_BRIGHTNESS	RGB2_Brightness								FFh
0Bh	RGB3_BRIGHTNESS	RGB3_Brightness								FFh
0Ch	RGB4_BRIGHTNESS	RGB4_Brightness								FFh
0Dh	RGB5_BRIGHTNESS	RGB5_Brightness								FFh
0Eh	RGB6_BRIGHTNESS	RGB6_Brightness								FFh
0Fh	RGB7_BRIGHTNESS	RGB7_Brightness								FFh
10h	RGB8_BRIGHTNESS	RGB8_Brightness								FFh
11h	RGB9_BRIGHTNESS	RGB9_Brightness								FFh
12h	RGB10_BRIGHTNESS	RGB10_Brightness								FFh
13h	RGB11_BRIGHTNESS	RGB11_Brightness								FFh
14h	R0_COLOR	R0_Color								00h
15h	G0_COLOR	G0_Color								00h
16h	B0_COLOR	B0_Color								00h
17h	R1_COLOR	R1_Color								00h
18h	G1_COLOR	G1_Color								00h
19h	B1_COLOR	B1_Color								00h
1Ah	R2_COLOR	R2_Color								00h
1Bh	G2_COLOR	G2_Color								00h
1Ch	B2_COLOR	B2_Color								00h
1Dh	R3_COLOR	R3_Color								00h
1Eh	G3_COLOR	G3_Color								00h
1Fh	B3_COLOR	B3_Color								00h
20h	R4_COLOR	R4_Color								00h
21h	G4_COLOR	G4_Color								00h
22h	B4_COLOR	B4_Color								00h
23h	R5_COLOR	R5_Color								00h
24h	G5_COLOR	G5_Color								00h
25h	B5_COLOR	B5_Color								00h
26h	R6_COLOR	R6_Color								00h
27h	G6_COLOR	G6_Color								00h
28h	B6_COLOR	B6_Color								00h
29h	R7_COLOR	R7_Color								00h
2Ah	G7_COLOR	G7_Color								00h
2Bh	B7_COLOR	B7_Color								00h
2Ch	R8_COLOR	R8_Color								00h
2Dh	G8_COLOR	G8_Color								00h
2Eh	B8_COLOR	B8_Color								00h
2Fh	R9_COLOR	R9_Color								00h
30h	G9_COLOR	G9_Color								00h
31h	B9_COLOR	B9_Color								00h
32h	R10_COLOR	R10_Color								00h
33h	G10_COLOR	G10_Color								00h
34h	B10_COLOR	B10_Color								00h
35h	R11_COLOR	R11_Color								00h
36h	G11_COLOR	G11_Color								00h
37h	B11_COLOR	B11_Color								00h
38h	RESET	RESET								00h
65h	FLAG	RESERVED			FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN	10h
66h	LED_GLOBAL_DIMMING	RESERVED		G5	G4	G3	G2	G1	G0	00h
67h	Fault Wait	RESERVED						FW1	FW0	00h
68h	MASK and CLR	RESERVED	Por_Mask	Preuvlo_Mask	Preotp_Mask	Short_Mask	Open_Mask	Clr_Fault	Clr_Por	00h

ADVANCED INFORMATION

Register Maps Description (Cont'd)

ADDR	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	DEFAULT
6Ah	OPEN_MASK0	Open_Mask_OUT7	Open_Mask_OUT6	Open_Mask_OUT5	Open_Mask_OUT4	Open_Mask_OUT3	Open_Mask_OUT2	Open_Mask_OUT1	Open_Mask_OUT0	00h
6Bh	OPEN_MASK1	Open_Mask_OUT15	Open_Mask_OUT14	Open_Mask_OUT13	Open_Mask_OUT12	Open_Mask_OUT11	Open_Mask_OUT10	Open_Mask_OUT9	Open_Mask_OUT8	00h
6Ch	OPEN_MASK2	Open_Mask_OUT23	Open_Mask_OUT22	Open_Mask_OUT21	Open_Mask_OUT20	Open_Mask_OUT19	Open_Mask_OUT18	Open_Mask_OUT17	Open_Mask_OUT16	00h
6Dh	OPEN_MASK3	Open_Mask_OUT31	Open_Mask_OUT30	Open_Mask_OUT29	Open_Mask_OUT28	Open_Mask_OUT27	Open_Mask_OUT26	Open_Mask_OUT25	Open_Mask_OUT24	00h
6Eh	OPEN_MASK4	RESERVED				Open_Mask_OUT35	Open_Mask_OUT34	Open_Mask_OUT33	Open_Mask_OUT32	00h
6Fh	SHORT_MASK0	Short_Mask_OUT7	Short_Mask_OUT6	Short_Mask_OUT5	Short_Mask_OUT4	Short_Mask_OUT3	Short_Mask_OUT2	Short_Mask_OUT1	Short_Mask_OUT0	00h
70h	SHORT_MASK1	Short_Mask_OUT15	Short_Mask_OUT14	Short_Mask_OUT13	Short_Mask_OUT12	Short_Mask_OUT11	Short_Mask_OUT10	Short_Mask_OUT9	Short_Mask_OUT8	00h
71h	SHORT_MASK2	Short_Mask_OUT23	Short_Mask_OUT22	Short_Mask_OUT21	Short_Mask_OUT20	Short_Mask_OUT19	Short_Mask_OUT18	Short_Mask_OUT17	Short_Mask_OUT16	00h
74h	SHORT_MASK3	Short_Mask_OUT31	Short_Mask_OUT30	Short_Mask_OUT29	Short_Mask_OUT28	Short_Mask_OUT27	Short_Mask_OUT26	Short_Mask_OUT25	Short_Mask_OUT24	00h
75h	SHORT_MASK4	RESERVED				Short_Mask_OUT35	Short_Mask_OUT34	Short_Mask_OUT33	Short_Mask_OUT32	00h
76h	OPEN_FAULT0	Open_Fault_OUT7	Open_Fault_OUT6	Open_Fault_OUT5	Open_Fault_OUT4	Open_Fault_OUT3	Open_Fault_OUT2	Open_Fault_OUT1	Open_Fault_OUT0	00h
77h	OPEN_FAULT1	Open_Fault_OUT15	Open_Fault_OUT14	Open_Fault_OUT13	Open_Fault_OUT12	Open_Fault_OUT11	Open_Fault_OUT10	Open_Fault_OUT9	Open_Fault_OUT8	00h
78h	OPEN_FAULT2	Open_Fault_OUT23	Open_Fault_OUT22	Open_Fault_OUT21	Open_Fault_OUT20	Open_Fault_OUT19	Open_Fault_OUT18	Open_Fault_OUT17	Open_Fault_OUT16	00h
79h	OPEN_FAULT3	Open_Fault_OUT31	Open_Fault_OUT30	Open_Fault_OUT29	Open_Fault_OUT28	Open_Fault_OUT27	Open_Fault_OUT26	Open_Fault_OUT25	Open_Fault_OUT24	00h
7Ah	OPEN_FAULT4	RESERVED				Open_Fault_OUT35	Open_Fault_OUT34	Open_Fault_OUT33	Open_Fault_OUT32	00h
7Bh	SHORT_FAULT0	Short_Fault_OUT7	Short_Fault_OUT6	Short_Fault_OUT5	Short_Fault_OUT4	Short_Fault_OUT3	Short_Fault_OUT2	Short_Fault_OUT1	Short_Fault_OUT0	00h
7Ch	SHORT_FAULT1	Short_Fault_OUT15	Short_Fault_OUT14	Short_Fault_OUT13	Short_Fault_OUT12	Short_Fault_OUT11	Short_Fault_OUT10	Short_Fault_OUT9	Short_Fault_OUT8	00h
7Dh	SHORT_FAULT2	Short_Fault_OUT23	Short_Fault_OUT22	Short_Fault_OUT21	Short_Fault_OUT20	Short_Fault_OUT19	Short_Fault_OUT18	Short_Fault_OUT17	Short_Fault_OUT16	00h
7Eh	SHORT_FAULT3	Short_Fault_OUT31	Short_Fault_OUT30	Short_Fault_OUT29	Short_Fault_OUT28	Short_Fault_OUT27	Short_Fault_OUT26	Short_Fault_OUT25	Short_Fault_OUT24	00h
7Fh	SHORT_FAULT4	RESERVED				Short_Fault_OUT35	Short_Fault_OUT34	Short_Fault_OUT33	Short_Fault_OUT32	00h

Register Maps Description (Cont'd)

Table 5.2 Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
$\overline{W}$	$\overline{W}$	Write
Power On Reset or Default value		
(xxh)		Value after POR or default value

5.1.1 DEVICE_CONFIG0 (Address = 00h) [default = 00h]

Figure 18. DEVICE_CONFIG0 Register

7	6	5	4	3	2	1	0
RESERVED	Chip_EN	RESERVED					
R/$\overline{W}$-(00h)	R/$\overline{W}$-(00h)	R/$\overline{W}$-(00h)					
Reserved	0=AL5887 Disabled 1=AL5887 Enabled	Reserved					

ADVANCED INFORMATION

Register Maps Description (Cont'd)

5.1.2 DEVICE_CONFIG1 (Address = 01h) [default= AEh]

Figure 19. DEVICE_CONFIG1 Register

7	6	5	4	3	2	1	0
Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current_Option	LED_Global_Off
R/W-(01h)	R/W-(00h)	R/W-(01h)	R/W-(00h)	R/W-(01h)	R/W-(01h)	R/W-(01h)	R/W-(00h)
0 = Disabled 1 =Enabled	-	0 = Linear curve Enabled 1 = Logarithmic curve Enabled	0 = Power Save Mode Disabled 1 = Power Save Mode Enabled	-	0 = Disabled 1 = Enabled	0 = 29.25mA 1 = 39mA	0 = Normal Operation 1 = Shutdown all LEDs

5.1.3 LED_CONFIG0 (Address = 02h) [default= 00h]

Figure 20. LED_CONFIG0 Register

7	6	5	4	3	2	1	0
LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN
R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)
0 =Independent Mode Enabled 1 =Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled

5.1.4 LED_CONFIG1 (Address = 03h) [default= 00h]

Figure 21. LED_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED				LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN
R/W-(00h)				R/W-(00h)	R/W-(00h)	R/W-(00h)	R/W-(00h)
Reserved				0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled	0 =Independent Mode Enabled 1 = Bank Mode Enabled

Register Maps Description (Cont'd)

5.1.5 BANK_BRIGHTNESS (Address = 04h) [default= FFh]

Figure 22. BANK_BRIGTHNESS Register

7	6	5	4	3	2	1	0
BANK_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.6 BANK_A_COLOR (Address = 05h) [default= 00h]

Figure 23. BANK_A_COLOR Register

7	6	5	4	3	2	1	0
BANK_R_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

5.1.7 BANK_B_COLOR (Address = 06h) [default= 00h]

Figure 24. BANK_B_COLOR Register

7	6	5	4	3	2	1	0
BANK_G_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

5.1.8 BANK_C_COLOR (Address = 07h) [default= 00h]

Figure 25. BANK_C_COLOR Register

7	6	5	4	3	2	1	0
BANK_B_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

Register Maps Description (Cont'd)

5.1.9 RGB0_BRIGHTNESS (Address = 08h) [default= FFh]

Figure 26. RGB0_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB0_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.10 RGB1_BRIGHTNESS (Address = 09h) [default= FFh]

Figure 27. RGB1_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB1_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.11 RGB2_BRIGHTNESS (Address = 0Ah) [default= FFh]

Figure 28. RGB2_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB2_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.12 RGB3_BRIGHTNESS (Address = 0Bh) [default= FFh]

Figure 29. RGB3_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB3_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

Register Maps Description (Cont'd)

5.1.13 RGB4_BRIGHTNESS (Address = 0Ch) [default= FFh]

Figure 30. RGB4_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB4_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.14 RGB5_BRIGHTNESS (Address = 0Dh) [default= FFh]

Figure 31. RGB5_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB5_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.15 RGB6_BRIGHTNESS (Address = 0Eh) [default= FFh]

Figure 32. RGB6_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB6_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.16 RGB7_BRIGHTNESS (Address = 0Fh) [default= FFh]

Figure 33. RGB7_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB7_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

Register Maps Description (Cont'd)

5.1.17 RGB8_BRIGHTNESS (Address = 10h) [default= FFh]

Figure 34. RGB8_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB8_BRIGHTNESS							
R/$\overline{W}$-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.18 RGB9_BRIGHTNESS (Address = 11h) [default= FFh]

Figure 35. RGB9_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB9_BRIGHTNESS							
R/$\overline{W}$-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.19 RGB10_BRIGHTNESS (Address = 12h) [default= FFh]

Figure 36. RGB10_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB10_BRIGHTNESS							
R/$\overline{W}$-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

5.1.20 RGB11_BRIGHTNESS (Address = 13h) [default= FFh]

Figure 37. RGB11_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB11_BRIGHTNESS							
R/$\overline{W}$-(FFh)							
00h = 0% of full brightness ... 80h = 50% of full ... FFh = 100 % of full brightness							

Register Maps Description (Cont'd)

5.1.21 Rx_COLORx=0 to 11(Address = 14h to 1Eh) [default= 00h]

Figure 38. Rx_COLOR Register

7	6	5	4	3	2	1	0
Rx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

5.1.22 Gx_COLORx=0 to 11(Address = 1Fh to 2Ah) [default= 00h]

Figure 39. Gx_COLOR Register

7	6	5	4	3	2	1	0
Gx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

5.1.23 Bx_COLORx=0 to 11(Address = 2Bh to 37h) [default= 00h]

Figure 40. Bx_COLOR Register

7	6	5	4	3	2	1	0
Bx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0% ... 80h = The color mixing percentage is 50% ... FFh = The color mixing percentage is 100%							

ADVANCED INFORMATION

Register Maps Description (Cont'd)

5.1.24 RESET (Address = 38h) [default= 00h]

Figure 41. RESET Register

7	6	5	4	3	2	1	0
RESET							
W-(00h)							
FFh = Resets all the registers to default value.							

5.1.25 FLAG (Address = 65h) [default= 00h]

Figure 42. FLAG Register

7	6	5	4	3	2	1	0
RESERVED			FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN
R/W-(00h)							
RESERVED			0 = No POR fault reported. 1 = POR fault reported	0 = No Pre_UVLO fault reported. 1 = Pre_UVLO fault reported.	0 = No Pre_OTP fault reported. 1 = Pre_OTP fault reported.	0 = No short fault reported on any channel. 1 = Short fault reported on any of the channels.	0 = No open fault reported on any channel. 1 = Open fault reported on any of the channels.

5.1.26 LED_GLOBAL_DIMMING (Address = 66h) [default= 00h]

Figure 43. LED_GLOBAL Register

7	6	5	4	3	2	1	0
Reserved		LED_Global_6	LED_Global_5	LED_Global_4	LED_Global_3	LED_Global_2	LED_Global_1
R/W-(00h)							
Reserved	6-bit LED Global current setting. See Section 2.7.1 for details						

5.1.27 LED_GLOBAL_DIMMING (Address = 67h) [default= 00h]

Figure 44. LED_GLOBAL Register

7	6	5	4	3	2	1	0
Reserved						FW1	FW0
R/W-(00h)							
Reserved						0 = as per table 1b 1 = as per table 1b	0 = as per table 1b 1 = as per table 1b

5.1.28 MASK and CLR (Address = 68h) [default= 00h]

Figure 45. MASK and CLR Register

7	6	5	4	3	2	1	0
RESERVED	Por_Mask	Preuvlo_Mask	Preotp_Mask	Short_Mask	Open_Mask	Clr_Fault	Clr_Por
R/W-(00h)							
01h = Write 1 to clear all flags	0 = POR mask turned off 1 = POR mask turned on	0 = Pre-Uvlo mask turned off 1 = Pre-Uvlo mask turned on	0 = Pre-OTP mask turned off 1 = Pre-OTP mask turned on	0 = Short detection mask turned off 1 = Short detection mask turned on	0 = Open detection mask turned off 1 = Open detection mask turned on	0 = Clearing faults turned off 1 = Clears the Faults	0 = Clearing POR turned off 1 = Clears the POR fault

Register Maps Description (Cont'd)

5.1.29 OPEN_MASK0 (Address = 6Ah) [default= 00h]

Figure 46. OPEN_MASK0 Register

7	6	5	4	3	2	1	0
Open_Mask_OUT7	Open_Mask_OUT6	Open_Mask_OUT5	Open_Mask_OUT4	Open_Mask_OUT3	Open_Mask_OUT2	Open_Mask_OUT1	Open_Mask_OUT0
R/W-(00h)							
0 = OUT7 Open detection mask turned off 1 = OUT7 Open detection mask turned on	0 = OUT6 Open detection mask turned off 1 = OUT6 Open detection mask turned on	0 = OUT5 Open detection mask turned off 1 = OUT5 Open detection mask turned on	0 = OUT4 Open detection mask turned off 1 = OUT4 Open detection mask turned on	0 = OUT3 Open detection mask turned off 1 = OUT3 Open detection mask turned on	0 = OUT2 Open detection mask turned off 1 = OUT2 Open detection mask turned on	0 = OUT1 Open detection mask turned off 1 = OUT1 Open detection mask turned on	0 = OUT0 Open detection mask turned off 1 = OUT0 Open detection mask turned on

5.1.30 OPEN_MASK01 (Address = 6Bh) [default= 00h]

Figure 47. OPEN_MASK1 Register

7	6	5	4	3	2	1	0
Open_Mask_OUT15	Open_Mask_OUT14	Open_Mask_OUT13	Open_Mask_OUT12	Open_Mask_OUT11	Open_Mask_OUT10	Open_Mask_OUT9	Open_Mask_OUT8
R/W-(00h)							
0 = OUT15 Open detection mask turned off 1 = OUT15 Open detection mask turned on	0 = OUT14 Open detection mask turned off 1 = OUT14 Open detection mask turned on	0 = OUT13 Open detection mask turned off 1 = OUT13 Open detection mask turned on	0 = OUT12 Open detection mask turned off 1 = OUT12 Open detection mask turned on	0 = OUT11 Open detection mask turned off 1 = OUT11 Open detection mask turned on	0 = OUT10 Open detection mask turned off 1 = OUT10 Open detection mask turned on	0 = OUT9 Open detection mask turned off 1 = OUT9 Open detection mask turned on	0 = OUT8 Open detection mask turned off 1 = OUT8 Open detection mask turned on

Register Maps Description (Cont'd)

5.1.31 OPEN_MASK2 (Address = 6Ch) [default= 00h]

Figure 48. OPEN_MASK2 Register

7	6	5	4	3	2	1	0
Open_Mask_OUT23	Open_Mask_OUT22	Open_Mask_OUT21	Open_Mask_OUT20	Open_Mask_OUT19	Open_Mask_OUT18	Open_Mask_OUT17	Open_Mask_OUT16
R/$\overline{W}$-(00h)							
0 = OUT23 Open detection mask turned off 1 = OUT23 Open detection mask turned on	0 = OUT22 Open detection mask turned off 1 = OUT22 Open detection mask turned on	0 = OUT21 Open detection mask turned off 1 = OUT21 Open detection mask turned on	0 = OUT20 Open detection mask turned off 1 = OUT20 Open detection mask turned on	0 = OUT19 Open detection mask turned off 1 = OUT19 Open detection mask turned on	0 = OUT18 Open detection mask turned off 1 = OUT18 Open detection mask turned on	0 = OUT17 Open detection mask turned off 1 = OUT17 Open detection mask turned on	0 = OUT16 Open detection mask turned off 1 = OUT16 Open detection mask turned on

Register Maps Description (Cont'd)

5.1.32 OPEN_MASK3 (Address = 6Dh) [default= 00h]

Figure 49. OPEN_MASK3 Register

7	6	5	4	3	2	1	0
Open_Mask_OUT31	Open_Mask_OUT30	Open_Mask_OUT29	Open_Mask_OUT28	Open_Mask_OUT27	Open_Mask_OUT26	Open_Mask_OUT25	Open_Mask_OUT24
R/W-(00h)							
0 = OUT31 Open detection mask turned off 1 = OUT31 Open detection mask turned on	0 = OUT30 Open detection mask turned off 1 = OUT30 Open detection mask turned on	0 = OUT29 Open detection mask turned off 1 = OUT29 Open detection mask turned on	0 = OUT28 Open detection mask turned off 1 = OUT28 Open detection mask turned on	0 = OUT27 Open detection mask turned off 1 = OUT27 Open detection mask turned on	0 = OUT26 Open detection mask turned off 1 = OUT26 Open detection mask turned on	0 = OUT25 Open detection mask turned off 1 = OUT25 Open detection mask turned on	0 = OUT24 Open detection mask turned off 1 = OUT24 Open detection mask turned on

5.1.33 OPEN_MASK4 (Address = 6Eh) [default= 00h]

Figure 50. OPEN_MASK4 Register

7	6	5	4	3	2	1	0
RESERVED				Open_Mask_OUT35	Open_Mask_OUT34	Open_Mask_OUT33	Open_Mask_OUT32
R/W-(00h)							
RESERVED				0 = OUT35 Open detection mask turned off 1 = OUT35 Open detection mask turned on	0 = OUT34 Open detection mask turned off 1 = OUT34 Open detection mask turned on	0 = OUT33 Open detection mask turned off 1 = OUT33 Open detection mask turned on	0 = OUT32 Open detection mask turned off 1 = OUT32 Open detection mask turned on

ADVANCED INFORMATION

Register Maps Description (Cont'd)

5.1.34 SHORT_MASK0 (Address = 6Fh) [default= 00h]

Figure 51. SHORT_MASK0 Register

7	6	5	4	3	2	1	0
SHORT_Mask_OUT7	SHORT_Mask_OUT6	SHORT_Mask_OUT5	SHORT_Mask_OUT4	SHORT_Mask_OUT3	SHORT_Mask_OUT2	SHORT_Mask_OUT1	SHORT_Mask_OUT0
R/W-(00h)							
0 = OUT7 SHORT detection mask turned off 1 = OUT7 SHORT detection mask turned on	0 = OUT6 SHORT detection mask turned off 1 = OUT6 SHORT detection mask turned on	0 = OUT5 SHORT detection mask turned off 1 = OUT5 SHORT detection mask turned on	0 = OUT4 SHORT detection mask turned off 1 = OUT4 SHORT detection mask turned on	0 = OUT3 SHORT detection mask turned off 1 = OUT3 SHORT detection mask turned on	0 = OUT2 SHORT detection mask turned off 1 = OUT2 SHORT detection mask turned on	0 = OUT1 SHORT detection mask turned off 1 = OUT1 SHORT detection mask turned on	0 = OUT0 SHORT detection mask turned off 1 = OUT0 SHORT detection mask turned on

5.1.35 SHORT_MASK1 (Address = 70h) [default= 00h]

Figure 52. SHORT_MASK1 Register

7	6	5	4	3	2	1	0
SHORT_Mask_OUT15	SHORT_Mask_OUT14	SHORT_Mask_OUT13	SHORT_Mask_OUT12	SHORT_Mask_OUT11	SHORT_Mask_OUT10	SHORT_Mask_OUT9	SHORT_Mask_OUT8
R/W-(00h)							
0 = OUT15SHORT detection mask turned off 1 = OUT15SHORT detection mask turned on	0 = OUT14SHORT detection mask turned off 1 = OUT14SHORT detection mask turned on	0 = OUT13SHORT detection mask turned off 1 = OUT13SHORT detection mask turned on	0 = OUT12SHORT detection mask turned off 1 = OUT12SHORT detection mask turned on	0 = OUT11SHORT detection mask turned off 1 = OUT11SHORT detection mask turned on	0 = OUT10SHORT detection mask turned off 1 = OUT10SHORT detection mask turned on	0 = OUT9 SHORT detection mask turned off 1 = OUT9 SHORT detection mask turned on	0 = OUT8 SHORT detection mask turned off 1 = OUT8 SHORT detection mask turned on

5.1.36 SHORT_MASK2 (Address = 71h) [default= 00h]

Figure 53. SHORT_MASK2 Register

7	6	5	4	3	2	1	0
SHORT_Mask_OUT23	SHORT_Mask_OUT22	SHORT_Mask_OUT21	SHORT_Mask_OUT20	SHORT_Mask_OUT19	SHORT_Mask_OUT18	SHORT_Mask_OUT17	SHORT_Mask_OUT16
R/W-(00h)							
0 = OUT23SHORT detection mask turned off 1 = OUT23SHORT detection mask turned on	0 = OUT22SHORT detection mask turned off 1 = OUT22SHORT detection mask turned on	0 = OUT21SHORT detection mask turned off 1 = OUT21SHORT detection mask turned on	0 = OUT20SHORT detection mask turned off 1 = OUT20SHORT detection mask turned on	0 = OUT19SHORT detection mask turned off 1 = OUT19SHORT detection mask turned on	0 = OUT18SHORT detection mask turned off 1 = OUT18SHORT detection mask turned on	0 = OUT17SHORT detection mask turned off 1 = OUT17SHORT detection mask turned on	0 = OUT16SHORT detection mask turned off 1 = OUT16SHORT detection mask turned on

Register Maps Description (Cont'd)

5.1.37 SHORT_MASK3 (Address = 74h) [default= 00h]

Figure 54. SHORT_MASK3 Register

7	6	5	4	3	2	1	0
SHORT_Mask_OUT31	SHORT_Mask_OUT30	SHORT_Mask_OUT29	SHORT_Mask_OUT28	SHORT_Mask_OUT27	SHORT_Mask_OUT26	SHORT_Mask_OUT25	SHORT_Mask_OUT24
R/W-(00h)							
0 = OUT31SHORT detection mask turned off 1 = OUT31SHORT detection mask turned on	0 = OUT30SHORT detection mask turned off 1 = OUT30SHORT detection mask turned on	0 = OUT29SHORT detection mask turned off 1 = OUT29SHORT detection mask turned on	0 = OUT28SHORT detection mask turned off 1 = OUT28SHORT detection mask turned on	0 = OUT27SHORT detection mask turned off 1 = OUT27SHORT detection mask turned on	0 = OUT26SHORT detection mask turned off 1 = OUT26SHORT detection mask turned on	0 = OUT25SHORT detection mask turned off 1 = OUT25SHORT detection mask turned on	0 = OUT24SHORT detection mask turned off 1 = OUT24SHORT detection mask turned on

5.1.38 SHORT_MASK4 (Address = 75h) [default= 00h]

Figure 55. SHORT_MASK4 Register

7	6	5	4	3	2	1	0
RESERVED				SHORT_Mask_OUT35	SHORT_Mask_OUT34	SHORT_Mask_OUT33	SHORT_Mask_OUT32
R/W-(00h)							
RESERVED				0 = OUT35SHORT detection mask turned off 1 = OUT35SHORT detection mask turned on	0 = OUT34SHORT detection mask turned off 1 = OUT34SHORT detection mask turned on	0 = OUT33SHORT detection mask turned off 1 = OUT33SHORT detection mask turned on	0 = OUT32SHORT detection mask turned off 1 = OUT32SHORT detection mask turned on

Register Maps Description (Cont'd)

5.1.39 OPEN_FAULT0 (Address = 76h) [default= 00h]

Figure 56. OPEN_FAULT0 Register

7	6	5	4	3	2	1	0
Open_Fault_OUT 7	Open_Fault_OUT 6	Open_Fault_OUT 5	Open_Fault_OUT 4	Open_Fault_OUT 3	Open_Fault_OUT 2	Open_Fault_O UT1	Open_Fault_O UT0
R/$\overline{W}$-(00h)							
0 = OUT7 Open Fault not detected 1 = OUT7 Open Fault detected	0 = OUT6 Open Fault not detected 1 = OUT6 Open Fault detected	0 = OUT5 Open Fault not detected 1 = OUT5 Open Fault detected	0 = OUT4 Open Fault not detected 1 = OUT4 Open Fault detected	0 = OUT3 Open Fault not detected 1 = OUT3 Open Fault detected	0 = OUT2 Open Fault not detected 1 = OUT2 Open Fault detected	0 = OUT1 Open Fault not detected 1 = OUT1 Open Fault detected	0 = OUT0 Open Fault not detected 1 = OUT0 Open Fault detected

5.1.40 OPEN_FAULT1 (Address = 77h) [default= 00h]

Figure 57. OPEN_FAULT1 Register

7	6	5	4	3	2	1	0
Open_Fault_OUT 15	Open_Fault_OUT 14	Open_Fault_OUT 13	Open_Fault_OUT 12	Open_Fault_OUT 11	Open_Fault_OUT 10	Open_Fault_O UT9	Open_Fault_O UT8
R/$\overline{W}$-(00h)							
0 = OUT15 Open Fault not detected 1 = OUT15 Open Fault detected	0 = OUT14 Open Fault not detected 1 = OUT14 Open Fault detected	0 = OUT13 Open Fault not detected 1 = OUT13 Open Fault detected	0 = OUT12 Open Fault not detected 1 = OUT12 Open Fault detected	0 = OUT11 Open Fault not detected 1 = OUT11 Open Fault detected	0 = OUT10 Open Fault not detected 1 = OUT10 Open Fault detected	0 = OUT9 Open Fault not detected 1 = OUT9 Open Fault detected	0 = OUT8 Open Fault not detected 1 = OUT8 Open Fault detected

5.1.41 OPEN_FAULT2 (Address = 78h) [default= 00h]

Figure 58. OPEN_FAULT2 Register

7	6	5	4	3	2	1	0
Open_Fault_OUT 23	Open_Fault_OUT 22	Open_Fault_OUT 21	Open_Fault_OUT 20	Open_Fault_OUT 19	Open_Fault_OUT 18	Open_Fault_O UT17	Open_Fault_O UT16
R/$\overline{W}$-(00h)							
0 = OUT23 Open Fault not detected 1 = OUT23 Open Fault detected	0 = OUT22 Open Fault not detected 1 = OUT22 Open Fault detected	0 = OUT21 Open Fault not detected 1 = OUT21 Open Fault detected	0 = OUT20 Open Fault not detected 1 = OUT20 Open Fault detected	0 = OUT19 Open Fault not detected 1 = OUT19 Open Fault detected	0 = OUT18 Open Fault not detected 1 = OUT18 Open Fault detected	0 = OUT17 Open Fault not detected 1 = OUT17 Open Fault detected	0 = OUT16 Open Fault not detected 1 = OUT16 Open Fault detected

Register Maps Description (Cont'd)

5.1.42 OPEN_FAULT3 (Address = 79h) [default= 00h]

Figure 59. OPEN_FAULT3 Register

7	6	5	4	3	2	1	0
Open_Fault_OUT 31	Open_Fault_OUT 30	Open_Fault_OUT 29	Open_Fault_OUT 28	Open_Fault_OUT 27	Open_Fault_OUT 26	Open_Fault_O UT25	Open_Fault_O UT24
R/W-(00h)							
0 = OUT31 Open Fault not detected 1 = OUT31 Open Fault detected	0 = OUT30 Open Fault not detected 1 = OUT30 Open Fault detected	0 = OUT29 Open Fault not detected 1 = OUT29 Open Fault detected	0 = OUT28 Open Fault not detected 1 = OUT28 Open Fault detected	0 = OUT27 Open Fault not detected 1 = OUT27 Open Fault detected	0 = OUT26 Open Fault not detected 1 = OUT26 Open Fault detected	0 = OUT25 Open Fault not detected 1 = OUT25 Open Fault detected	0 = OUT24 Open Fault not detected 1 = OUT24 Open Fault detected

5.1.43 OPEN_FAULT4 (Address = 7Ah) [default= 00h]

Figure 60. OPEN_FAULT4 Register

7	6	5	4	3	2	1	0
RESERVED				Open_Fault_OUT 35	Open_Fault_OUT 34	Open_Fault_O UT33	Open_Fault_O UT32
R/W-(00h)							
RESERVED				0 = OUT35 Open Fault not detected 1 = OUT35 Open Fault detected	0 = OUT34 Open Fault not detected 1 = OUT34 Open Fault detected	0 = OUT33 Open Fault not detected 1 = OUT33 Open Fault detected	0 = OUT32 Open Fault not detected 1 = OUT32 Open Fault detected

Register Maps Description (Cont'd)

5.1.44 SHORT_FAULT0 (Address = 7Bh) [default= 00h]

Figure 61. SHORT_FAULT0 Register

7	6	5	4	3	2	1	0
SHORT_Fault_OUT7	SHORT_Fault_OUT6	SHORT_Fault_OUT5	SHORT_Fault_OUT4	SHORT_Fault_OUT3	SHORT_Fault_OUT2	SHORT_Fault_OUT1	SHORT_Fault_OUT0
R/W-(00h)							
0 = OUT7 SHORT Fault not detected 1 = OUT7 SHORT Fault detected	0 = OUT6 SHORT Fault not detected 1 = OUT6 SHORT Fault detected	0 = OUT5 SHORT Fault not detected 1 = OUT5 SHORT Fault detected	0 = OUT4 SHORT Fault not detected 1 = OUT4 SHORT Fault detected	0 = OUT3 SHORT Fault not detected 1 = OUT3 SHORT Fault detected	0 = OUT2 SHORT Fault not detected 1 = OUT2 SHORT Fault detected	0 = OUT1 SHORT Fault not detected 1 = OUT1 SHORT Fault detected	0 = OUT0 SHORT Fault not detected 1 = OUT0 SHORT Fault detected

5.1.45 SHORT_FAULT1 (Address = 7Ch) [default= 00h]

Figure 62. SHORT_FAULT1 Register

7	6	5	4	3	2	1	0
SHORT_Fault_OUT15	SHORT_Fault_OUT14	SHORT_Fault_OUT13	SHORT_Fault_OUT12	SHORT_Fault_OUT11	SHORT_Fault_OUT10	SHORT_Fault_OUT9	SHORT_Fault_OUT8
R/W-(00h)							
0 = OUT15 SHORT Fault not detected 1 = OUT15 SHORT Fault detected	0 = OUT14 SHORT Fault not detected 1 = OUT14 SHORT Fault detected	0 = OUT13 SHORT Fault not detected 1 = OUT13 SHORT Fault detected	0 = OUT12 SHORT Fault not detected 1 = OUT12 SHORT Fault detected	0 = OUT11 SHORT Fault not detected 1 = OUT11 SHORT Fault detected	0 = OUT10 SHORT Fault not detected 1 = OUT10 SHORT Fault detected	0 = OUT9 SHORT Fault not detected 1 = OUT9 SHORT Fault detected	0 = OUT8 SHORT Fault not detected 1 = OUT8 SHORT Fault detected

5.1.46 SHORT_FAULT2 (Address = 7Dh) [default= 00h]

Figure 63. SHORT_FAULT2 Register

7	6	5	4	3	2	1	0
SHORT_Fault_OUT23	SHORT_Fault_OUT22	SHORT_Fault_OUT21	SHORT_Fault_OUT20	SHORT_Fault_OUT19	SHORT_Fault_OUT18	SHORT_Fault_OUT17	SHORT_Fault_OUT16
R/W-(00h)							
0 = OUT23 SHORT Fault not detected 1 = OUT23 SHORT Fault detected	0 = OUT22 SHORT Fault not detected 1 = OUT22 SHORT Fault detected	0 = OUT21 SHORT Fault not detected 1 = OUT21 SHORT Fault detected	0 = OUT20 SHORT Fault not detected 1 = OUT20 SHORT Fault detected	0 = OUT19 SHORT Fault not detected 1 = OUT19 SHORT Fault detected	0 = OUT18 SHORT Fault not detected 1 = OUT18 SHORT Fault detected	0 = OUT17 SHORT Fault not detected 1 = OUT17 SHORT Fault detected	0 = OUT16 SHORT Fault not detected 1 = OUT16 SHORT Fault detected

Register Maps Description (Cont'd)

5.1.47 SHORT_FAULT3 (Address = 7Eh) [default= 00h]

Figure 64. SHORT_FAULT3 Register

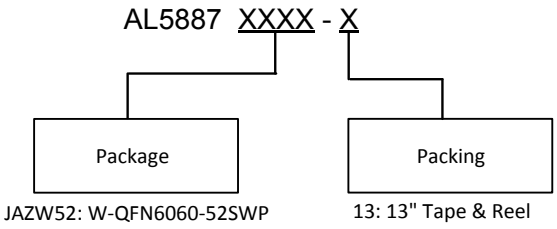
7	6	5	4	3	2	1	0
SHORT_Fault_OUT31	SHORT_Fault_OUT30	SHORT_Fault_OUT29	SHORT_Fault_OUT28	SHORT_Fault_OUT27	SHORT_Fault_OUT26	SHORT_Fault_OUT25	SHORT_Fault_OUT24
R/W-(00h)							
0 = OUT31 SHORT Fault not detected 1 = OUT31 SHORT Fault detected	0 = OUT30 SHORT Fault not detected 1 = OUT30 SHORT Fault detected	0 = OUT29 SHORT Fault not detected 1 = OUT29 SHORT Fault detected	0 = OUT28 SHORT Fault not detected 1 = OUT28 SHORT Fault detected	0 = OUT27 SHORT Fault not detected 1 = OUT27 SHORT Fault detected	0 = OUT26 SHORT Fault not detected 1 = OUT26 SHORT Fault detected	0 = OUT25 SHORT Fault not detected 1 = OUT25 SHORT Fault detected	0 = OUT24 SHORT Fault not detected 1 = OUT24 SHORT Fault detected

5.1.48 SHORT_FAULT4 (Address = 7Fh) [default= 00h]

Figure 65. SHORT_FAULT4 Register

7	6	5	4	3	2	1	0
RESERVED				SHORT_Fault_OUT35	SHORT_Fault_OUT34	SHORT_Fault_OUT33	SHORT_Fault_OUT32
R/W-(00h)							
RESERVED				0 = OUT35 SHORT Fault not detected 1 = OUT35 SHORT Fault detected	0 = OUT34 SHORT Fault not detected 1 = OUT34 SHORT Fault detected	0 = OUT33 SHORT Fault not detected 1 = OUT33 SHORT Fault detected	0 = OUT32 SHORT Fault not detected 1 = OUT32 SHORT Fault detected

Ordering Information

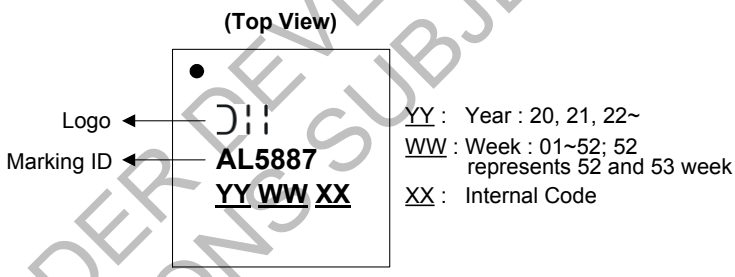


Part Number	Package Code	Packaging	7"Tape and Reel	
			Quantity	Part Number Suffix
AL5887JAZW52-13	JAZW52	W-QFN6060-52SWP (Note 11)	4000/Tape & Reel	-13

Note: 11. For packaging details, go to our website at http://www.diodes.com/products/packages.htm.

Marking Information

W-QFN6060-52 (SWP)



Mechanical Data

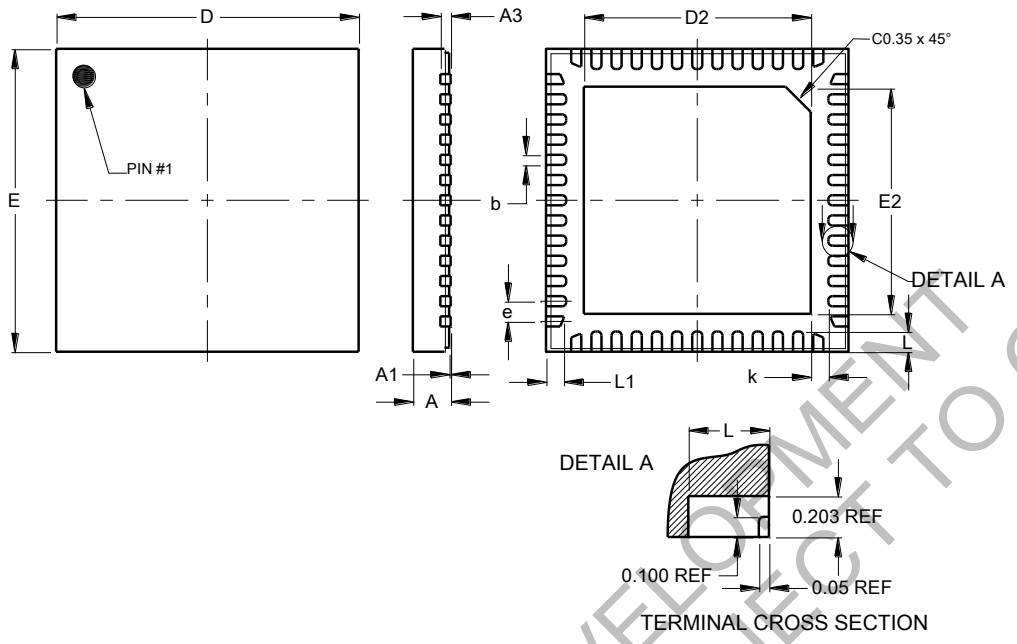
Package W-QFN6060-52 (SWP)

- Moisture Sensitivity: MSL Level 3 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per JESD22-B102
- Weight: 0.0095 grams (Approximate)

ADVANCED INFORMATION

Package Outline Dimensions

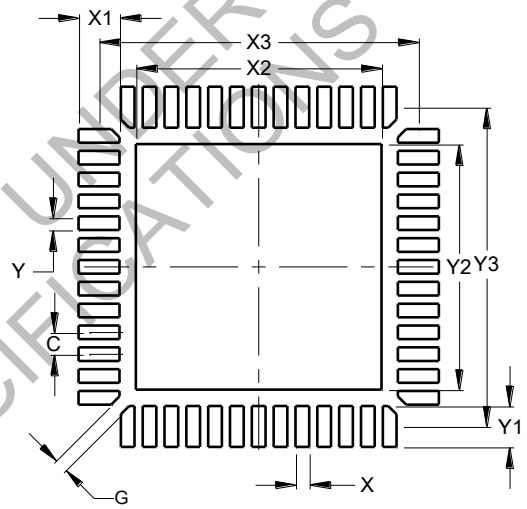
W-QFN6060-52/SWP (Type A1)



W-QFN6060-52/SWP (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.700	0.800	0.750
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.15	0.25	0.20
D	6.00 BSC		
D2	4.45	4.55	4.50
E	6.00 BSC		
E2	4.45	4.55	4.50
e	0.40 BSC		
k	0.20	--	--
L	0.35	0.45	0.40
L1	0.30	0.40	0.35
All Dimensions in mm			

Suggested Pad Layout

W-QFN6060-52/SWP (Type A1)



Dimensions	Value (in mm)
C	0.400
G	0.250
X	0.250
X1	0.750
X2	4.500
X3	5.850
Y	0.250
Y1	0.750
Y2	4.500
Y3	5.850

ALL DIMENSIONS ARE NOMINAL VALUES SHOWN IN MILLIMETERS

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These numbers may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

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