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OBC/DCDC solution with Stellar-E MCU

Sep, NEV LAB,Shanghai

OBC system team

LV3 DFAE training agenda(26th Sep)

- Team member introduce —Arrow,ST,09:30-09:45
- Stellar-E MCU highlight feature for OBC/DCDC topology —Jacob,09:45-10:15
- ST product introduce for OBC/DCDC(SiC MOSFET,SBC) —Jacob,10:25-10:45
- 22kW combo solution introduce(requirement, solution structure, status) —Jacob,10:45-11:30
- 22kW combo system firmware develop introduce —Charos,13:30-14:30

OBC+DCDC LV3 DFAE training program

	ST LV3 DFAE technical support	Disty responsible & action required	Task duration time

Step1	• **Stellar-E total solution training**
	  • Stellar-E highlight feature for OBC,DCDC
	  • System controller structure & topology
	  • ST highlight product introduce (SiC,SBC)
	  • 22kW combo system solution introduce
		• Vinfast current OBC,DCDC system block (topology, power, safety, controller structure)
		• Market OBC,DCDC technical trend (power, safety, controller structure, OTA)
		• Competitor solution information, key PN. and adv/disadv
			WK2

Step2	• **On site NEV CC co-work for customer prj**
	  • Set up NEV CC 22kw combo EVM for customer promotion
	  • Customization development based NEV CC 22kw combo platform
		• Assign AE/FAE to familiar 22kw combo EVM and able to setup EVM at CTM side for high power running
		• Assign AE/FAE to test/co-develop for customization requirement at system level
			WK4

Step3	• **Co-develop based Stellar-E 22kw combo platform**
	  • Single phase 6.6kW charging and inverting function R&D
	  • 12V to 800V boost DCDC function R&D
		• Assign R&D team and resource for solution develop
		• Monthly review status with ST team
			WK24

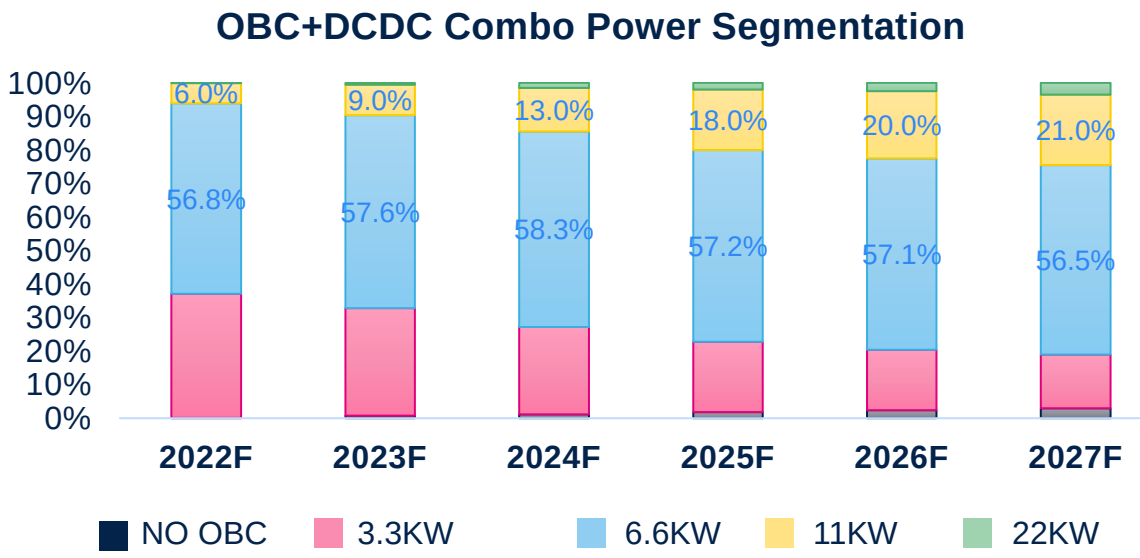
Step4	• **Customer prj support**
	  • MCAL · OS · BSW · RTE support
	  • CDD L9396
		• Assign FAE to support MCU configuration and integration
		• Assign FAE to support SBC register configure according customer requirement
			WK24

OBC DCDC Market

- Leading by Local Player
- Dominate with OBC DCDC Combo solution

Project Leading Customer

Top 10 OBC Supplier	2021 (ku)	YoY	Y21 Market share
Vmax	603	211%	20.9%
FinDreams	455	217%	15.8%
Evtech （杭州富特）	343	178%	11.9%
Tesla(SANMINA-SCI)	312	125%	10.8%
TC charger (杭州铁城)	246	68%	8.5%
Shinry	207	146%	7.2%
Enpower	152	>500%	5.3%
Lihua	136	388%	4.7%
Kostal	119	150%	4.1%
Delta	64	-6%	2.2%
Total	**2,636**		

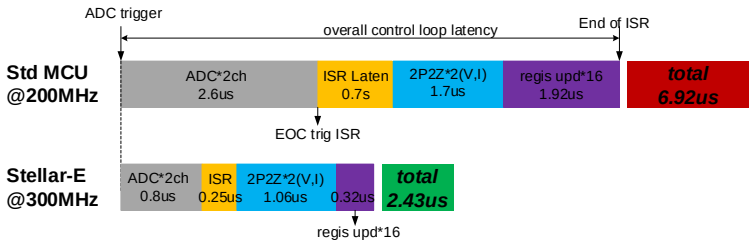


	2022F	2023F	2024F	2025F	2026F	2027F	CAGR Y22 vs Y27
China NEV (M sets)	5.8	7.5	10	12.6	15.1	17.2	24%
Growth Rate		29%	33%	26%	20%	14%	
SAM-Gate driver (M$)	25.4	33.6	46.4	60.2	73.1	83.9	28%
SAM-SBC (M$)	6.2	8.7	12.6	16.9	21.0	24.6	32%
SAM-MCU (M$)	47.7	62.1	83.7	106.4	128.0	146.1	26%
SAM-Power Device (M$)	170.9	233.6	335.9	451.8	559.1	656.3	31%

Stellar E MCU Series

Innovation with Value

Optimized for Power Conversion with SiC/GaN



FAST

- CPU power
- ADC&PWM access
- Protection

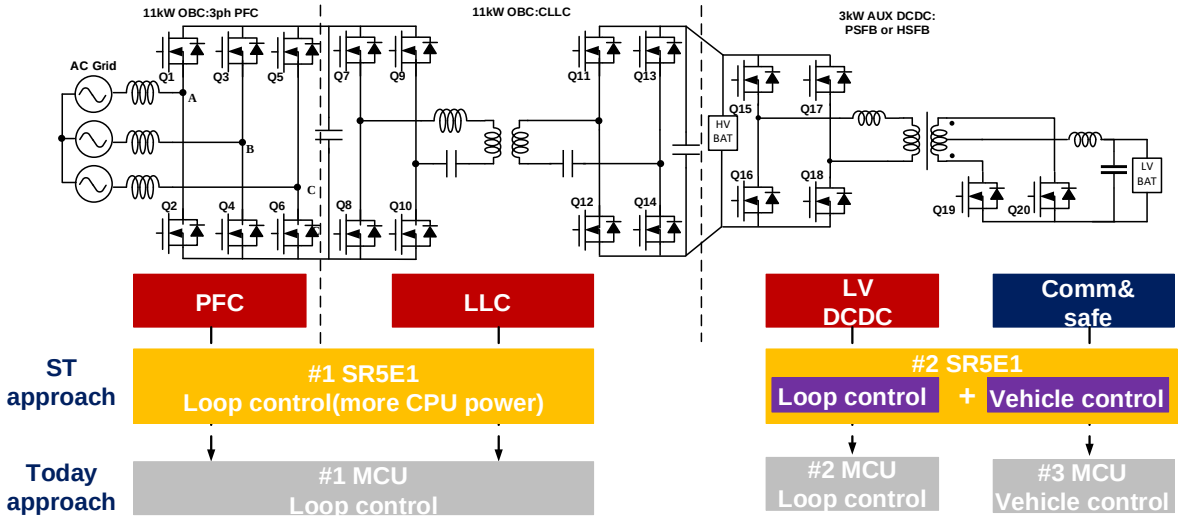
Safe and Secure ARM® Family

BEST

Real Time
Safety
Security

ECU System Cost Optimization

All System Control in
ONE MCU
to drive wide bandgap
Power Technologies



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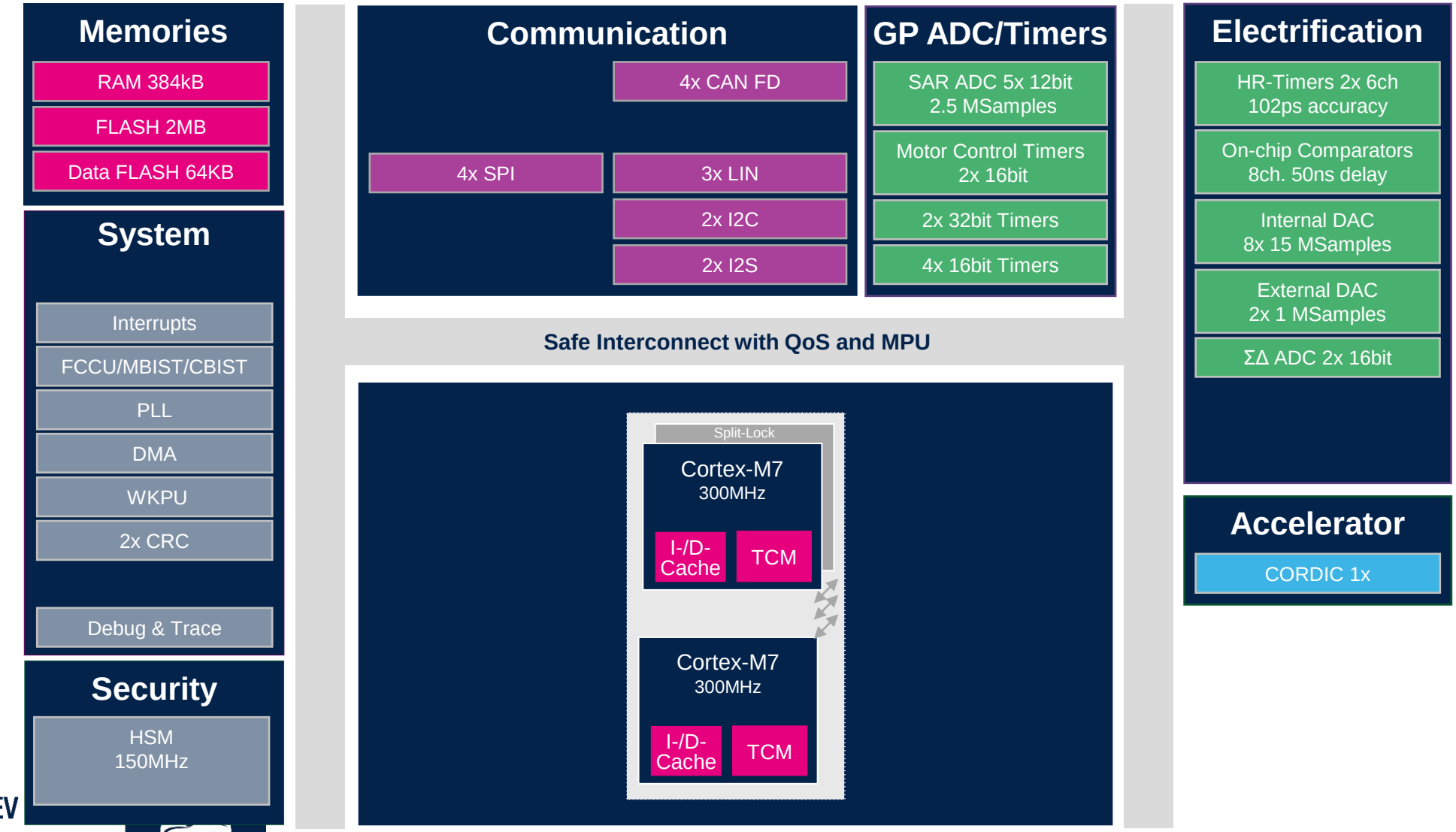
Stellar E1

Device Block Diagram



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OBC+DCDC System Approach

Innovative **Stellar E**lectrification MCU Family

Stellar-E technical highlight for OBC/DCDC	Benefits at system level
• **Ultra-low latency control loop processing** with optimized peripheral access and CPU power to best leverage SiC/GaN	→ **increasing efficiency and extending driving mileage**
• **High resolution PWM** (104ps) to best leverage **GaN/SiC**, **flexible PWM generation** capability for complex topology(magnetic integration 3port DCDC)	→**saving transistor, mechanical size and higher power density**
• Enhance analog with **SARADC (2.5MSPS),analog comparator** (fast protect & cycle by cycle PWM control) , and **DAC(slope compensation for PCMC)**	→**faster control response(dynamic load claimed by LV ECU)**
• Function safety **ASIL-D.**ISO26262 compatible	→**safer power supply to LV ECU(LV3 autopilot)**
• **CAN-FD and hardware OTA** (A/B swap)	→**low maintain cost**
• Hardware security module**(HSM)**	→**protect personal privacy**

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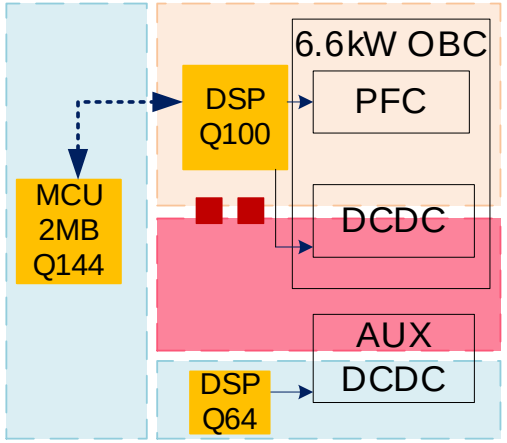
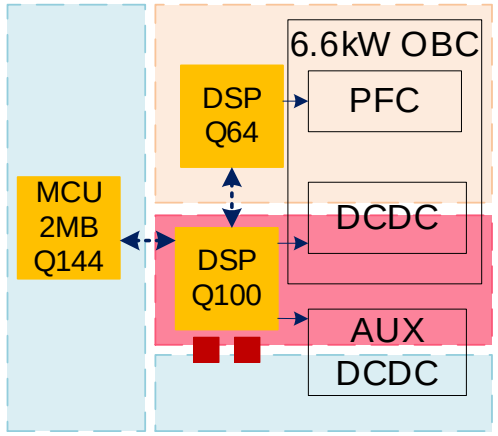
MCU solution BOM benchmark OBC+3KW AUX DCDC

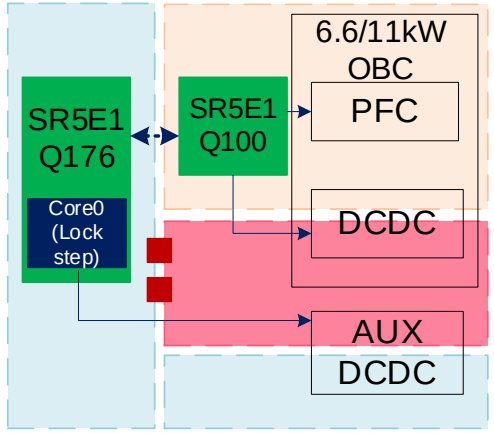
Solution1:2 DSP+1MCU



Solution2: 2 DSP+1MCU

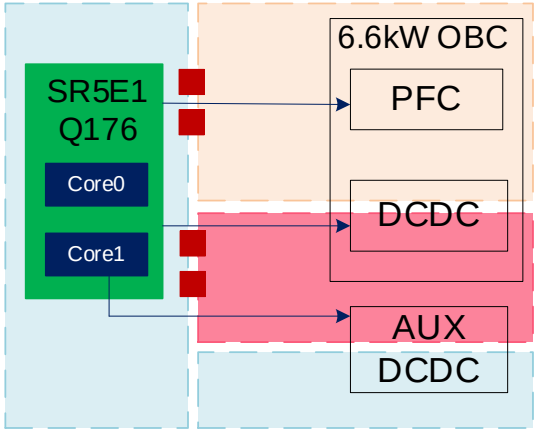


Solution3: 1 DSP+1MCU



- LV SR5E1 replace DSP+MCU
- Peak current mode control(HW current loop)
- LV DCDC ASIL-C/D

Solution4: 1MCU



- Single chip solution
- Peak current mode
- LV DCDC ASIL-B
- Isolation amplifier cost slight increase

Overall BOM benchmark(IC)

Item	Solution1: 2DSP+1MCU	Solution2: 2DSP+1MCU	Solution3: 1 DSP+1 MCU	Solution4: 1MCU
MCU/DSP	DSP*2 MCU:2MB ASIL-D	DSP*2 MCU:2MB ASIL-D	DSP*1 MCU:SR5E1E7	MCU:SR5E1E7
Isolated amplifier	2ch	2ch	2ch	4ch
Digital isolator	4ch	8ch	4ch	0
Basic /reinforce /non-isolation gate driver	4+4+1	6+3	4+4+1	0+8+1

AC GND domain
HV GND domain
LV GND domain
Isolated amplifier
Digital isolator
Competitor MCU
Stellar-E MCU

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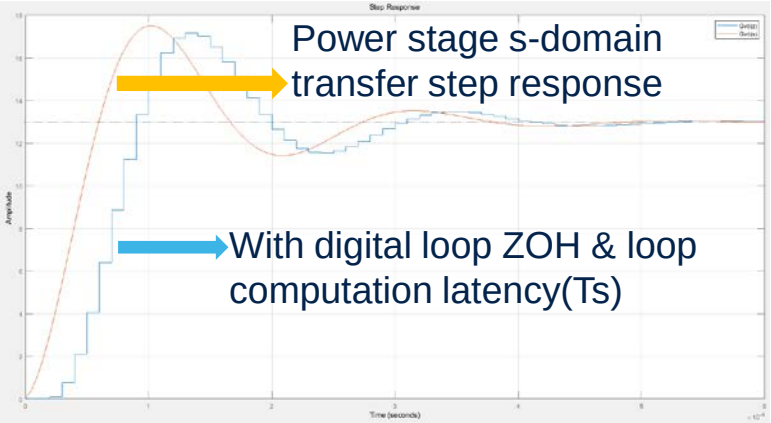
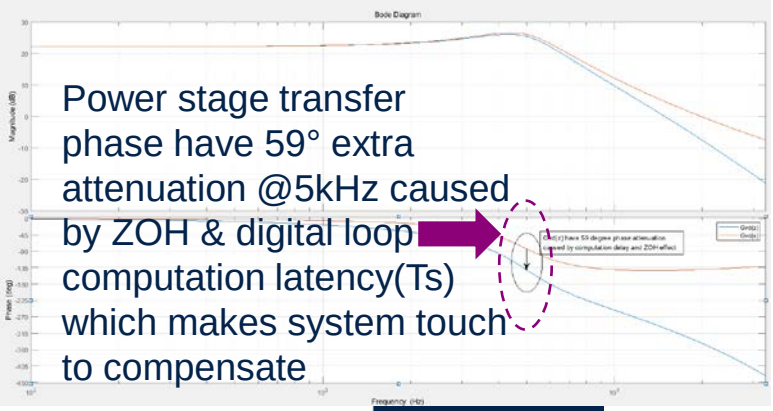
Stellar E MCU highlight for OBC/DCDC topology

May,2022

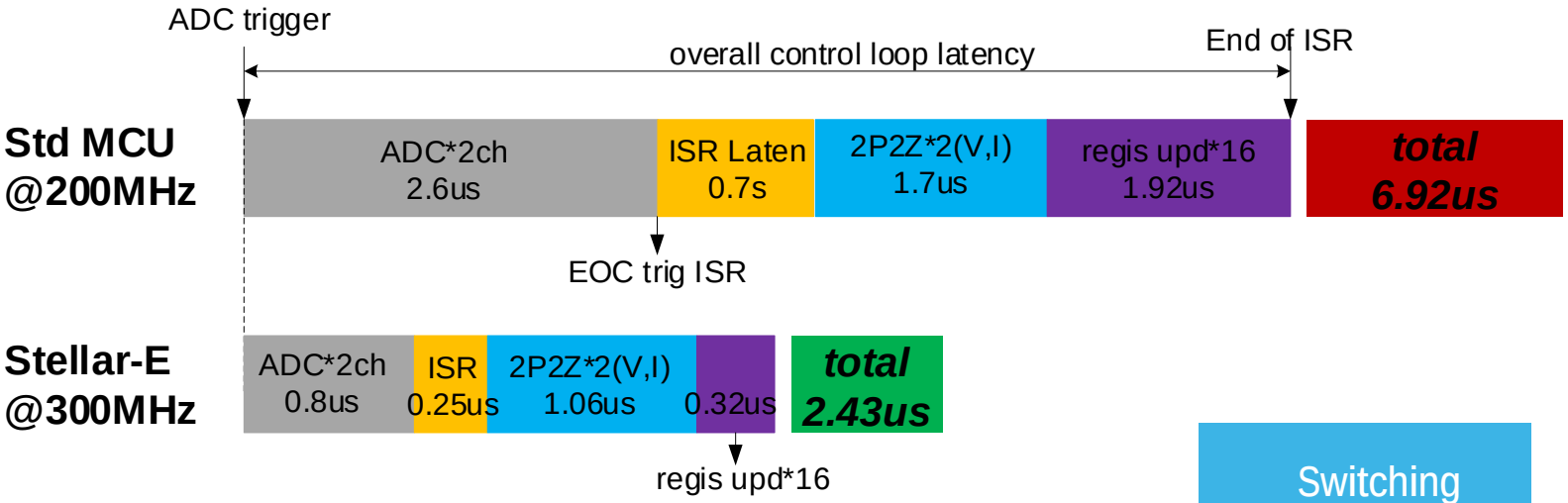
Faster control loop best leverage SiC/GaN

Digital control loop latency effect





Control loop time decreased with Stellar-E



- Bode graph example with PSFB(400V→12V) power stage
- Loop computation delay=Ts(10us) defined from ADC SOC to PWM register updated.
- Control loop example with CLLC topology PFM+phase control.

Stellar
Stellar Electrification MCU

X2~3

Switching Control Frequency to Leverage SiC/GaN

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Scenario0:High resolution timer(HRTIM) for GaN/SiC

High resolution timer(HRTIM) address digital SMPS with high PWM switching frequencies

- Higher duty cycle resolution(Buck/boost…)
- Better accuracy on output voltage
- No limit cycling oscillation issues
- Higher frequency adjustment step resolution in resonant topology(LLC…)

	SiC/GaN freq	PWM counter	ADC granularity	PWM granularity	output control accuracy
Stellar-E PWM resolution **-104ps**	100kHz	96153	4.47mV/tick	0.24mV/tick	Good
	250kHz	38461	4.47mV/tick	0.6mV/tick	Good
	500kHz	19230	4.47mV/tick	1.2mV/tick	Good
	1MHz	9615	4.47mV/tick	2.4mV/tick	Good
STD MCU PWM resolution **-10ns**	100kHz	1000	4.47mV/tick	23.1mV/tick	No Good
	250kHz	400	4.47mV/tick	57.7mV/tick	No Good

Limit cycling oscillation issues:

- Output voltage variation between two PWM ticks has to be equal or smaller than the smallest error variation(limited by voltage between two ADC ticks)

Example:

400-to-12V DC/DC with 18:1 turn ratio buck derived topology
- Switching Frequency: 250 kHz
- Nominal Duty Cycle: 54%(Vo=Vin*D*n)

- PWM Settings
  - Resolution: 1ns
  - Period: 4000 ticks
- ADC Settings:
  - ADC Reference Voltage: 3.3 V
  - ADC Resolution: 12-bit
  - Feedback Voltage Divider:
    - Divider Ratio (Rup/Rdn): 10k/ 2.2k
    - Vfb_ADC @ 12V: 2.164 V
- **Input granularity(ADC):4.46mV/tick**
- **Output granularity(PWM):5.56mV/tick, larger than input granularity and has risk to happen limit cycling oscillation issue.**

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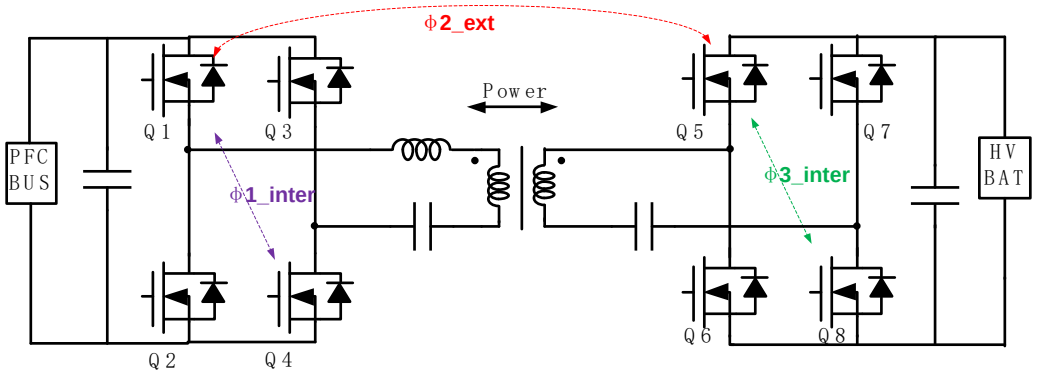
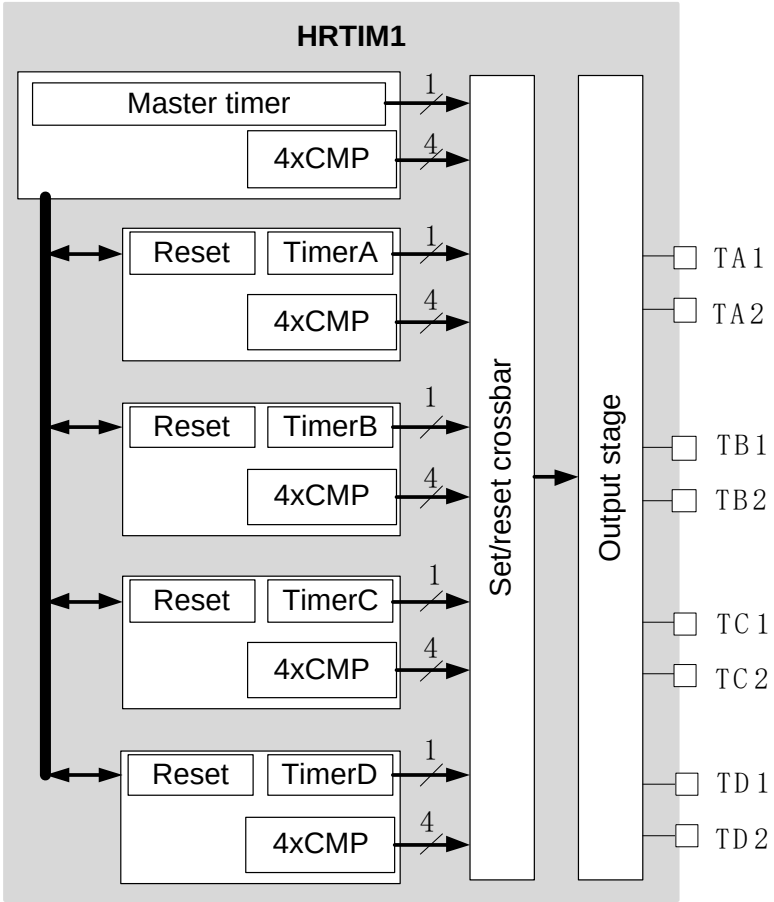
Scenario1:Serial resonant converter(CLLC) : PFM+phase shift control

CLLC topology(OBC)



Stellar-E solution block



Application requirement:

- Pulse frequency modulation(PFM) to all channel and synchronized
- Q1&Q4 internal phase shift φ1_inter and phase shift direction fixed
- Q5&Q8 internal phase shift φ3_inter and phase shift direction fixed
- Q1&Q5 external phase shift φ2_ext and phase shift bi-direction configure
- eg:battery charging φ2_ext∈[0,90°]，battery discharging φ2_ext∈[-90°,0],angle=360°*(PWM rising edge delay time)/Ts. PWM lagging edge side as power topology output.
- Q1&Q2,Q3&Q4,Q5&Q6,Q7&Q8 complementary PWM with deadtime
- Typical switching frequency 100~200kHz
- All channel 50% duty cycle at steady state
- Phase shift & frequency not changing at same PWM cycle

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CLLC PFM + phase shift mix control: HRTIM multi-timer sync & flexible output manage

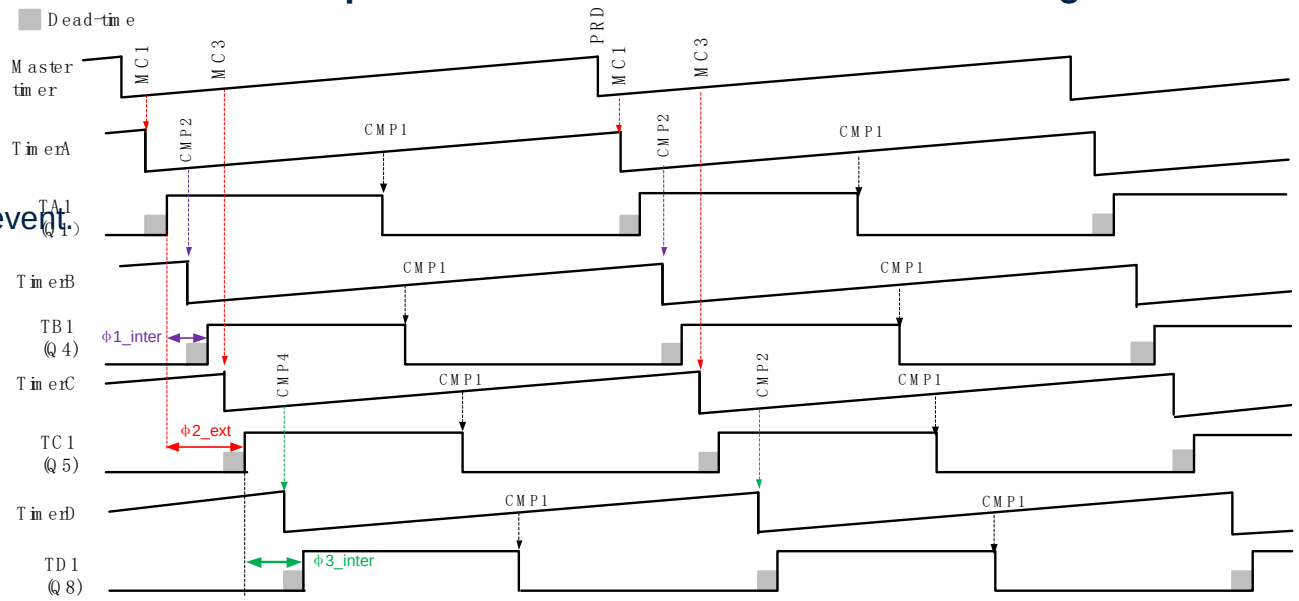
Solution benefits to system

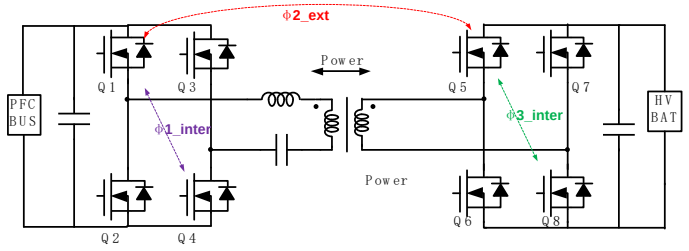
- Phase shift by control **one register and off CPU load**.
- **Multi timer sync by hardware**, more robustness
- Flexible **phase shift direction control** by swap relative value of MC1,MC3
- **All register update by global sync** (Master.PER) or by timer itself counter reset event.

Solution analysis:

- Master timer MC1,MC3 reset Timer A,C to control external phase shift φ2_ext and φ2_ext=abs(MC3-MC1).
- Relative value of MC1,MC3 controls phase shift direction.
  - MC3>MC1, φ2_ext >0;
  - MC3<MC1, φ2_ext <0;
- TimerA.CMP2 reset Timer B to control internal phase shift φ1_inter=TA.CMP2
- TimerC.CMP4 reset Timer D to control internal phase shift φ3_inter=TC.CMP2
- Timer A frequency controlled by proportional changed MC1 & master.PER.
- Output set/reset event may come from timer itself or other timers, refer to right table.

Simplified solution waveform & HRTIM configure





Source		Master timer			TimerA		TimerB	TimerC		TimeD
		CMP1	CMP3	Period	CMP1	CMP2	CMP1	CMP1	CMP4	CMP1
Destination	Master counter reset			√						
	TimerA counter reset	√								
	TimerB counter reset					√				
	TimerC counter reset		√							
	TimerD counter reset								√	
	TA1 output set	√								
	TA1 output reset				√					
	TB1 output set					√				
	TB1 output reset						√			
	TC1 output set		√							
	TC1 output reset							√		
	TD1 output set								√	
	TD1 output reset									√

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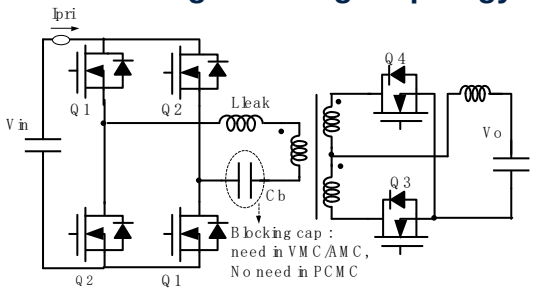
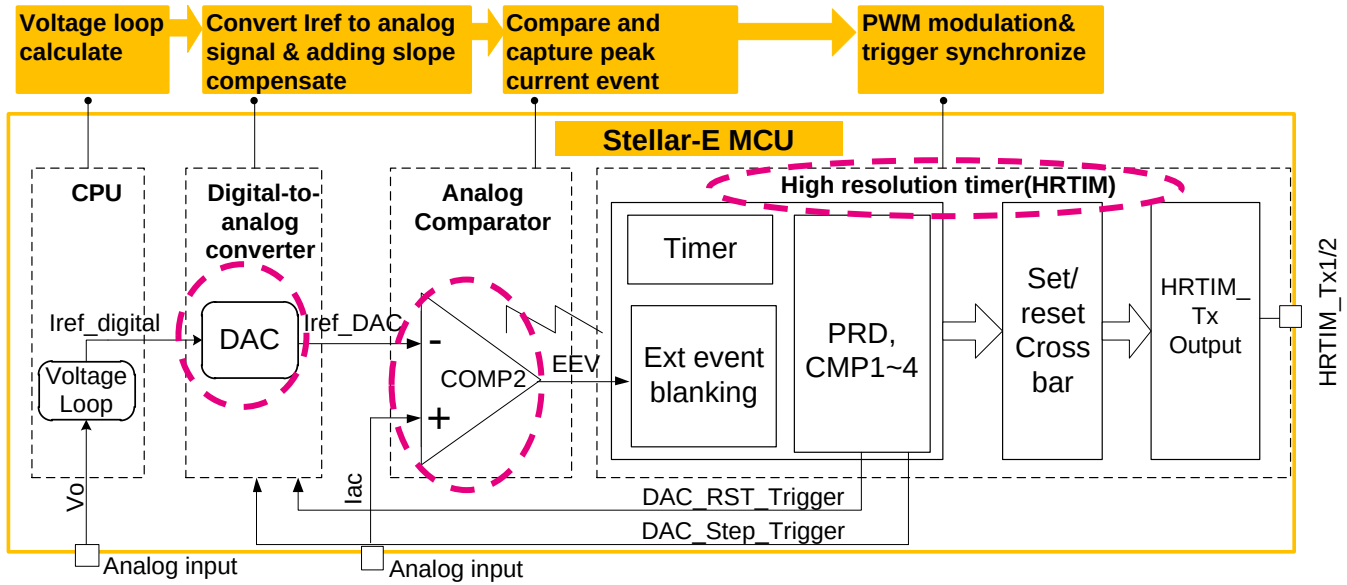
Scenario2:hard switching full bridge(HSFB): Peak current mode control(PCMC)

Hard switching full bridge topology



Stellar-E solution block



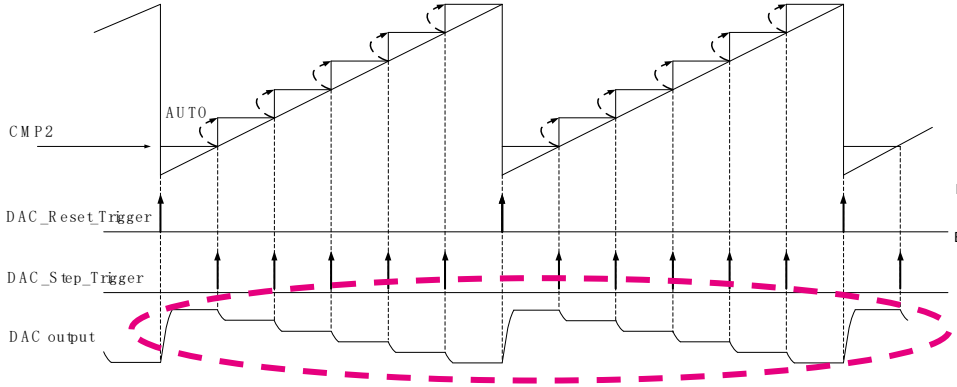
Application requirement:

- Peak current event modulate PWM width
- Q1-2 turn off controlled by comparator event at positive/negative half cycle respectively,Q1&Q4,Q2&Q3 complement with dead-time.
- Analog comparator need slope compensation
- Comparator event need blanking time at Q1,Q2 turn on to avoid false trigger

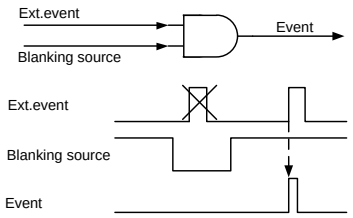
Solution analysis:

- Highlight peripheral : DAC converter, analog comparator, HRTIM PWM module
- Integrated analog comparator issue an event when primary peak current match comparator reference setting by DAC.
- DAC converts digital current reference to analog, dual DAC trigger configured to generate sawtooth reference as a slope compensation to diminish sub-harmonic oscillation in peak current mode control.
- Comparator event sent to HRTIM for PWM modulation. Event blanking used to prevent recovery noise at PWM start.

DAC sawtooth generator (slope compensate for COMP)



Event blanking mode



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HSFB peak current mode control : Analog comparator +DAC+HRTIM

Solution analysis(continue):

- Master timer used to sync all slave timer.
- Timer C/E twice frequency of TimerA/B to distinguish positive & negative half cycle and two blanking window generate for positive & negative half cycle respectively.
- Comparator event within blanking window discarded and filter window define by zero to CMP1 match of Timer C/E. EEV_TX_CMP1 is comparator event filtered by CMP1 window and assign to reset TA1,TB1 output respectively.
- In case comparator event EEV_TX_CMP1 missing, TA.CMP1 match used to reset TA1 output to finish PWM cycle. Master.PRD for TB1 reset known as timeout protect.
- Dual trigger DAC generate sawtooth reference for comparator, called slope compensation to eliminate control loop sub-harmonic oscillation.
- Timer E generate two trigger for DAC. TimerE counter reset event reset DAC to sync sawtooth reference with PWM period. TE.CMP2 step trigger generates requests for incremental DAC value changes. Active comparison value for timerE is automatically updated as soon as a compare match occur.

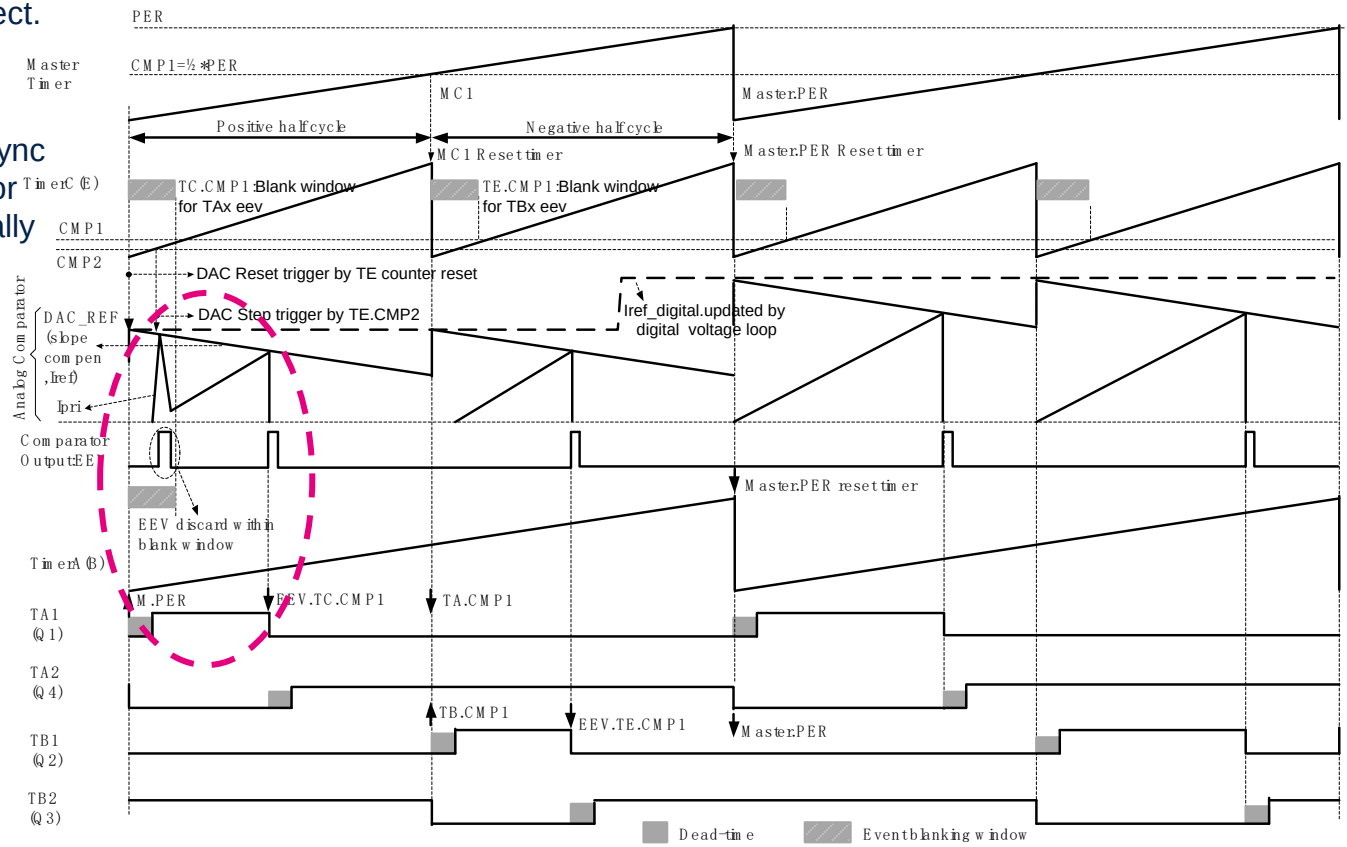
HRTIM configure

	Source	Master timer		TimerA	TimerB		TimerC	TimerE		
		CMP1	Period	CMP1	CMP1	PRD	CMP1_EEV	CMP1_EEV	CMP2	Reset
Destination	Comparator event blank window						√	√		
	TimerA counter reset		√							
	TimerB counter reset		√							
	TimerC counter reset	√	√							
	TimerE counter reset	√	√							
	TA1 output set		√							
	TA1 output reset			√			√			
	TB1 output set				√					
	TB1 output reset		√					√		
	DAC reset trigger									√
	DAC step trigger								√	

Solution benefits to system

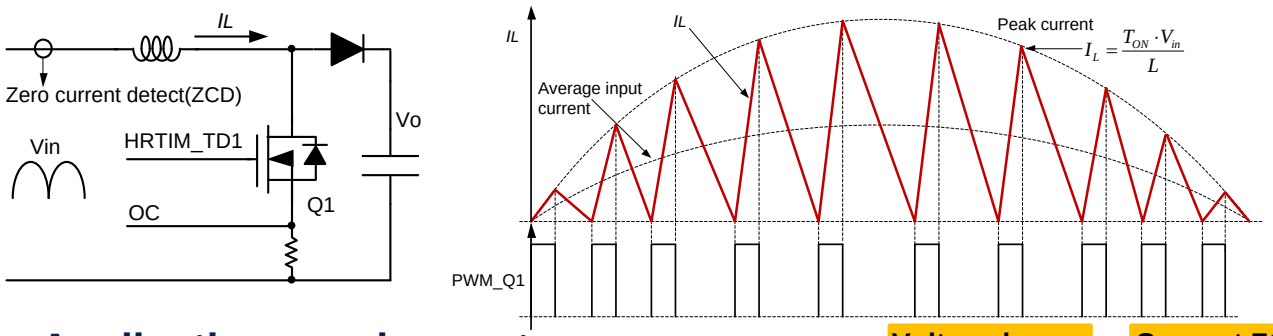
- **No transformer blocking capacitor and cost/size saving**
- **Hardware current loop, no CPU load**
- **Cycle by cycle HW current limit**
- **Faster response**, system degrade to one order

Simplified solution waveform



Scenario 3: Critical conduction mode PFC (CRM): 1MHz switching frequency with GaN

Boost topology & waveform



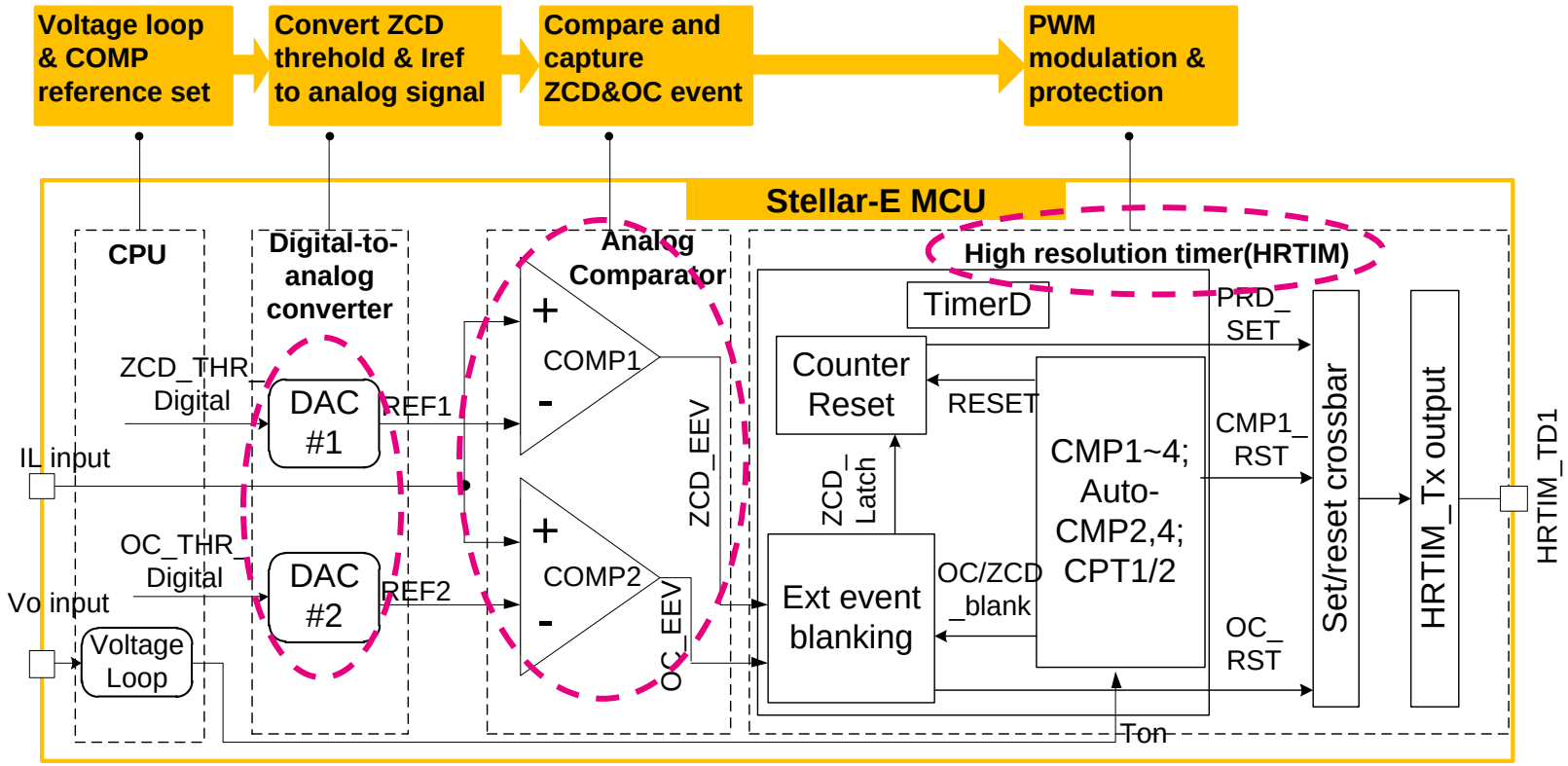
Solution benefits to system

- Up to **1MHz with GaN**,reducing inductor size and BOM cost.
- **HRTIM(HW) control PWM** TON & TOFF, **NO CPU load**
- **Cycle by cycle current limit**, flexible protect (OC or ZCD miss)

Application requirement

1. Constant TON time to build-up inductor current
2. TOFF time managed by inductor current decreased to zero event, controller restart next PWM cycle by inductor current zero crossing detection(ZCD).
3. Cycle by cycle current limit in case over current(OC) happens within TON and PWM recoverable at next cycle.
4. Max TOFF limit in case no zero current detect(ZCD) event to limit minimum PWM frequency
5. Min TOFF time limit in case too early ZCD event to limit maximum PWM frequency

Stellar-E solution block



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CRM PFC with GaN: HRTIM configure summary

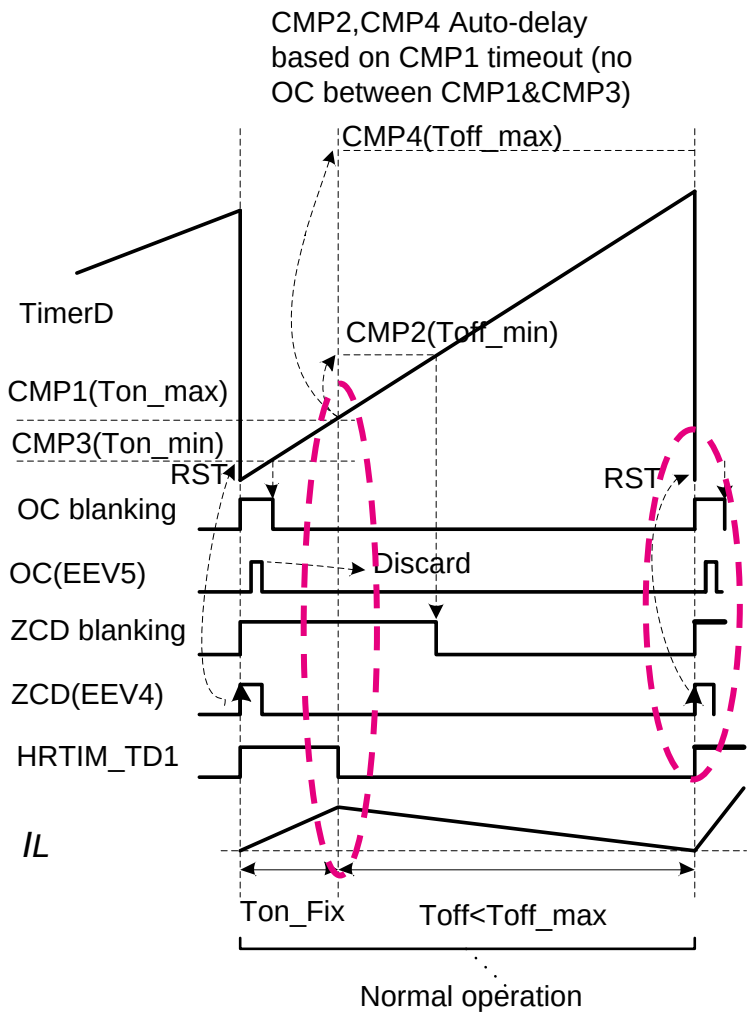
HRTIM configure

Source register/event		TimerD									
		CMP1	CMP2	CMP3	CMP4	Capture1	Capture2	Auto-delay_ CMP2	Auto-delay_ CMP4	OC_EEV_CMP3	ZCD_EEV_CMP 2
Describe	Value	Software				=Counter value at TA1 reset	=Counter value at TA1 reset	=Capture1 +CMP2	=Capture2 +CMP4	\	\
Describe	Active compare register	√	×	√	×			√	√		
Destination	Comparator1 ZCD EEV4 blank window							√			
Destination	Comparator2 OC EEV5 blank window			√							
Destination	TimerD counter reset								√		√
Destination	TD1 output set								√		√
Destination	TD1 output reset	√								√	

Solution analysis:

1. HRTIM_TD1(Q1) output：
   - SET by autodelay.CMP4 or ZCD_EEV_CMP2(ZCD event filtered by autodelay.CMP2)
   - RESET by TD.CMP1(fixed Ton time controlled) or OC_EVT_CMP3(current limit)
2. Timer D counter reset by
   - ZCD.EEV.CMP2
   - autodelay.CMP4 means timeout protect if no ZCD event happens
3. Capture1/2 define TOFF start moment, CMP2,CMP4 define minimum and maximum TOFF.

Simplified solution waveform



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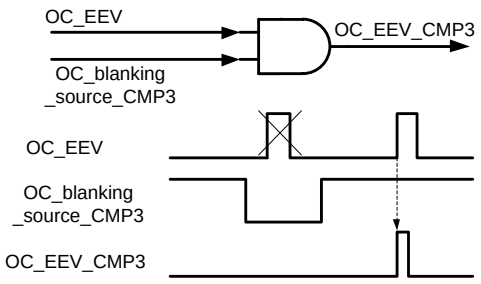
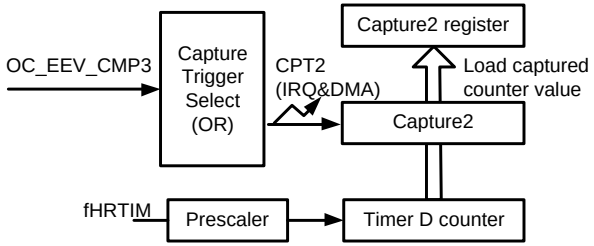
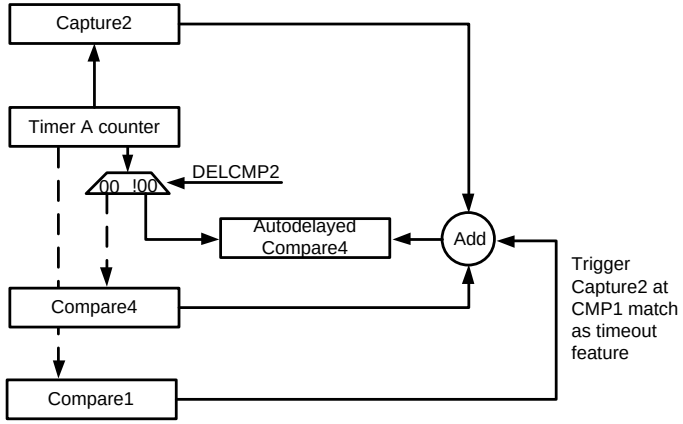
CRM PFC with GaN: Over current and maximum TOFF protect

Event blanking mode

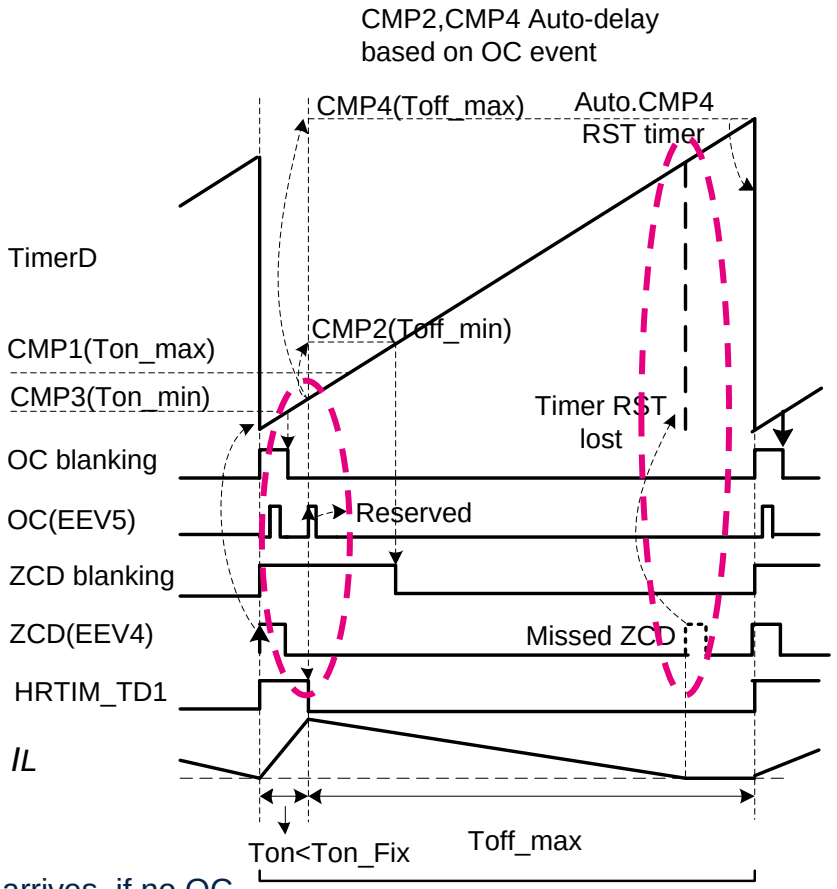


Timing unit capture & auto-delay compare





Simplified solution waveform



Over current, Ton<Ton_fix;
NO ZCD event,
counter reset on autodelay.CMP4

Application requirement

1. Cycle by cycle current limit in case over current(OC) happens within TON and PWM recoverable at next PWM cycle
2. Max TOFF limit in case no zero current detect(ZCD) event to limit minimum PWM frequency

Solution for item1 analysis:

1. Over current (OC) captured by analog comparator as an event used to reset TD1. A blanking window set by TD.CMP3 used to discarded OC event if it's false triggered by diode recovery at PWM cycle start , OC blanking window also is TON_min.

Solution for item2 analysis:

1. Capture2 register load counter value when OC_EEV_CMP3 arrives, if no OC event happens,CMP1 used to trigger capture unit as timeout mechanism.
2. Autodelay.CMP4 updated with value of capture2 adding CMP4. Capture2 value define TOFF start, CMP4 define maximum TOFF interval.
3. Autodelay.CMP4 reset counter in case ZCD event missing(timeout) to clamp minimum PWM frequency.

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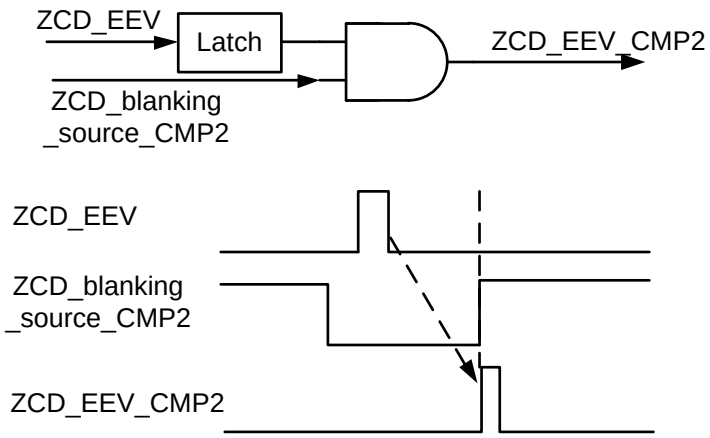
CRM PFC with GaN: Minimum TOFF protect

Event postpone mode

Application requirement

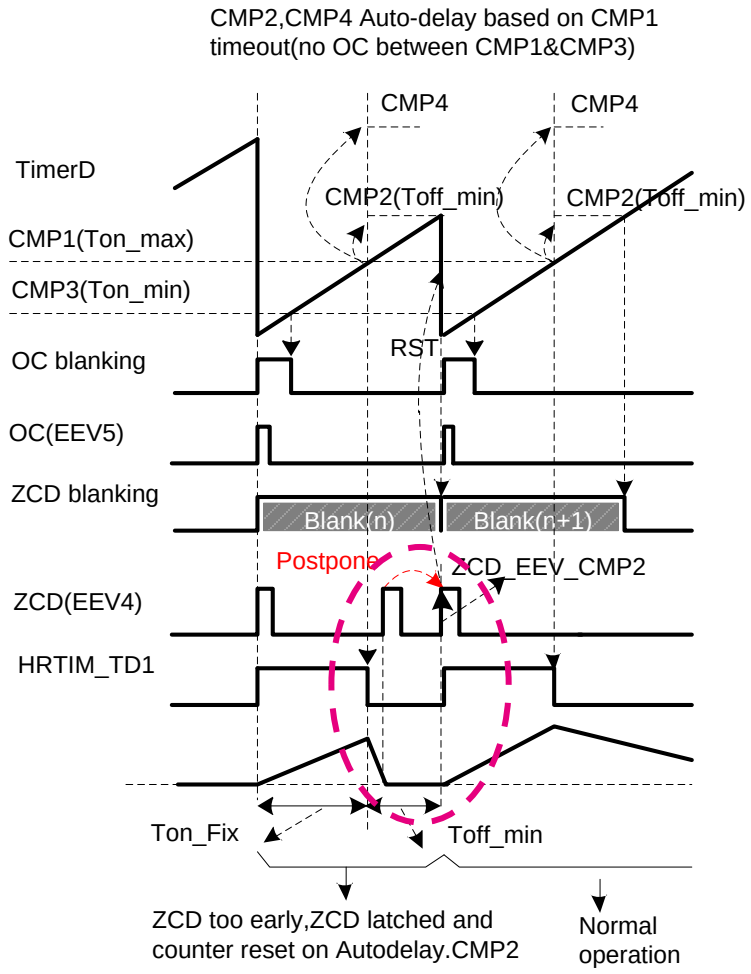
- Min TOFF time limit in case too early ZCD event to limit maximum PWM frequency



Solution analysis

- In case ZCD event arrive too early, a ZCD blanking window defined from timer counter reset to Autodelay.CMP2.
- If ZCD event happens during ZCD blanking window, it will not be discarded and will be latched to end of window as ZCD_EEV_CMP2 and will reset timer counter.
- Autodelay.CMP2 register updated with value of capture1 adding compare2. Capture1 define TOFF start, and CMP2 define minimum TOFF interval. Capture1 triggered by OC_EEV_CMP3 with CMP1 timeout mechanism.

Simplified solution waveform



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ST highlight product for OBC,DCDC

May,2022

STPOWER SiC MOSFET
Positioning vs. product family & focus application

Breakdown Voltage						
650V		750V / 900V	1200V			1700V
Series						
G2	G3	G3	G1	G2	G3	G1
On-state resistance						
18 mOhm to 55 mOhm	14 to 55 mOhm	11 mOhm (750) 12 mOhm (1200)	52 mOhm to 520 mOhm	25 mOhm to 75 mOhm	8 to 69 mOhm	1 Ohm and 65 mOhm
Focus Applications						
OBC & DC-DC Renewable energy Power Supply Industrial drives	Traction OBC & DC-DC High density Power Supply	Traction Inverter OBC & DC-DC High density Power Supply	Photovoltaic Power supply	OBC & DC-DC Inverter Charging stations Industrial drives	Traction Inverter OBC & DC-DC HF Power Supply	DC-DC Power Supply Renewable energy

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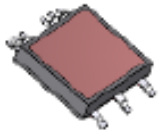
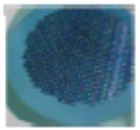
SiC MOSFET Package Roadmap

	PowerFLAT 8x8 STD & DSC	H2PAK-7L	HU3PAK	ACEPAK SMIT	HiP-247 (3 & 4 leads)	STPAK	Bare Dice
Package					 		 
	Surface Mounting				Through-Hole	Special Package Solutions	
Characteristics	▫ Very Thin (< 1mm) ▫ Well accepted in power conversion ▫ Dual side cooling option ▫ Leadless ▫ **Industrial domain**	▫ **AG qualified at 175dC** ▫ Kelvin Source for optimized driving ▫ High runner for Automotive customers	▫ **AG qualified at 175dC** ▫ **Top side cooling** ▫ Kelvin Source for optimized driving ▫ Very good thermal dissipation	▫ **AG qualified at 175dC** ▫ **Isolated Top side cooling** ▫ Suitable for different configurations (HB, Dual die, etc.) ▫ High Power ▫ Modular Approach	▫ **AG qualified at 200dC** ▫ **Very common Industry standard** ▫ Kelvin Source option for optimized driving ▫ High creepage version (1700V) in development	▫ **Unique Solution for traction Inverter** ▫ **AG qualified at 200dC** ▫ **Very High thermal dissipation efficiency** ▫ Sense pin for optimized driving ▫ Multi-sintered package	▫ **WLBI & KGD** ▫ **T&R or RWF options** ▫ **Compliant with the most stringent Automotive Quality Requirements**

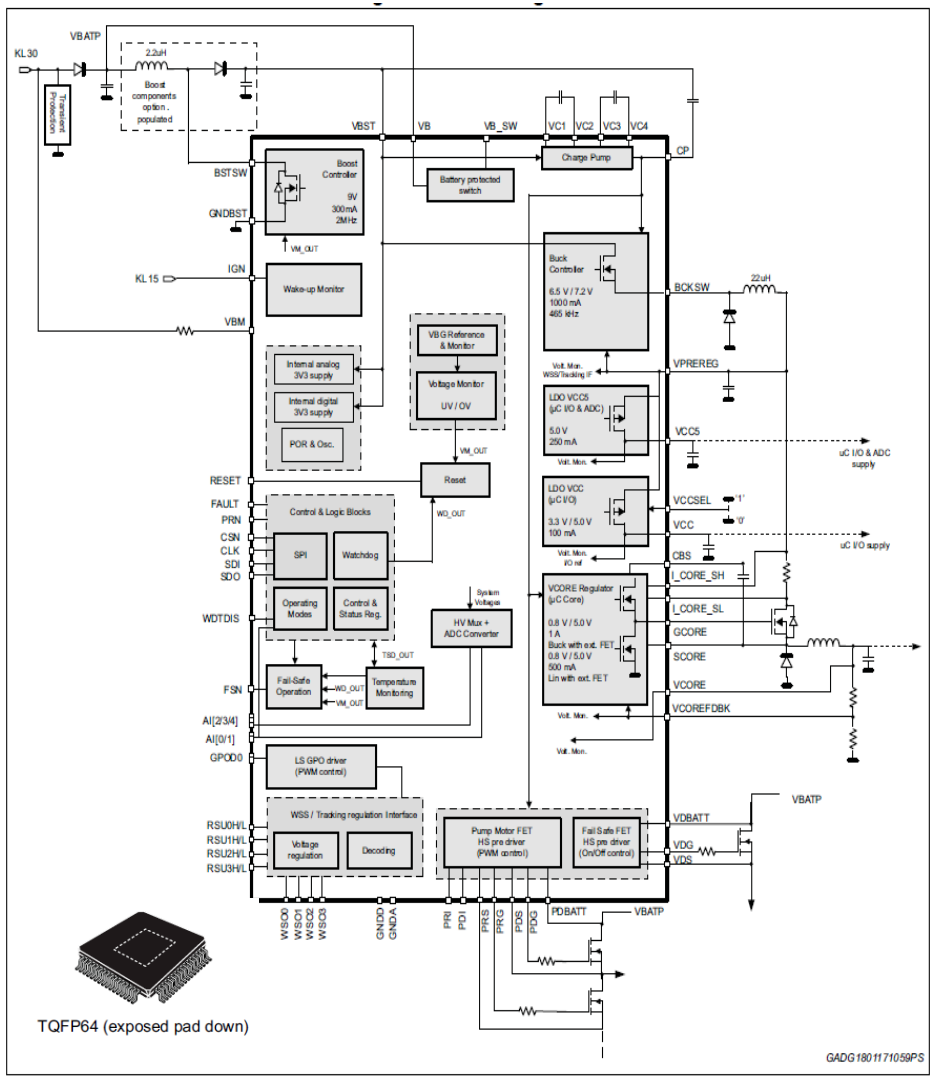
Gen3 SiC MOSFET product Plan 1200V discrete

Part Number	V_{DS} [V]	R_{DS}(on) Typ @ 25ºC [Ω], *Vgs=18V	Package	Eng. Samples	Mat.30
SCT070HU120G3AG	1200	0.070	HU3PAK	Available	Q1 2022
SCT070H120G3AG			H2PAK-7L	Available	Q1 2022
SCT070W120G3AG			HiP247	Available	Q1 2022
SCT070W120G3-4AG			HiP247 4L (LL)	Available	Q2 2022
SCT040HU120G3AG	1200	0.040	HU3PAK	Q1 2022	Q2 2022
SCT040H120G3AG			H2PAK-7L	Q1 2022	Q2 2022
SCT040W120G3AG			HiP247	Q1 2022	Q2 2022
SCT040W120G3-4AG			HiP247 4L (LL)	Q1 2022	Q2 2022
SCT025HU120G3AG	1200	0.027	HU3PAK	Q1 2022	Q2 2022
SCT025H120G3AG			H2PAK-7L	Q1 2022	Q2 2022
SCT025W120G3AG			HiP247	Q1 2022	Q2 2022
SCT025W120G3-4AG			HiP247 4L (LL)	Q1 2022	Q2 2022
SCT020HU120G3AG	1200	0.020	HU3PAK	Available	Q2 2022
SCT020H120G3AG			H2PAK-7L	Available	Q2 2022
SCT016H120G3AG	1200	0.016	H2PAK-7L	Q1 2022	Q1 2022
SCT016HU120G3AG			HU3PAK	Q1 2022	Q2 2022
SCT015W120G3-4AG	1200	0.015	HiP247-4L	Available	Q2 2022

L9396 System Basis Chip

Technical information

- Integrated boost regulator, 9 V, 300 mA, 2 MHz
- Integrated buck pre-regulator, 6.5 V / 7.2 V, 1 A, 465 kHz
- Integrated LDO, 5 V, 250 mA for µC I/O and ADC supply
- Integrated configurable LDO, 3.3 V / 5 V, 100 mA for µC I/O supply
- Configurable and programmable regulator with external FET, 0.8 V to 5 V for µC core supply
  - up to 1 A in buck configuration
  - up to 750 mA in linear configuration
- 2x tracking regulator supply (3.3 V / 5 V, 120mA)
- Configurable and programmable double watchdog (Q&A WD and PRUN WD)
- Fail-Safe Output (FSN) and Configurable Fail-Safe Functionality
- Wake-up input (IGN) (standby current comsumption: 30uA)
- Low-side general purpose output with programmable PWM control (GPO)
- Integrated 10-bit ADC with system diagnostics
- Operating voltage: VBATP: 4.5 V to 19 V with boost; 6 V to 19 V without boost
- ISO 26262 compliant, ready for functional safety application up to ASIL-D



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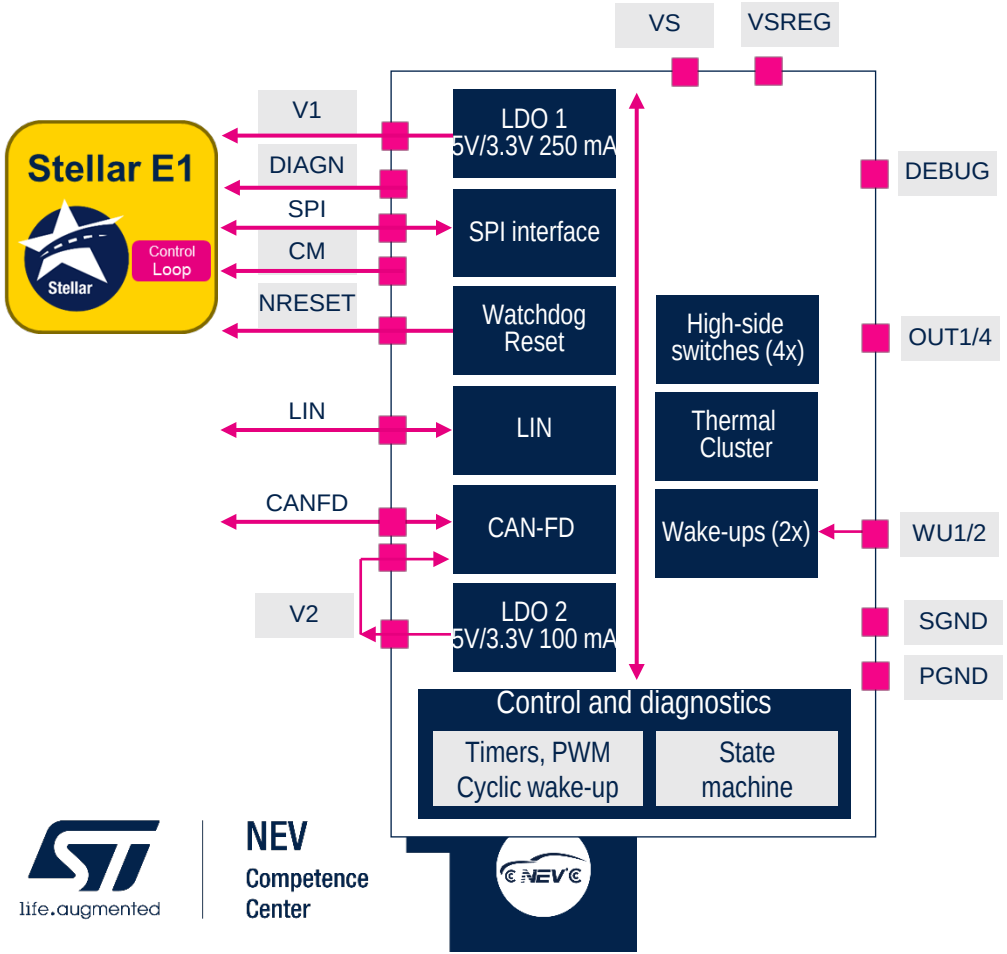
Power management for Stellar E1

Highly integrated and scalable SBC & PMIC for advanced MCUs

SPSB081: SBC with dual configurable LDO, LIN and CAN-FD. Team mating with Stellar E1 to support Electrification



- LDO1 5V/3.3V@250 mA, LDO2 5V/3.3V@100 mA
- Watchdog
- 2xWake up inputs
- Overvoltage detection
- All Outputs Short Circuit protected
- Dedicated diagnostic pin
- Temperature Warning and Thermal Shutdown
- CAN-FD
- LIN (optional)
- SPI for Mode Control and Diagnosis
- Very low Stand-By Current
- Thermal Clusters
- Direct Input
- ASIL-B

QFN32 5x5 WF

ES Available
SOP H2 '22

Fulfilling Stellar family with scalable solutions

SPSA068

- PMIC with 1 Buck (5V, 3V3) @ 1A load current + 1 Vref @ 20mA
- Battery compatible
- Low power mode (<75uA active not switching)
- Internal compensation
- Window WD and Reset
- Voltage and current supervisors, Fault pin
- OTP parameters and SPI
- ASIL-B

QFN32 5x5 WF

ES Q1'23
SOP Q2 '24

L99VR02J

- Configurable LDO, 500mA max out
- Advanced diagnostics, battery compatible
- ASIL-B

PowerSS0-12

ES Available
SOP Q4'22

SPSB110
SPSB083

Under definition

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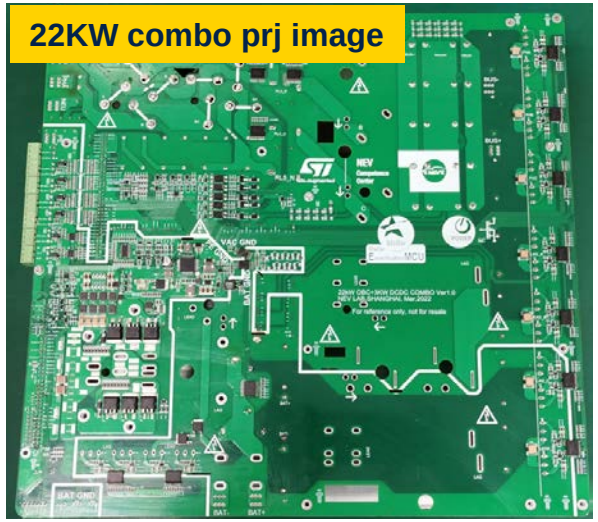
22kw obc+3kw dcdc combo system solution introduce

Sep,2022

22kW OBC+DCDC Combo prj summary & schedule

22KW combo prj image



Main target

- System Validation Stellar-E MCU，Gen3 SiC MOSFET:
  - Faster control frequency to best leverage SiC performance
  - Strengthen analog capability for cycle by cycle PWM control and protect
  - Function safety validation for AUX DCDC(ASIL-C)
- Offering system solution shorten customer evaluating time.
- Customization support at system level

Solution output profile:

- System design analysis
- System test report(data,waveform)
- Application note (hardware, software, safety design detail explain)
- Model base develop training document
- EVM kit schematic/pcb source file

Combo project main schedule(Y2022)

WK26: First prototype PCB ready

WK34: 3ph PFC basic function
- 800V DC,22kW output

WK42: 3kW DCDC basic function
- 12V/220A output
- Peak current mode control

WK49: 22kW CLLC basic function
- 800V DC,22kw output
- Voltage/current closed loop

WK52

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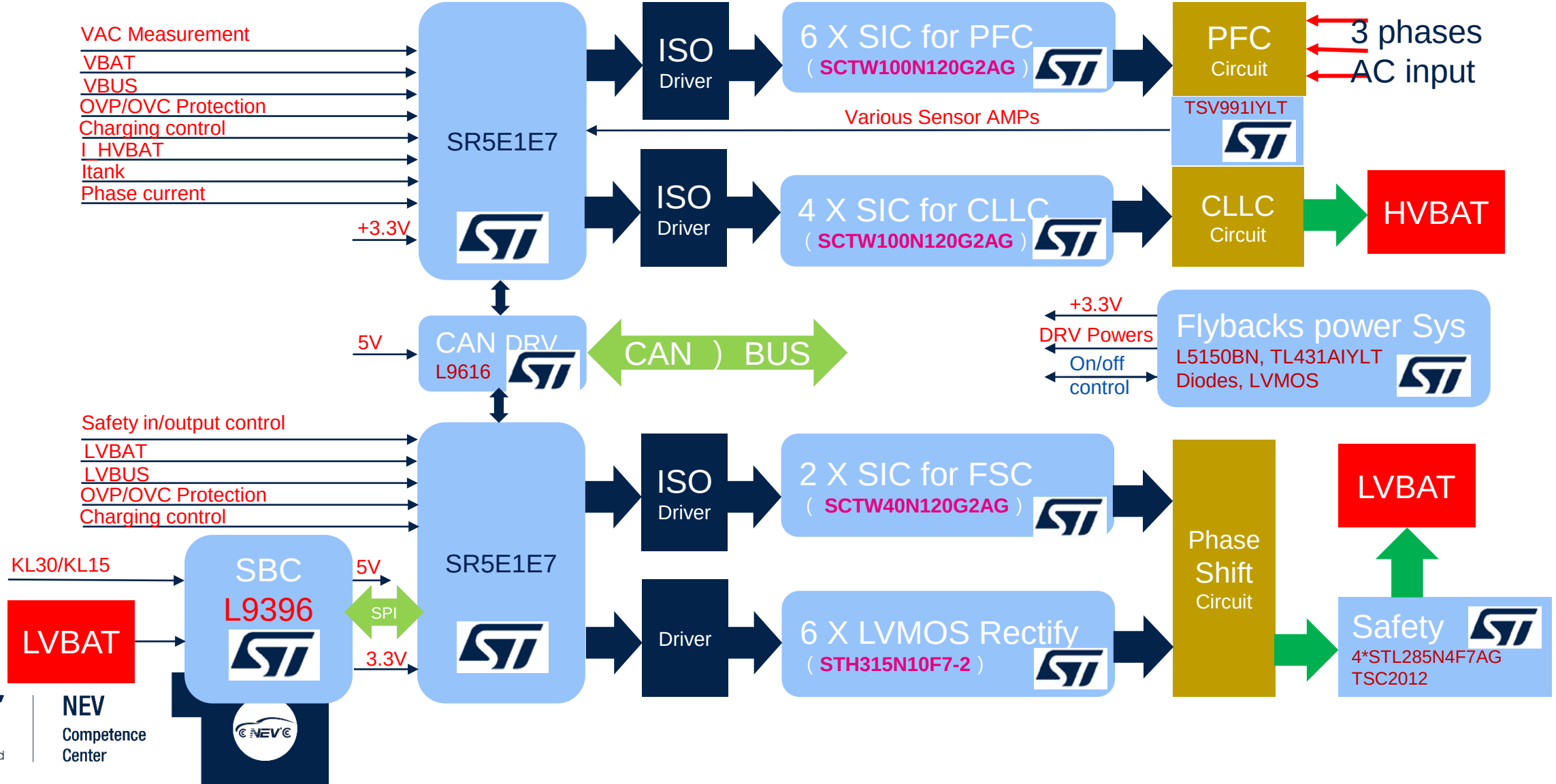
22kw OBC+DCDC combo solution structure -Stellar-E MCU+1200V SiC MOSFET



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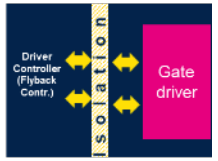
22kW OBC combo solution highlight benefits

developing

Stellar

STPOWER



Name	Part number
Microcontroller	• SR5E1E7
1200V SiC (Gen3 pending)	• SCTW100N120NG2AG • SCTW40N120G2VAG
LV MOSFET	• STH315N10F7
SBC	• L9396 • STPM066
Analog	• TSV791IYLT • TSV911IYLT • TSC2011IYDT

Technical highlights

- Stellar-E MCU digital control to best leverage SiC/GaN
- Full SiC MOSFET with 800V and efficiency optimized
- Synchronization rectification solution for CLLC
- Peak current mode control solution for AUX DCDC(PSFB)
- One MCU platform to handle power loop and vehicle control (OTA,ASIL-D,CAN-FD, AUTOSAR)

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22kw OBC+3kw DCDC power stage spec

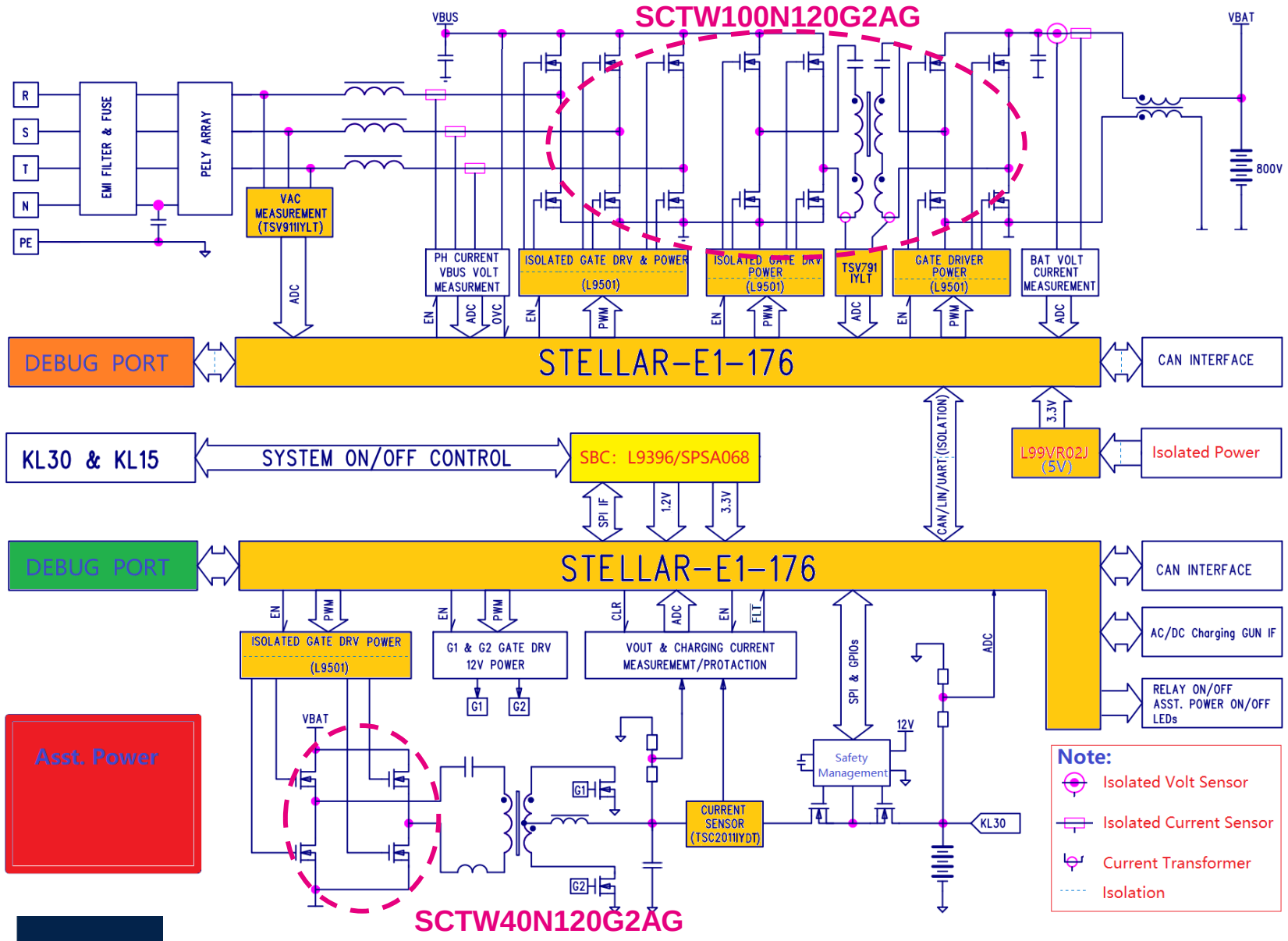
- **3ph 22KW OBC spec**

Parameter	3phase AC input charging
Input Voltage	304Vac~456Vac, @380V,50Hz
Output voltage	450-900V DC →450-900V @800V battery
Output power	→22kW 36A max @800V
DC bus voltage	650-900V DC
Switching frequency, PFC/CLLC	50kHz/200kHz
Communication	CAN/CAN-FD
Housing	Water cooling

- **3KW DCDC spec**

Parameter	Value
Input Voltage	450-900V DC@800V
Output voltage	9-16V @14V
Output power	3kW
Power stage frequency	100kHz
Output ripple	<280mV@full power
Communication	CAN/CAN-FD
Housing	Water cooling

22kw OBC+DCDC combo power topology -Stellar-E MCU+1200V SiC MOSFET



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ST highlight component in 22kW combo platform

developing

Stellar

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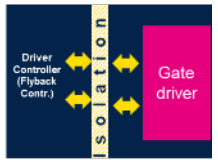
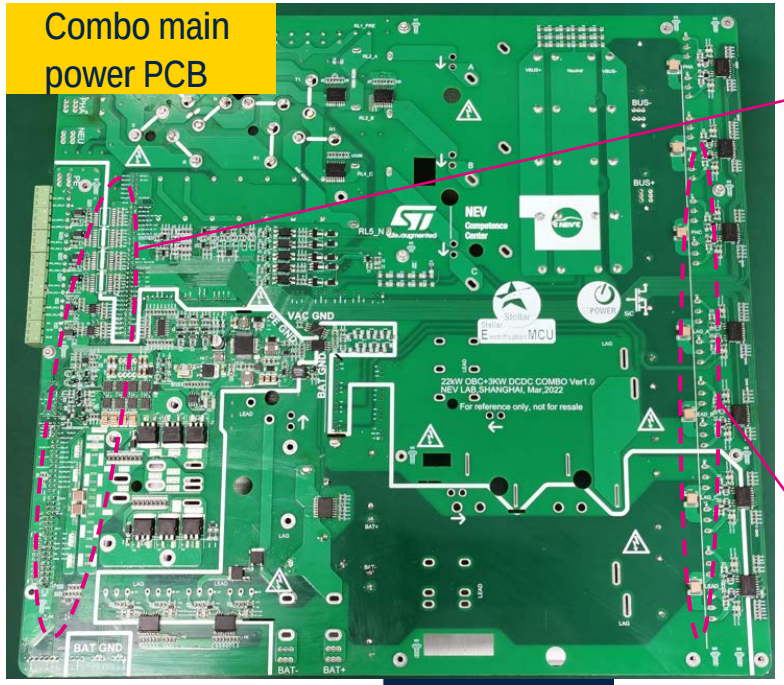
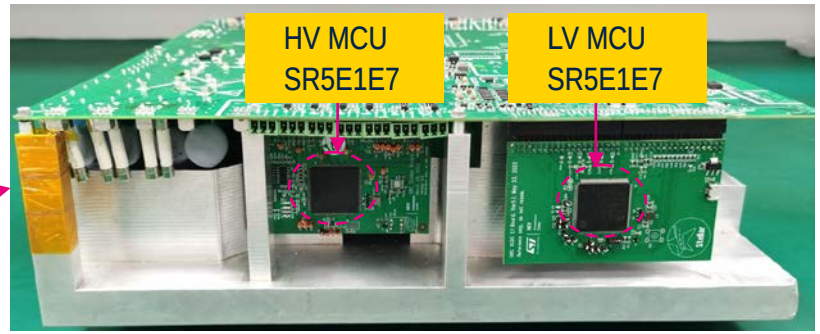
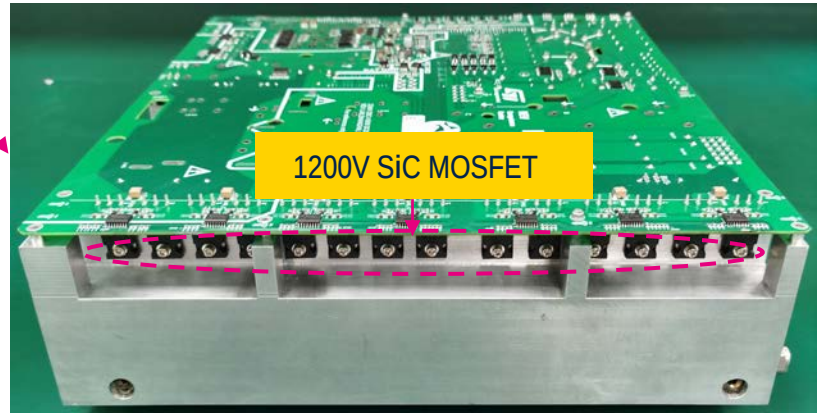
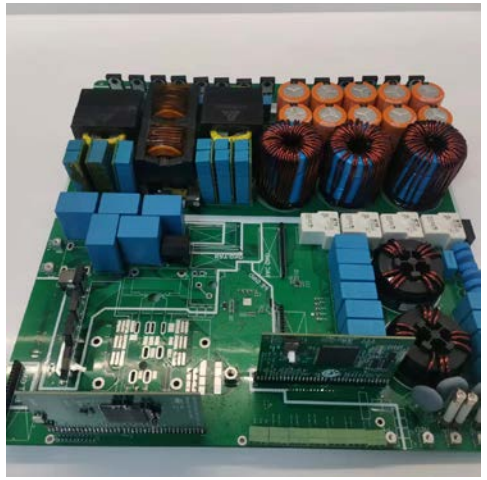








Name	Part number
Microcontroller	• SR5E1E7
1200V SiC (GEN3 pending for test)	• SCTW100N120NG2AG • SCTW40N120G2VAG
LV MOSFET	• STH315N10F7
SBC	• L9396 • STPM066
Analog	• TSV791IYLT • TSV911IYLT • TSC2011IYDT



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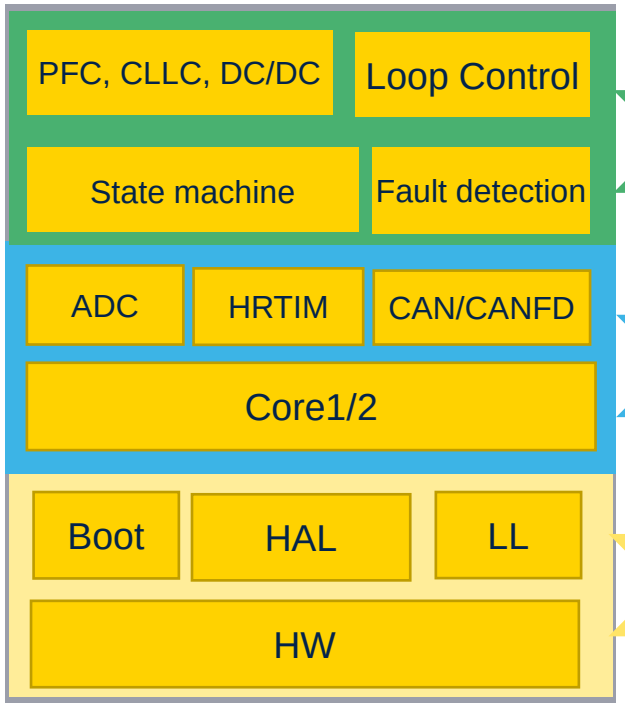
22kW Combo system SW structure



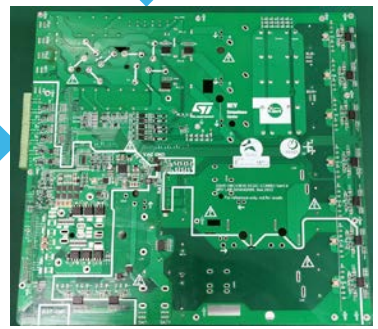
Application
- MIL Test
- Loop control design
- State machine

Peripheral drive
- ADC sampling
- HRTIM PWM
- CANFD communication

Stellar Studio / SDK
- Code integration and compilation

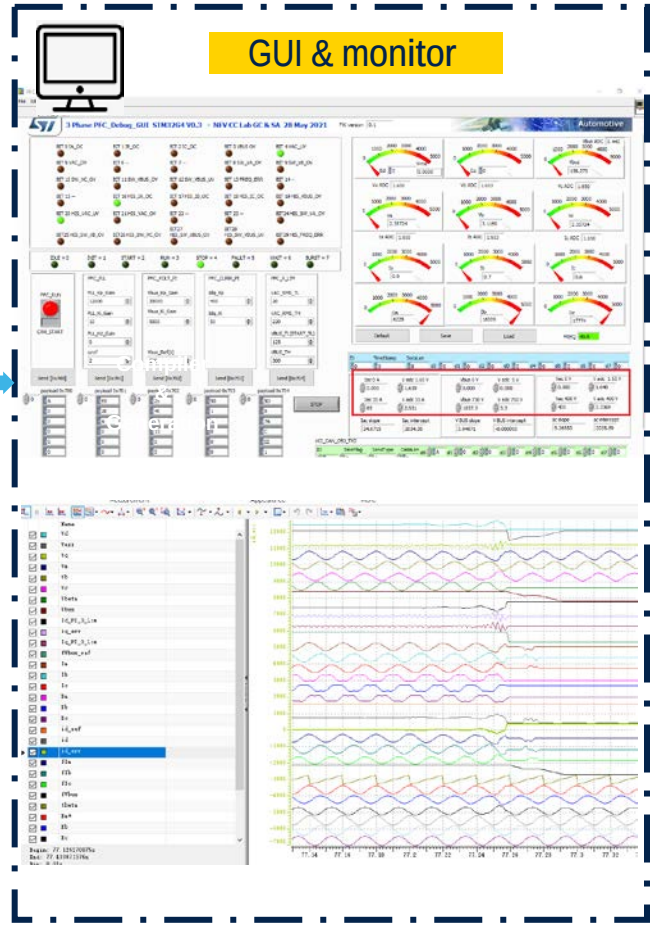
- Model-Based Design
- V model process
- PFC, CLLC,DC/DC Applications
- Multicore
- Docs & Quality

Program Download



CAN/CANFD

GUI
- Status monitor
- System configuration



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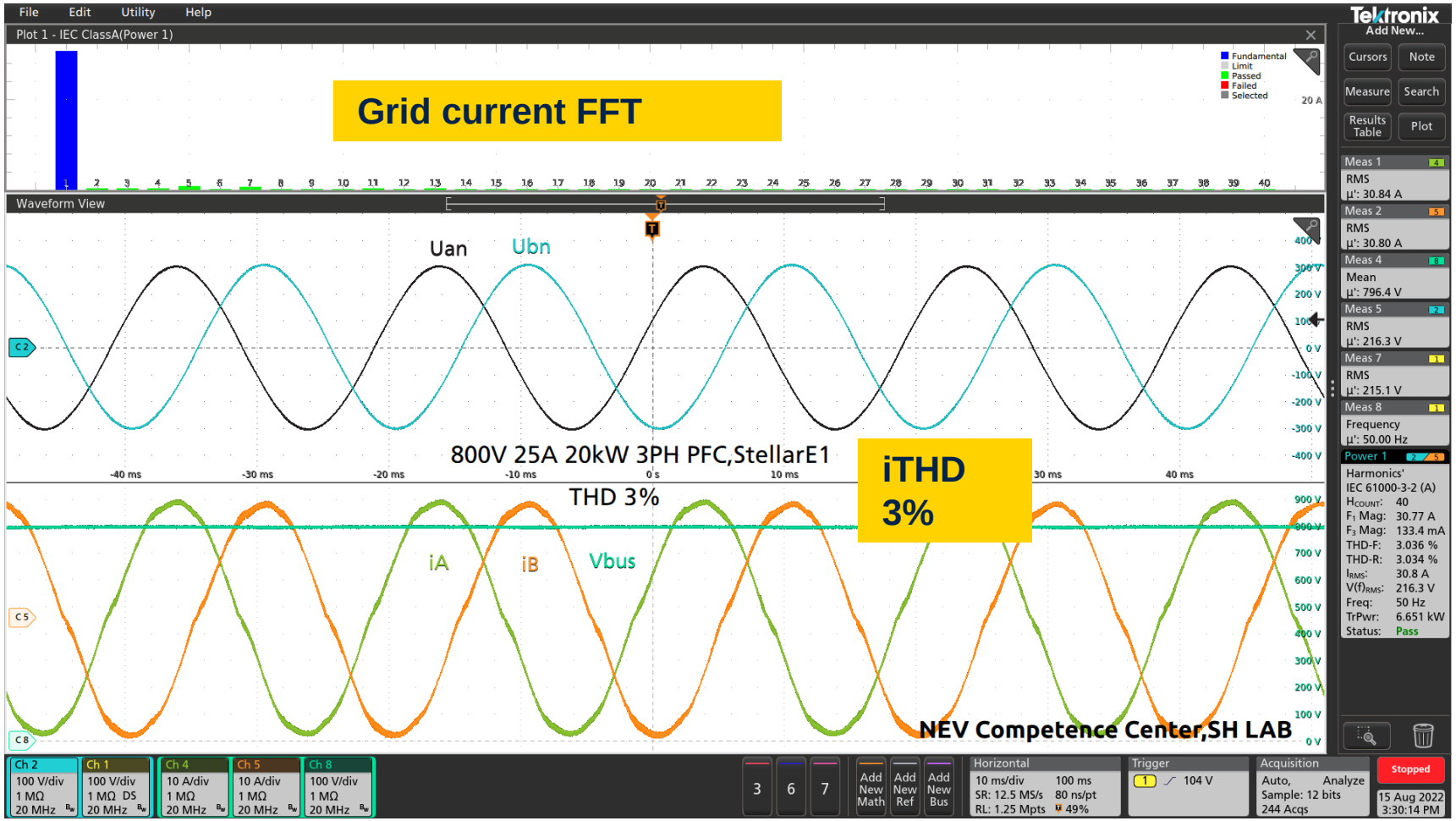
3ph PFC full power running

- Input:380VAC(L-L),32A RMS
- Output:800VDC,25A,20KW
- **Ithd:3%**
- Control loop : every cycle(50kHz)
- SiC water cooling, PFC inductor force air,ambient temp 25℃，water temp 21℃



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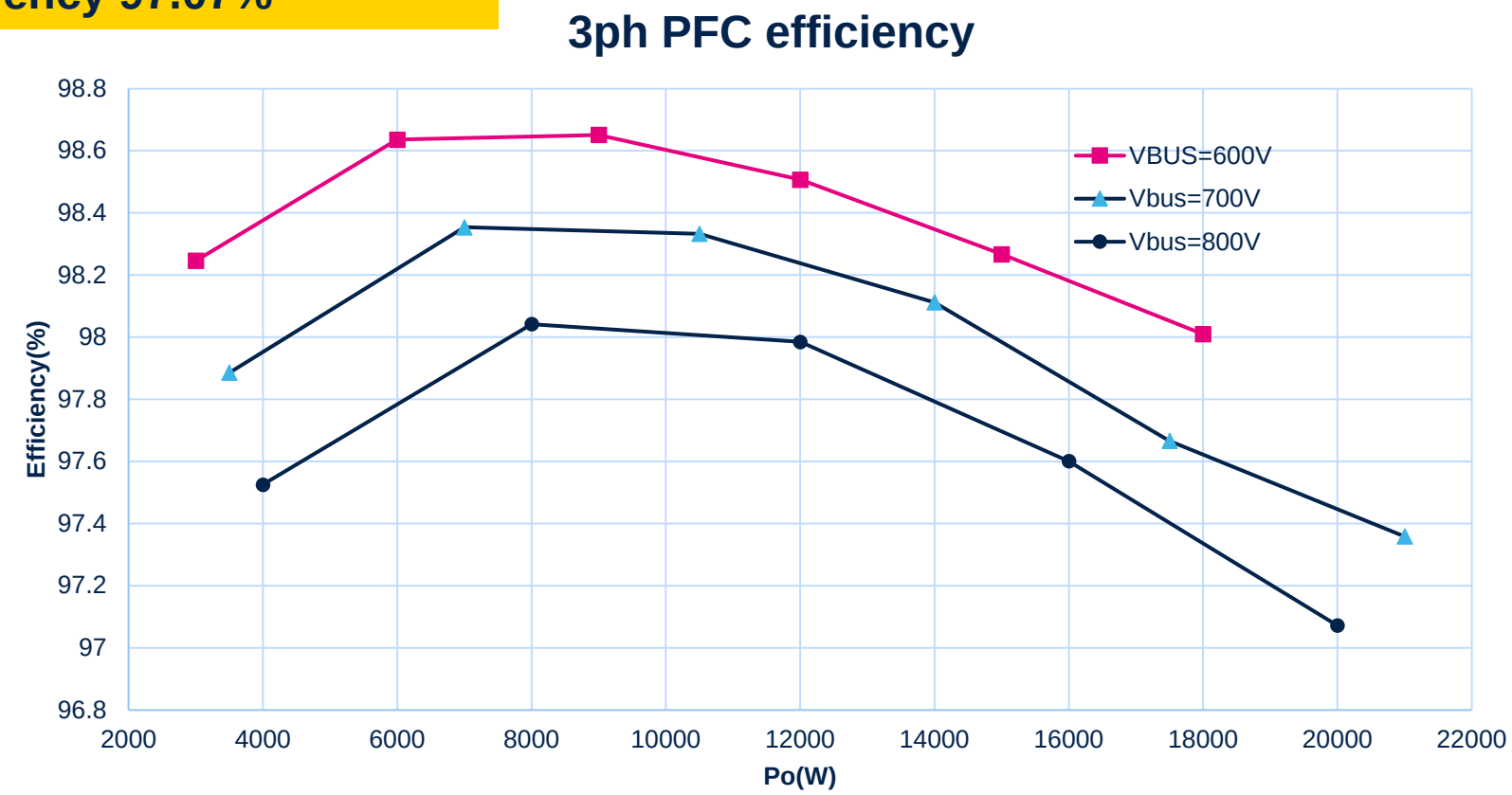
3ph PFC efficiency

- **Peak efficiency 98.63%**
- **800V/20KW full load efficiency 97.07%**

- Peak efficiency:98.63%
- Input:380VAC(L-L)
- Switching frequency:50kHz
- Topology:2 level PWM rectifier(B6)
- Dead-time:300ns
- Rgon=5.1R,Rgoff=6.8R
- Chroma power resistor load and WT5000 power analyzer
- Bias power not included



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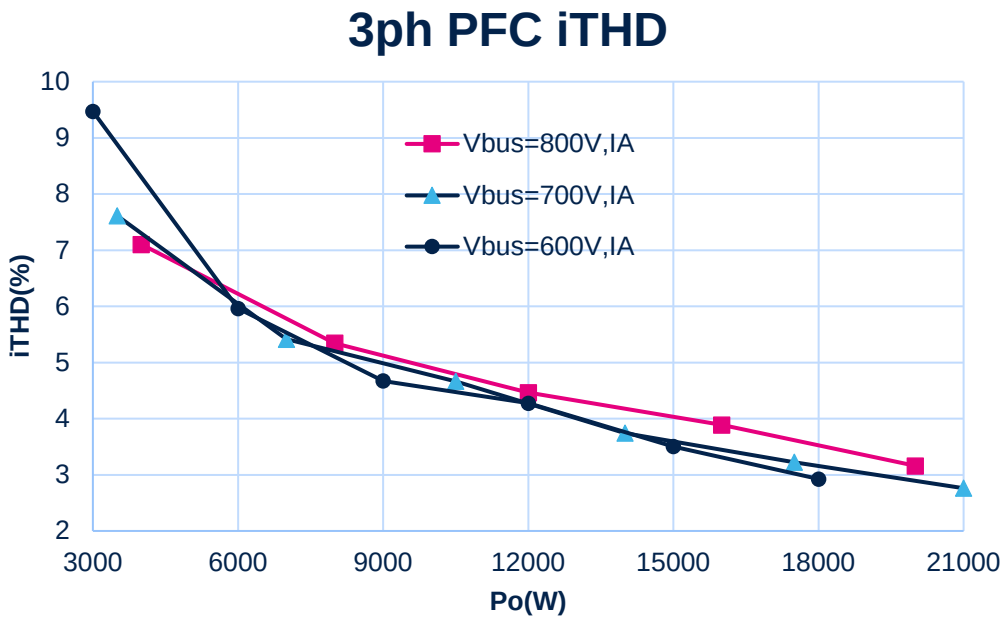
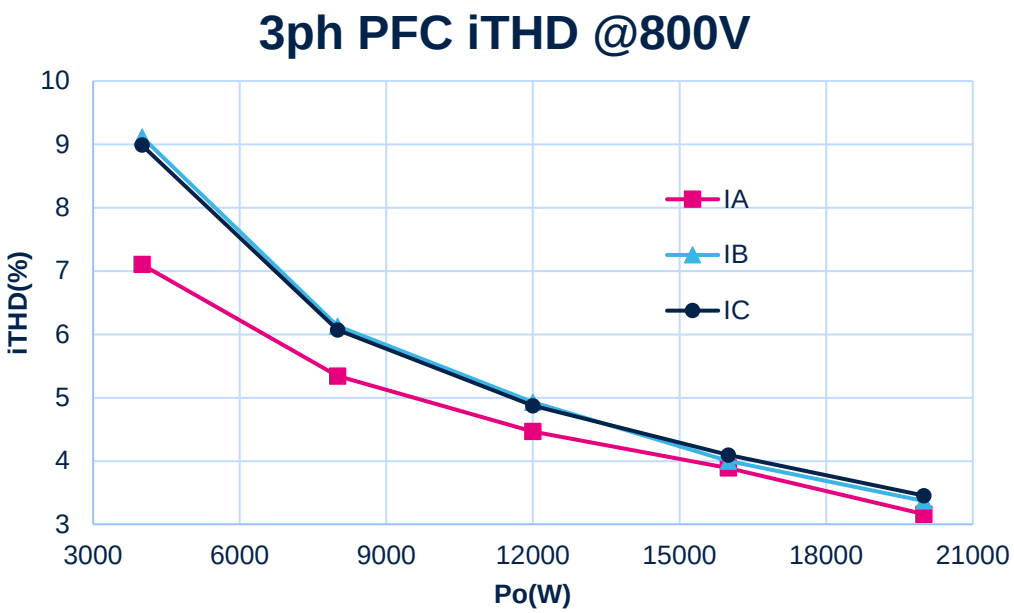
3ph PFC THD(%) data

- **Full load iTHD 2.76% @700V/30A (requirement <5% ?)**
- **Three phase iTHD good consistency**





- Input:380VAC(L-L)
- Current loop execute : cycle by cycle(50kHz)
- Switching frequency:50kHz
- Dead-time:300ns
- Chroma power resistor load 63224E and power analyzer WT5000

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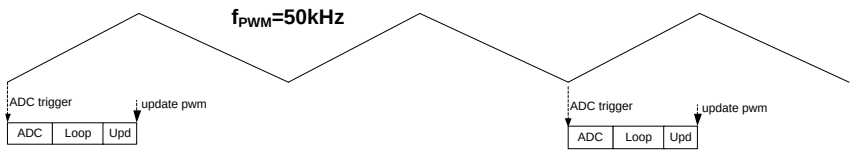
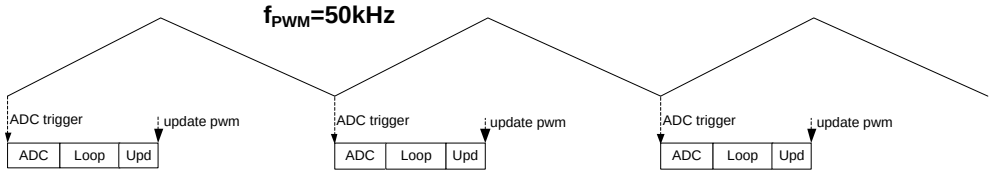
iTHD optimized with cycle by cycle(CBC) control loop updating

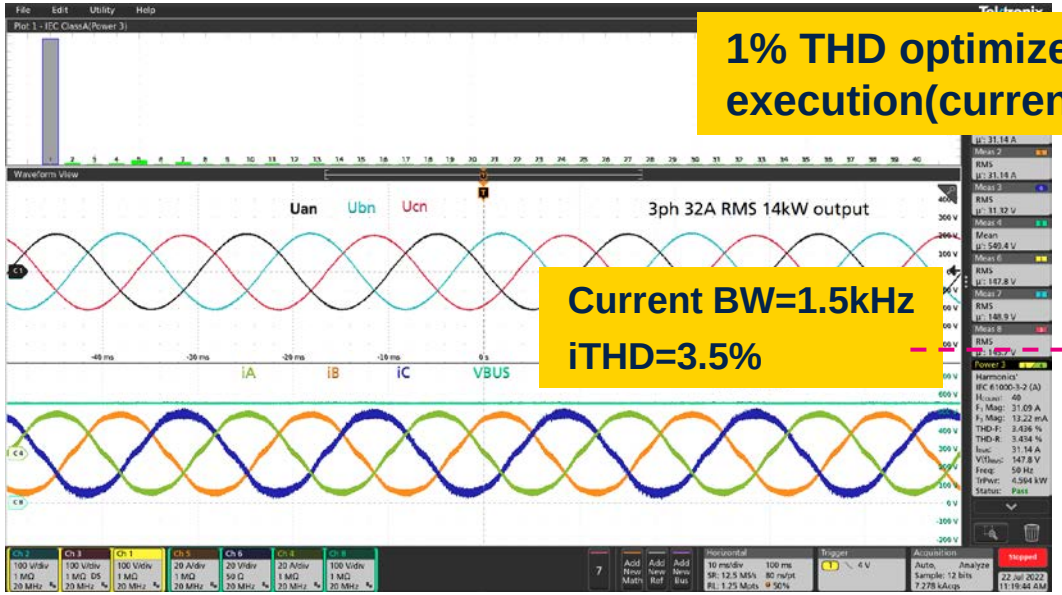
Control loop updating every two PWM cycle



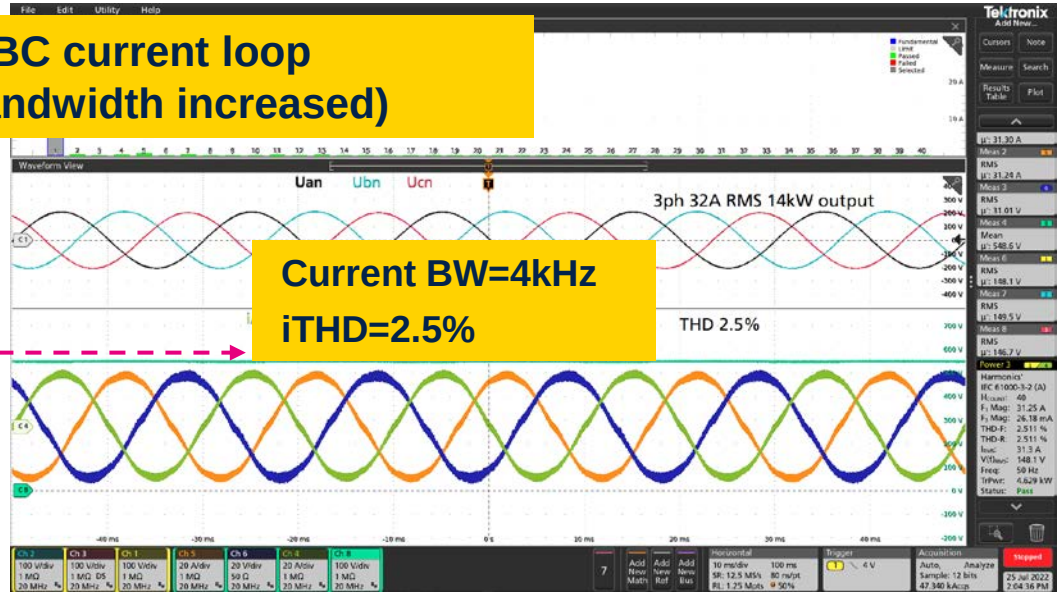
Control loop updating every PWM cycle



1% THD optimized with CBC current loop execution(current loop bandwidth increased)



Current BW=1.5kHz
iTHD=3.5%



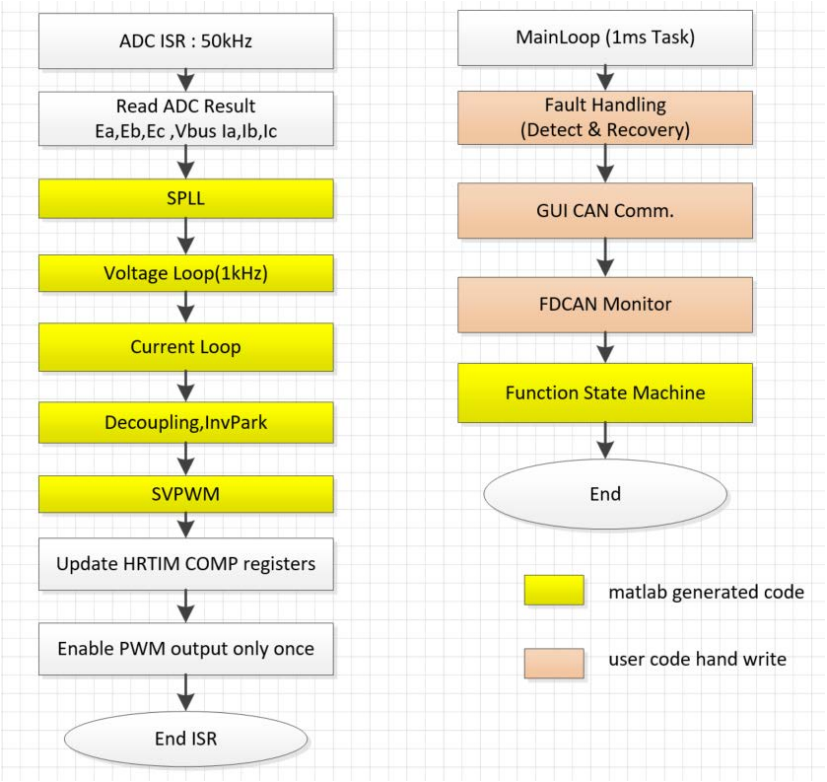
Current BW=4kHz
iTHD=2.5%

Control loop execution time with Stellar-E

- **current loop execute at 50kHz(CBC) and total execution time 6.1us,very low CPU load**
- **yellow part is Simulink(MATLAB) generated loop control and state machine code**

Task Name		Execution Frequency	Execution time	Function
	Voltage loop	1KHz	1.58us	Voltage loop control
VSR_Code_G()	**PLL**	50KHz	**6.13us**	Electric angle calculation
	Current loop	50KHz		DQ axis current loop control
	DQ axis	50KHz		DQ axis current decoupling
	Coordinate transformation and SVPWM	50KHz		Include Clark, Park, Inv-Clark, Inv-Park transformation and SVPWM function
pfc_mainState()		1KHz	690ns	System state machine
MainLp_Cali_PFC_CAN_Task()		1KHz	2.08us	GUI calibration
MainLp_ECU_CAN_Task()		1KHz	16us	Display system variables curve
PFC_FaultCheck()		1KHz	1.18us	System fault check and recovery

ADC ISR and main loop SW task



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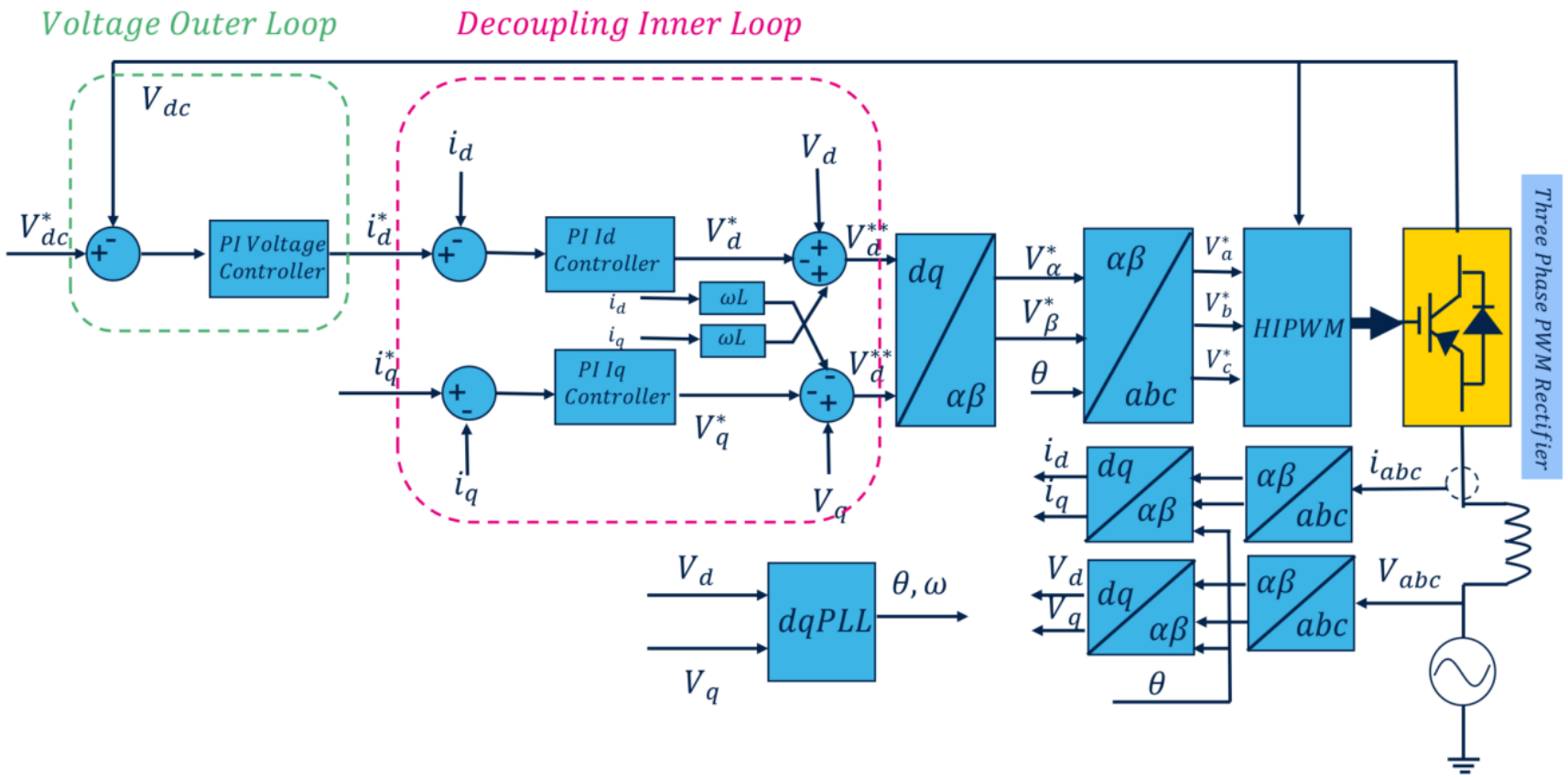
Voltage-oriented Vector Control Diagram Block

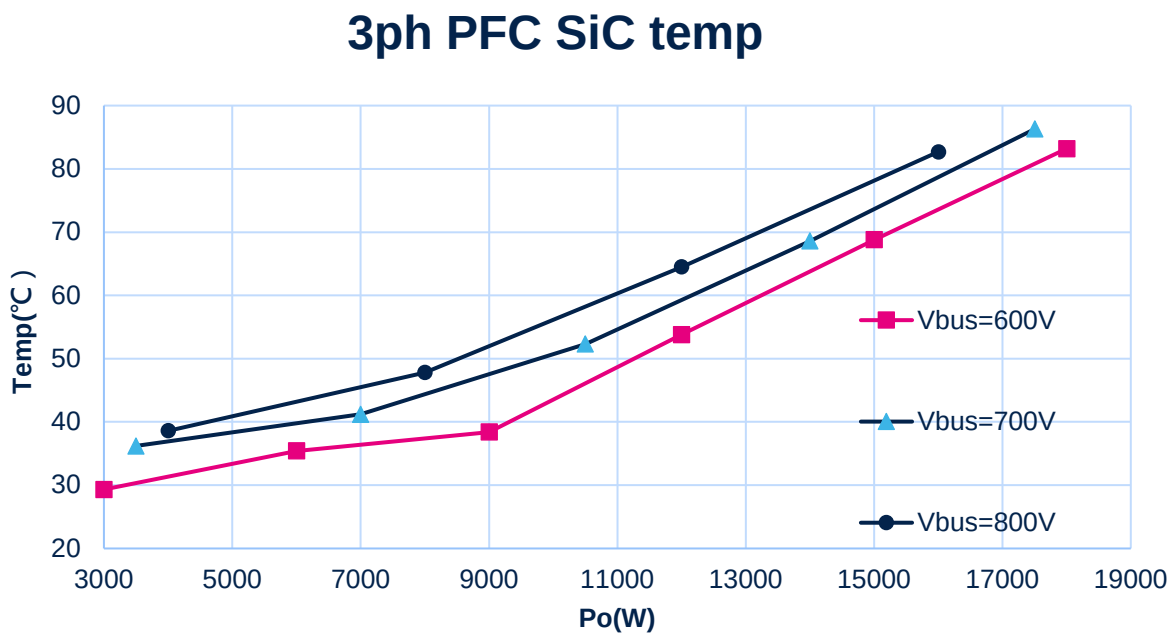
- Current decoupling inner loop and voltage outer loop control
- dqPLL electric angle and frequency calculation
- Harmonic injection pulse width modulation
- Notch filter for bus voltage sampling

PFC Voltage-oriented vector control strategy

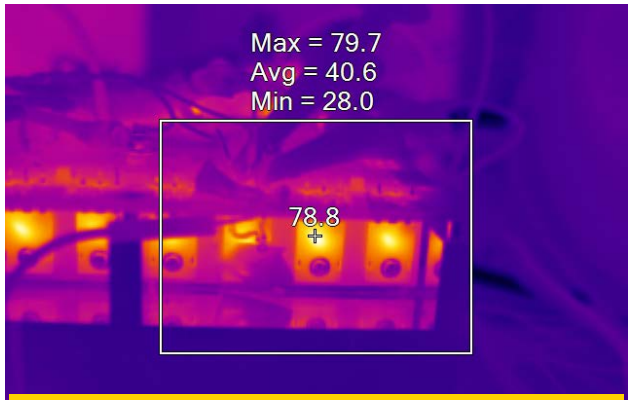


System thermal stress

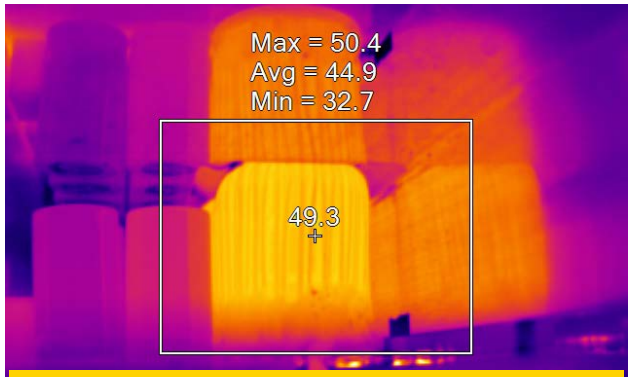
- **Higher bus voltage, SiC thermal stress is worse**
- **30mOhm,1200V SiC @40kHz suggested for 22kW 3ph PFC**



- SiC water cooling, PFC inductor force air,ambient temp 25℃，water temp 21℃
- Input:380VAC(L-L)
- Switching frequency:50kHz
- Dead-time:300ns
- Rgon=5.1R,Rgoff=6.8R



800V,16ADC 3ph PFC SiC thermal image



800V,16A 3ph PFC main inductor thermal image

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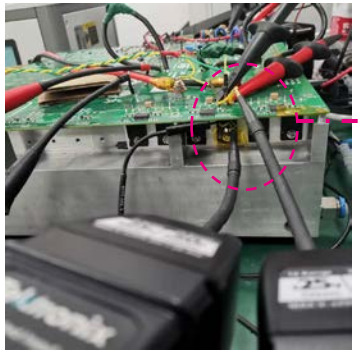
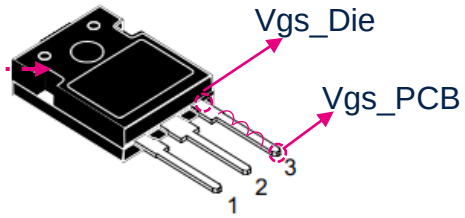
#1 3ph PFC SiC driver-source inductor effect



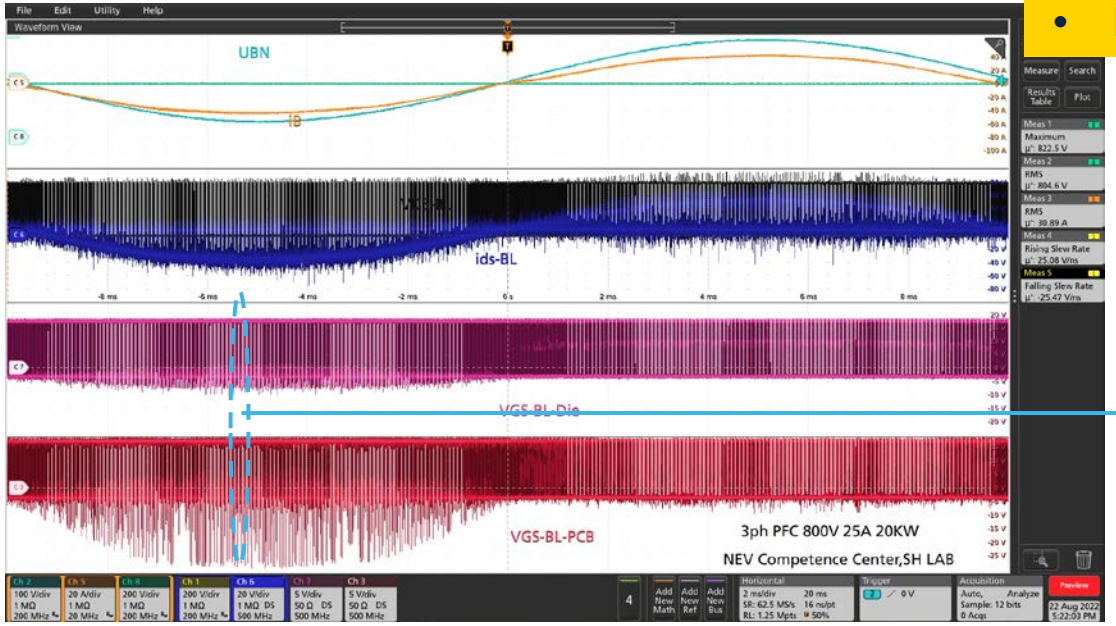


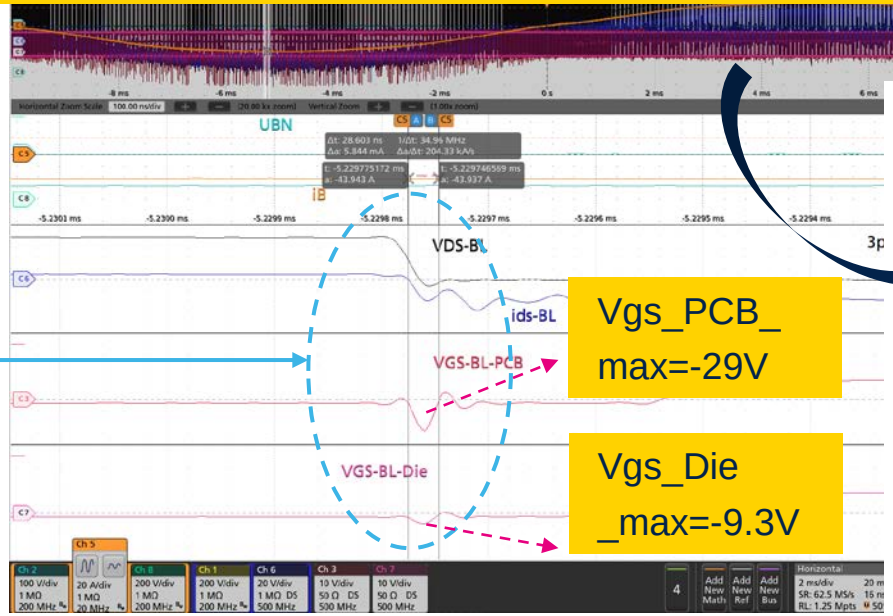
HiP247

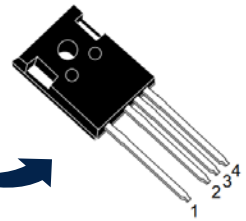
SiC test probe position	Vgs glitch voltage maximum	Vgs glitch voltage duration
Vgs_die	**-9.3V**	28.6ns
Vgs_PCB	**-28.7V**	28.6ns

- Input:380VAC(L-L),32A RMS
- Output:800VDC,25A,20KW
- Rgon=5.1R,Rgoff=6.8R
- Vgon=17.8V,Vgoff=-3.6V
- Grid current negative cycle, Vgs glitch cause by opposite SiC turn off

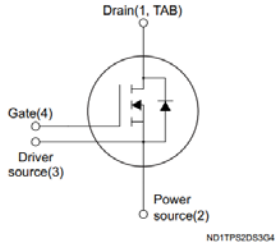
- **Source parasitic inductor involve Vgs glitch with high di/dt**
- **Miller capacitor involve Vgs glitch with high dv/dt**







HiP247-4



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Thank you

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