Highly Integrated USB PD Type-C Controller for SMPS

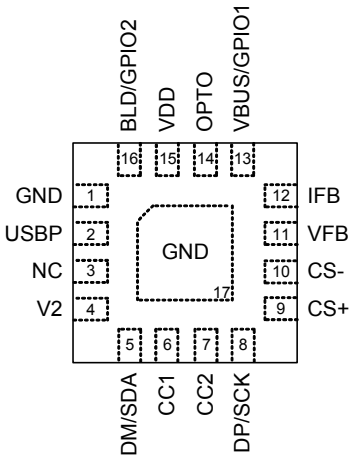
General Description

The RT7202KJ is a simple and yet flexible for multipurpose of USB PD controller. By programming, it could operate as a source or a sink.

When used as a source, it could be used in an off-line AC-DC converter, as it integrates shun regulator, constant voltage (CV) and constant current (CC) control loop with programmable reference voltage to meet the specification of Programmable Power Supply (PPS) specification. When combined with external buck or buck boost controller, it could constitute a DC-DC converter, such as a car charger, and could also meet the PPS specification. When used as a sink, it is simple, low cost, yet flexible to use to request required power from a source. If using the RT7202KJ for a sink design, it has I^2C interface and two GPIOs for flexible use and could be easily controlled by other MCU which plays a master role.

Pin Configuration

(TOP VIEW)



WQFN-16L 4x4

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

- **Protocols Supported**
  - **USB PD 2.0 and 3.0 (PPS)**
  - **Other Proprietary Protocols**
- **Highly Integrated**
  - **Embedded MCU with an Mask-ROM of 24kB, an OTP-ROM of 16kB, and an SRAM of 2kB**
  - **Embedded BMC Transceiver**
  - **Wide V_{DD} Operation Range : 3V to 22V**
  - **Built-in Shut Regulator for Constant-Voltage and Constant-Current Regulation**
  - **Built-in 10-bit Analog-to-Digital Converter (ADC)**
  - **Programmable Cable Compensation**
  - **BLD Pin for Quick Discharge of Output Capacitor**
  - **USBP Pin for Direct Drive of External Blocking N-MOSFET**
  - **Power-Saving Mode in Standby Mode**
- **Protection**
  - **Adaptive Over-Voltage Protection**
  - **Adaptive Under-Voltage Protection**
  - **Firmware-Programmable Over-Current Protection**

Applications

- USB PD Type-C Chargers/Adapters for Smart Phones, NBs, Tablets and All Other Electronics
- USB PD Extension Cores with Offline AC-DC Converters

Ordering Information

RT7202KJ □□-□

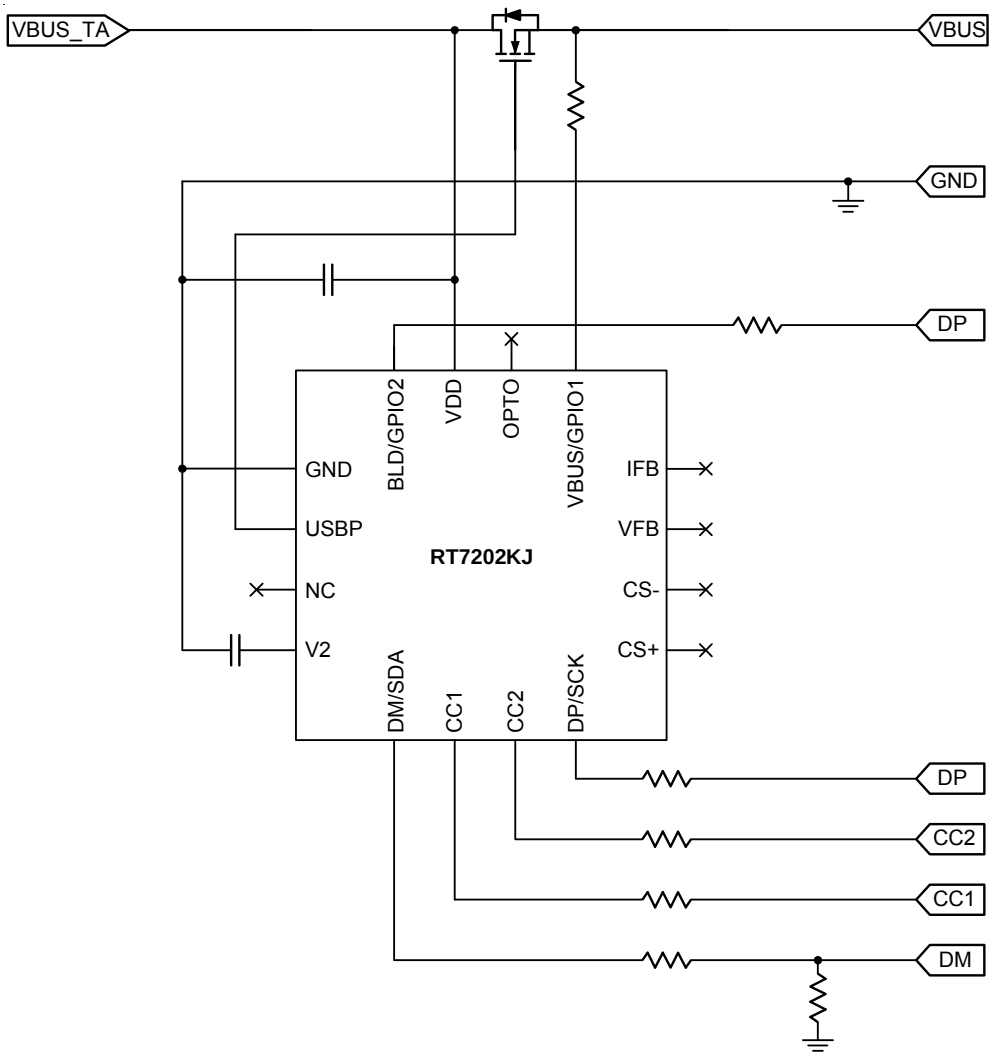
- Programmed Firmware Code AABBX
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- Package Type
  - QW : WQFN-16L 4x4 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

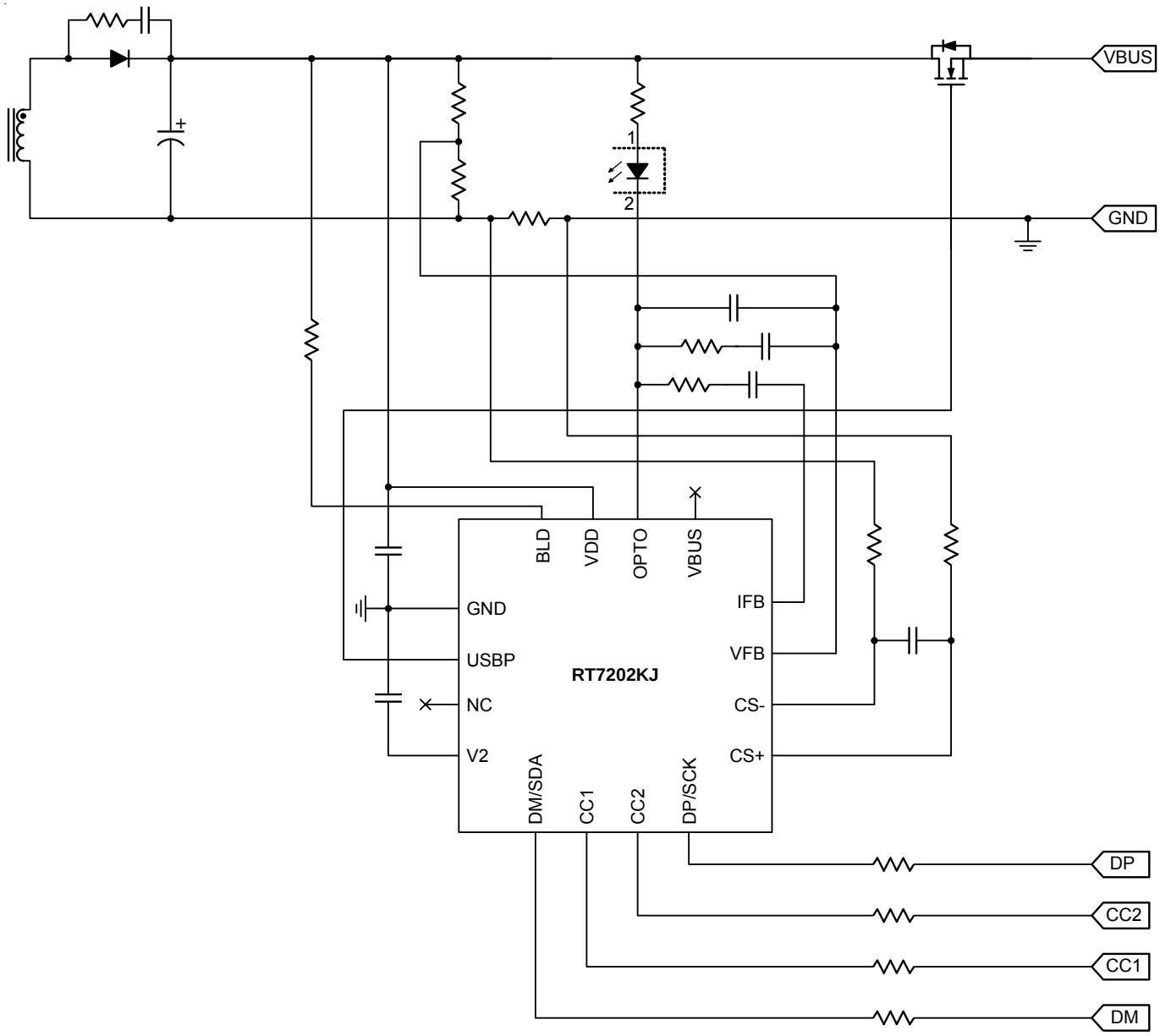
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Simplified Application Circuit



RT7202KJ Simplified Application Circuit for Sink Side



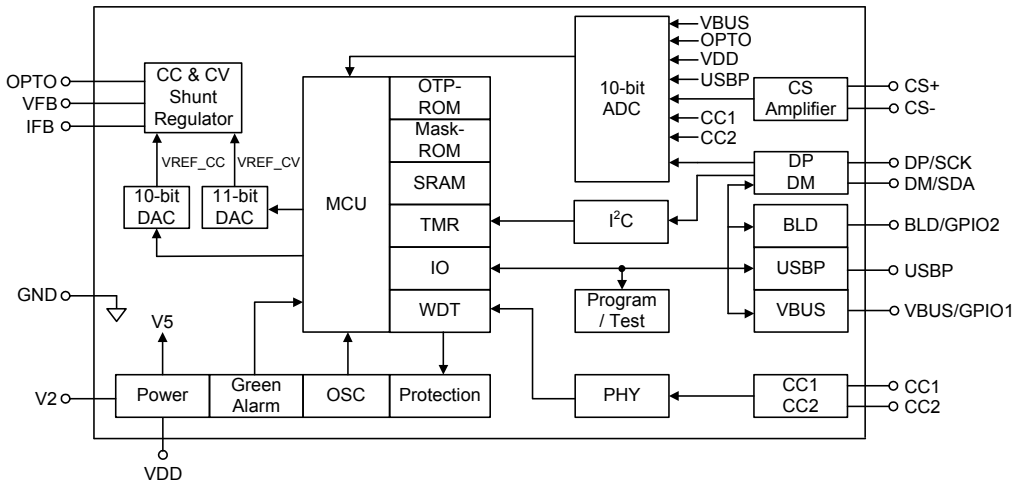
RT7202KJ Simplified Application Circuit for Source Side

Functional Pin Description

RT7202KJ

Pin No.	Pin Name	Type	Pin Function
1, 17 (Exposed Pad)	GND	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	USBP	D IO	Control signal of the blocking N-MOSFET.
3	NC	--	No internal connection.
4	V2	PWR	Regulated DC bias to supply for the MCU.
5	DM/SDA	A/D IO	USB DM channel.
6	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
7	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
8	DP/SCK	A/D IO	USB DP channel.
9	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
10	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
11	VFB	AI	Feedback input for the constant-voltage loop.
12	IFB	AI	Feedback input for the constant-current loop.
13	VBUS/GPIO1	A IO	Over-voltage fault indication output, used to pull low an optocoupler.
14	OPTO	AO	Current sink output for optocoupler connection.
15	VDD	PWR	Supply input voltage.
16	BLD/GPIO2	D IO	Bleeder connection node to provide another path to discharge the output capacitor.

Functional Block Diagram



Operation

The RT7202KJ is a highly integrated secondary-side USB PD Type-C controller with various functions and protections for off-line AC-DC converters.

Power Structure

Biased by the VDD pin, the RT7202KJ has two regulated DC output voltages, V_5 and V_2, to supply internal circuitry and an internal microprocessor (MCU). A bypass capacitor at the V2 pin is required to improve stability of the internal LDO and to minimize regulated ripple voltages.

Constant-Voltage (CV) Regulators

A constant-voltage (CV) regulator is connected to OPTO, an open-drain output pin. The operation of the feedback loop is similar to that of the traditional TL431 shunt regulator except that V_{OPTO} operating range is wider, from 0.3V to 25V, which enables easy design of converters with a wider output range. The OPTO pin will be in high-impedance state, if the VDD voltage is still below a UVLO threshold V_{VDD_ON}, to ensure a smooth power-on sequence. The reference voltage, V_{REF_CV}, for the voltage feedback loop, is analog output voltage from the embedded DAC, and its digital counterpart is from the MCU. The analog output range of the 11-bit DAC is from V_{DAC_MIN} = 0.15V to V_{DAC_MAX} (typical 2.2V), which makes output voltage resolution as small as 10mV to achieve high-precision CV regulation.

Constant-Current (CC) Regulators

The constant-current (CC) regulator is also connected to OPTO pin. The analog current loop output range of the 10-bit DAC is from 0 to V_{DAC_MAX} (typical 1.5V).

Current-Sense Amplifier

To minimize power loss of the current sense resistor in the converter, the RT7202KJ includes an amplifier with virtually zero input offset voltage and with a register-programmable voltage gain of 20 or 40. The sensed output current signal is amplified by the current-sense amplifier, shown as "Io_signal" in Figure 1, which is then sent to the MCU, by way of an ADC for analog-to-digital conversion, to update the output current status in the MCU. According to the output current status and firmware- programmable over-current threshold, the over-current protection can be activated.

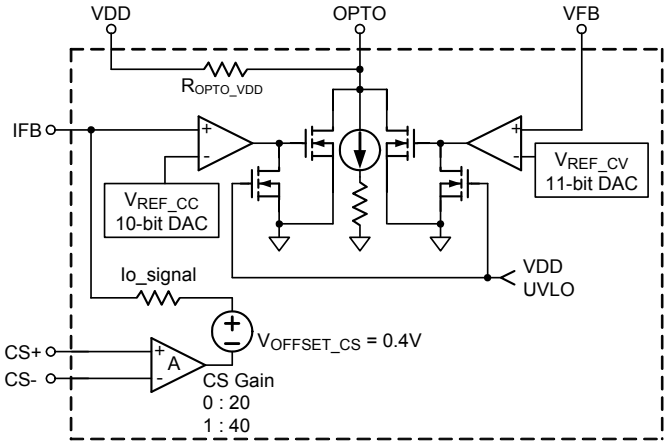


Figure 1. CV/CC Loop Block Diagram

Interface of DP and DM

The DP and DM pin, connected to the MCU via an ADC, can be reprogrammed for other purposes since they can be used as an analog/digital input /output, as shown in Figure 2.

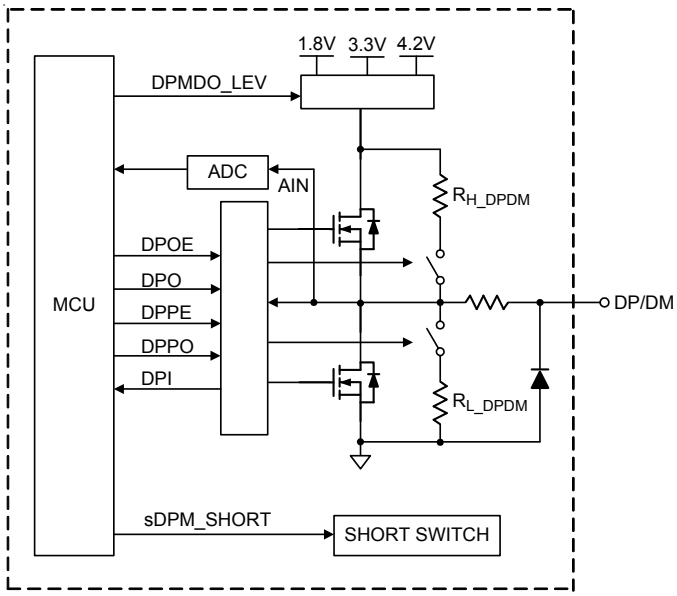


Figure 2. Interface of DP/DM

Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with USB PD Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80µA, 180µA, and 330µA, provided by each of the CC pins, will be advertised to an Upstream Facing Port (UFP) as default USB current, 1.5A, and 3.0A, respectively, as shown in Figure 3.

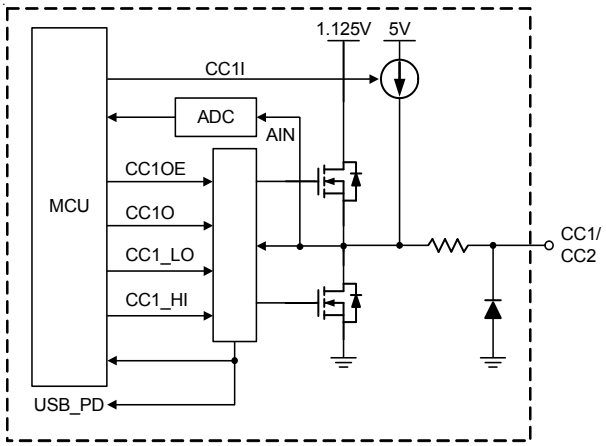


Figure 3. Interface of CC1 and CC2

Open-Drain Drivers for BLD and VBUS Pins

The BLD and VBUS pins with their specific functions are driven by open-drain drivers, as shown in Figure 5 and explained below.

The BLD pin is used as a bleeder to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 12V to 5V. A resistor is connected between V_{OUT} and the BLD pin and a power resistor can be used for better power dissipation capability.

The VBUS pin is used as a bleeder to help discharge the VBUS capacitor to V_{safe0V} upon the detachment of a connected device and provide real-time VBUS voltage detection by ADC.

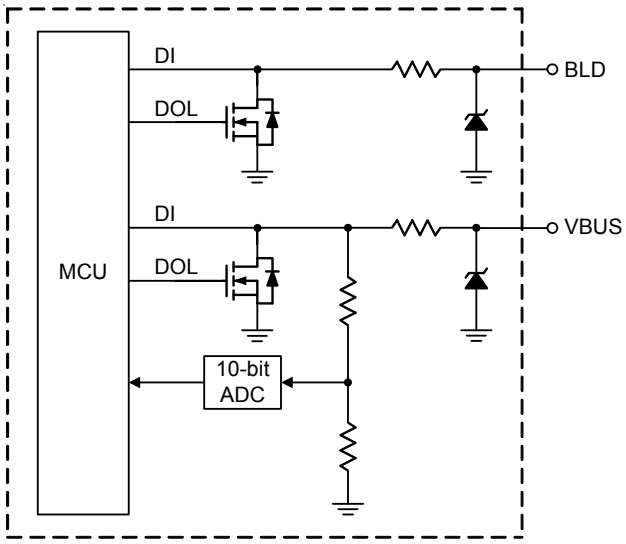


Figure 4. Interface of the BLD and VBUS Pins

Absolute Maximum Ratings (Note 1)

- USBP to GND ---------- –0.3V to 32V
- VDD, OPTO, BLD/GPIO2, VBUS/GPIO1 to GND ---------- –0.3V to 28V
- CC1, CC2 to GND ---------- –0.3V to 22V
- VFB, IFB, DP, DM, CS+, CS- to GND ---------- –0.3V to 7V
- V2 to GND ---------- –0.3V to 2.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 4x4 ---------- 0.39W
- Package Thermal Resistance (Note 2)
  WQFN-16L 4x4, θ_{JA} ---------- 256.4°C/W
  WQFN-16L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 3V to 22V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold Voltage	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold Voltage	V_{VDD_OFF}		2.7	2.75	2.8	V
VDD Turn-On/-Off Hysteresis	V_{VDD_HYS}		--	0.3	--	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.6V	--	200	300	μA
VDD Operating Current	I_{DD_OP}		--	6	--	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	In sleep mode	--	--	750	μA
VDD Over-Voltage Protection Threshold Voltage	V_{VDD_OVP}		23	24	25	V
VDD Over-Voltage Protection Deglitch Time	t_{D_VDDOVP}	(Note 5)	--	50	--	μs

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Register-Programmable Over-Voltage Protection Threshold	V_{VOUT_OVP}	Ratio of V_{REF_CV}	00	109.25	115	120.75	%
			01	114	120	126	
			10	118.75	125	131.25	
			11	Disable			
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} = 5V		20.5	21.6	22.7	MHz
Internal Bias							
V2	V_{BIAS_V2}	3V < V_{DD} < 25V		1.71	1.80	1.89	V
V2 Output Short-Circuit Current	I_{V2_SC}			30	50	70	mA
Regulator Section							
Default Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$			0.485	0.5	0.515	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	11-bit D/A conversion		--	0.15	--	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$			2.178	2.2	2.222	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$	10-bit Digital-to-Analog converter		1.485	1.5	1.515	V
Maximum ADC Sense Voltage	V_{ADC_MAX}	10-bit A/D conversion		2.178	2.2	2.222	V
Ratio of Change in Reference Input Voltage to Change in OPTO Voltage	$\frac{\Delta V_{REF}}{\Delta V_{OPTO}}$	ΔV_{OPTO} = 25V to V_{REF} (Note 5)		−2.4	−1.2	--	mV/V
Reference Input Current	I_{REF}	(Note 5)		--	0.1	1	μA
Off-State OPTO Current	I_{OPTO_OFF}	OPTO is open (Note 5)		--	230	500	nA
Dynamic Impedance	$\|Z_{OPTO}\|$	V_{OPTO} = V_{REF}, I_{OPTO} = 1mA, at 1kHz (Note 5)		--	0.22	0.5	Ω
OPTO Turn-On Impedance	R_{ON_OPTO}	I_{OPTO_SINK} = 10mA (Note 5)		--	--	150	Ω
Maximum OPTO Sinking Current	I_{OPTO_MAX}			2	--	20	mA
Internal Resistor between OPTO and VDD	R_{OPTO_VDD}			40.8	51	61.2	kΩ
Internal Resistor between OPTO and GND	R_{OPTO_GND}			50	60	70	kΩ
Internal Sinking Current Source	I_{SINK_OPTO}	During VDD UVLO, I_{SINK_OPTO} will be shorted.		20	25	30	μA
VBUS Section							
Maximum VBUS Sinking Current	I_{VBUS_MAX}			2	--	20	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_SINK} = 10mA (Note 5)		--	--	150	Ω
Register-Programmable Internal Bias Current	I_{BIAS_VBUS}		0	Open-Drain			μA
			1	90	100	110	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
BLD Section							
Maximum BLD Sinking Current	I_{BLD_MAX}	In 300ms		0.23	--	0.32	A
Pull-Low Impedance	R_{L_BLD}	(Note 5)		--	30	--	Ω
Current Sense Amplifier							
Register-Programmable Current-Sense Voltage Gain	K_{CS}		0	--	20	--	V/V
			1	--	40	--	
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			--	0.4	--	V
Unit Gain Bandwidth		(Note 5)		1000	--	--	kHz
Output Current		(Note 5)		--	0.1	--	mA
DP, DM Section							
Pull-High Resistor	R_{H_DPDM}			5	10	15	kΩ
Pull-Low Resistor	R_{L_DPDM}			15	20	25	kΩ
Register-Programmable Output High Voltage	V_{OH_OD}	V_{DD} = 5V, R_{Load} = 15kΩ	00	Open-Drain			V
	$V_{OH\_3.3V}$		01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.2V}$		11	3.78	4.2	4.62	
Output Low Voltage	V_{OL_OD}	R_{Load} = 15kΩ		--	--	0.2	V
	$V_{OL\_3.3V}$						
	$V_{OL\_1.8V}$						
	$V_{OL\_4.2V}$						
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	0.7	0.8	0.9	V
			01	0.8	0.9	1.0	
			10	0.9	1.0	1.1	
			11	1.0	1.1	1.2	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.4	0.5	0.6	V
			01	0.5	0.6	0.7	
			10	0.6	0.7	0.8	
			11	0.7	0.8	0.9	
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
Register-Programmable Internal Bias Current	I_{BIAS_DPDM}		0	Disable			μA
			1	90	100	110	
CC1, CC2 Section							
Output High Voltage	V_{OH_CC}			1.05	1.125	1.2	V
Output Low Voltage	V_{OL_CC}			0	0.0375	0.075	V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Register-Programmable Input High Trip Voltage	V_{IH_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Rising Time	t_{R_CC}	C_{Load} = 470pF		300	--	700	ns
Falling Time	t_{F_CC}	C_{Load} = 470pF		300	--	700	ns
Register-Programmable Sourcing Current	I_{CC_SRC}		00	High Impedance			μA
			01	72	80	88	
			10	166	180	194	
			11	304	330	356	
USBP Section							
Output High Voltage	V_{OH_USBP}			VDD + 6.5	VDD + 8	VDD + 9.5	V
Maximum Output High Voltage	V_{MAX_USBP}			26.5	28	29.5	V
Register-Programmable Rise Time	t_{R_USBP}	C_{Load} = 4nF, V_{DD} = 5V, from 20% to 80%	00	200	300	400	μs
			01	480	600	720	
			10	980	1200	1440	
			11	1920	2400	2880	
Output Low Voltage	V_{OL_USBP}	V_{DD} = 3V, I_{USBP} = 100μA before start-up		--	--	1	V
Fall Time	t_{F_USBP}	C_{Load} = 4nF, V_{DD} = 5V, from 90% to 10%		--	--	2	μs

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

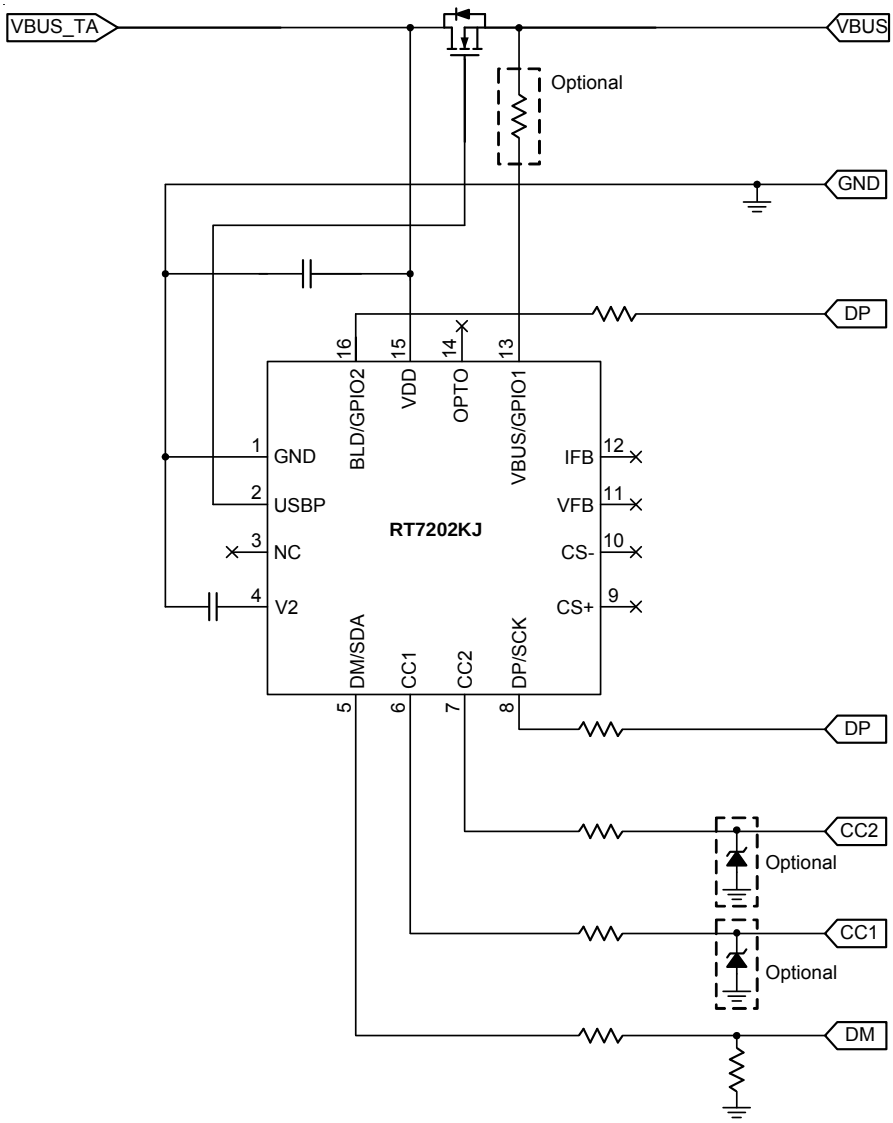
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

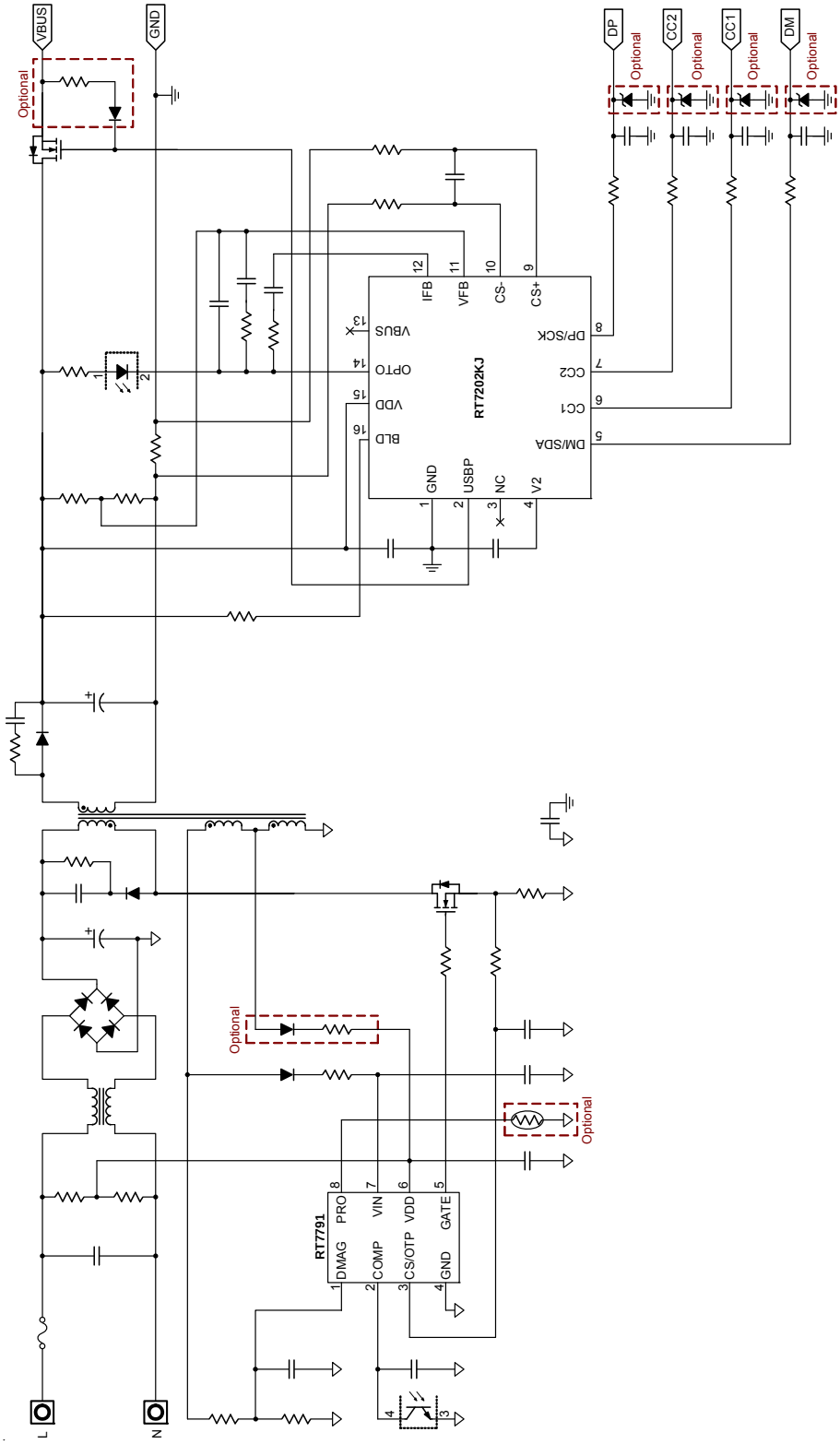
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guaranteed by design.

Typical Application Circuit

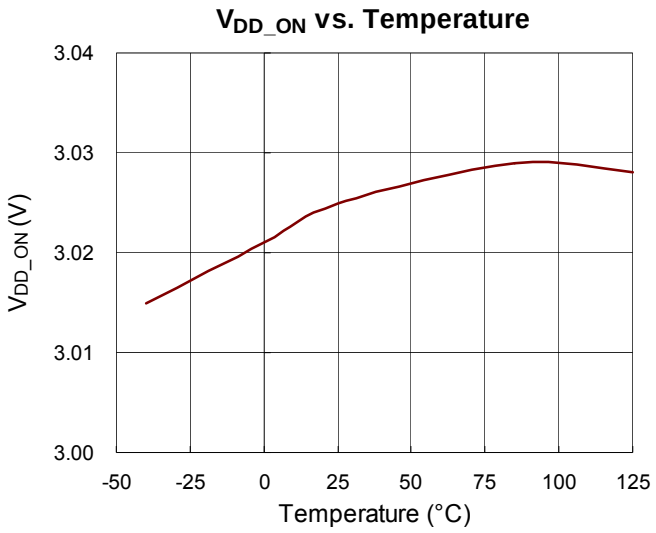


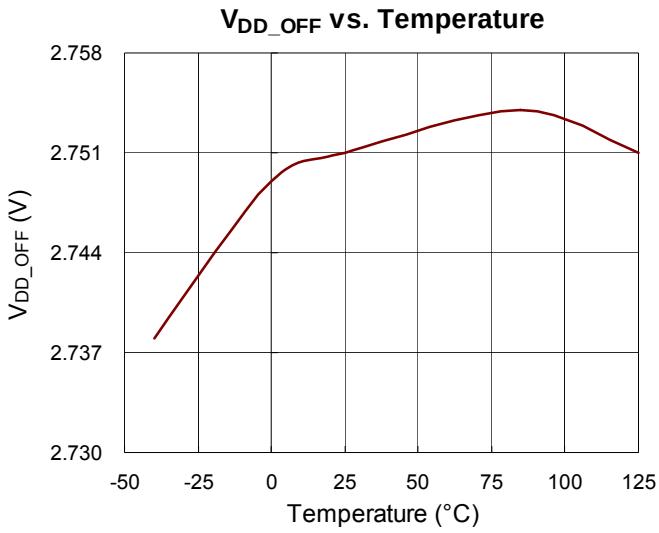
RT7202KJ Typical Application Circuit for Sink Side

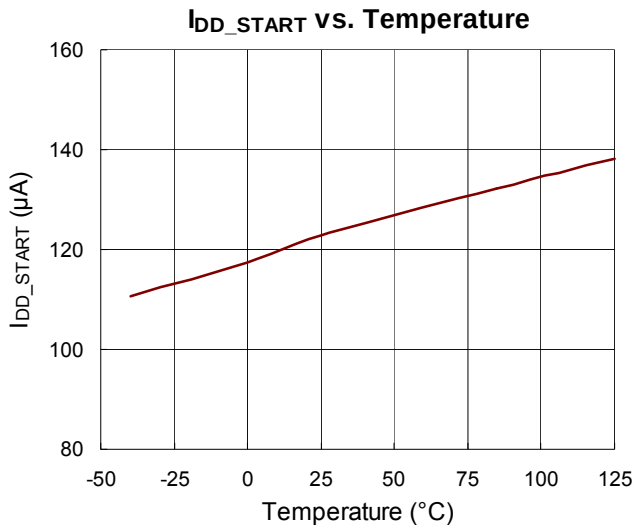


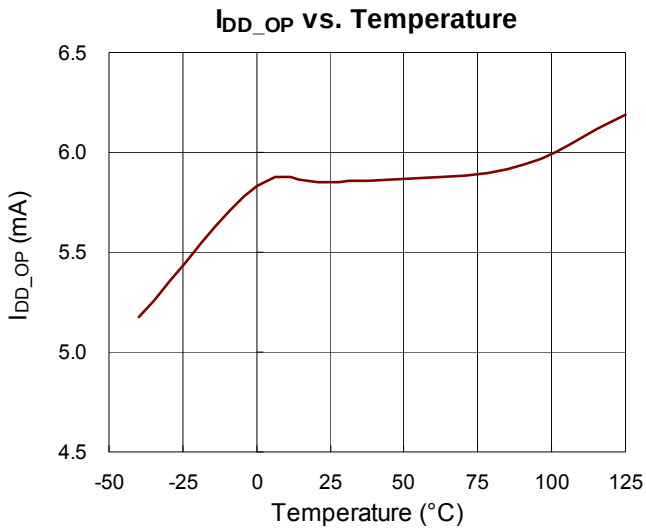
RT7202KJ Typical Application Circuit for Source Side

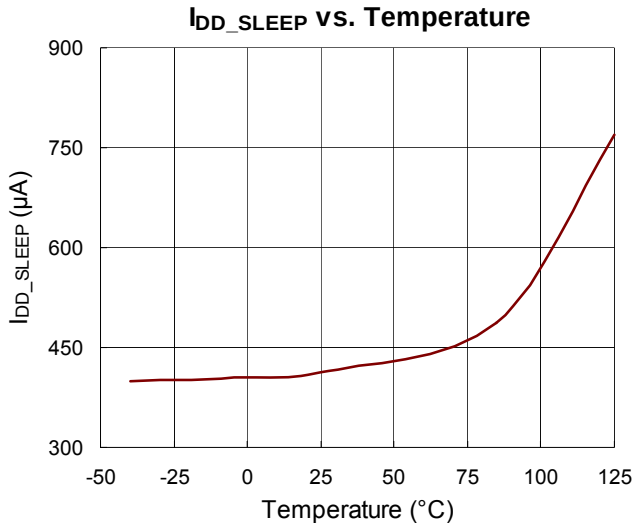
Typical Operating Characteristics

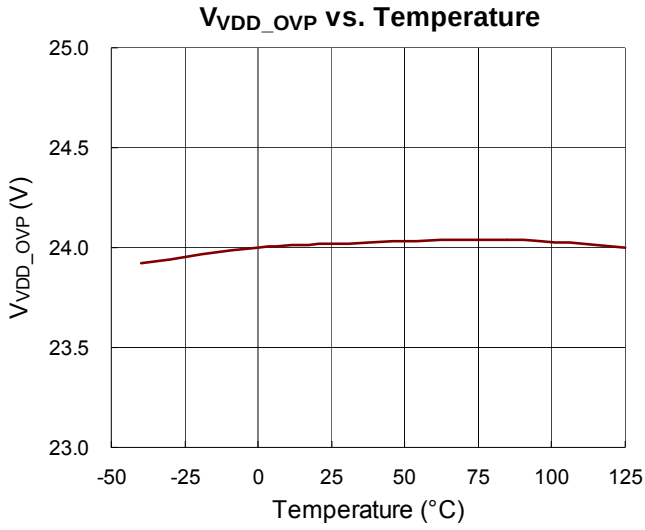


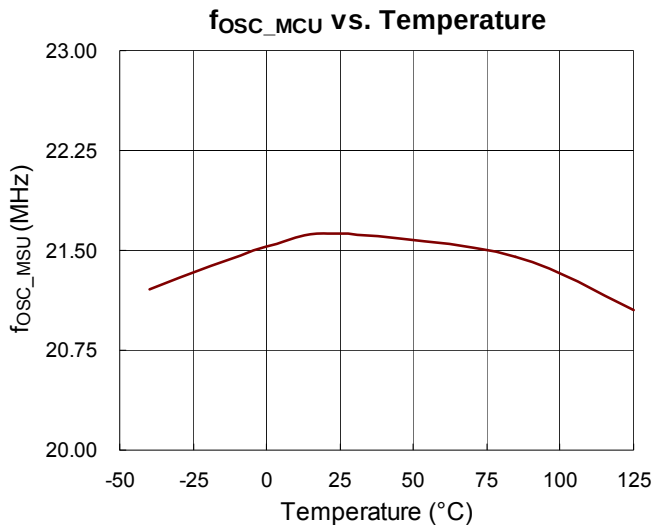


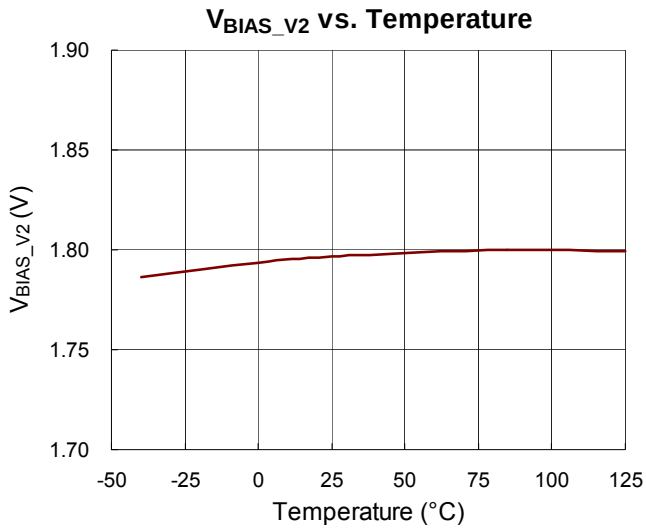


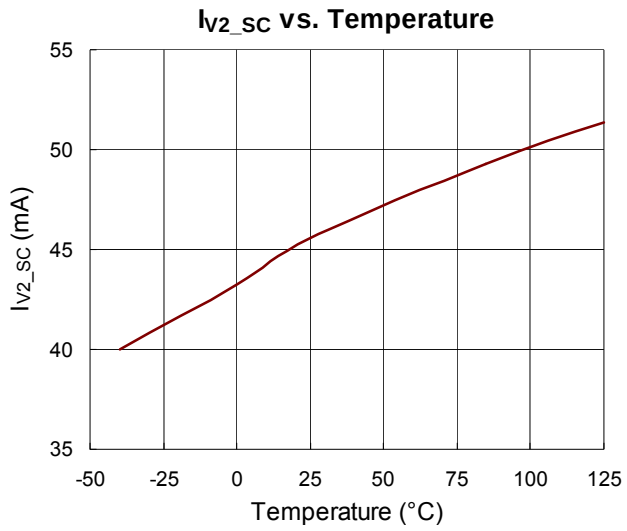


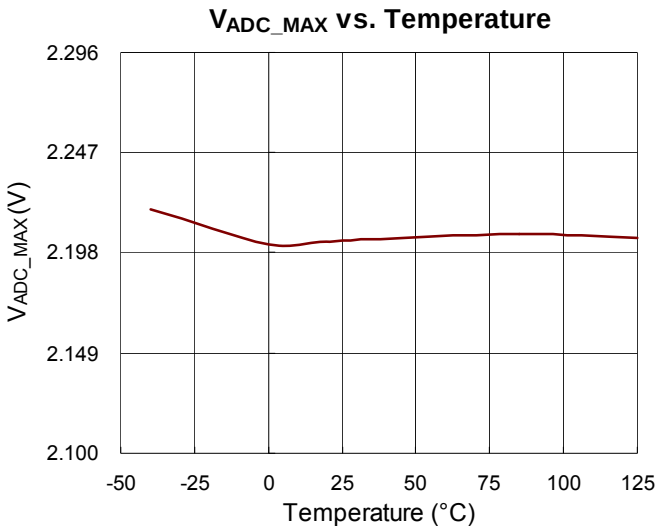


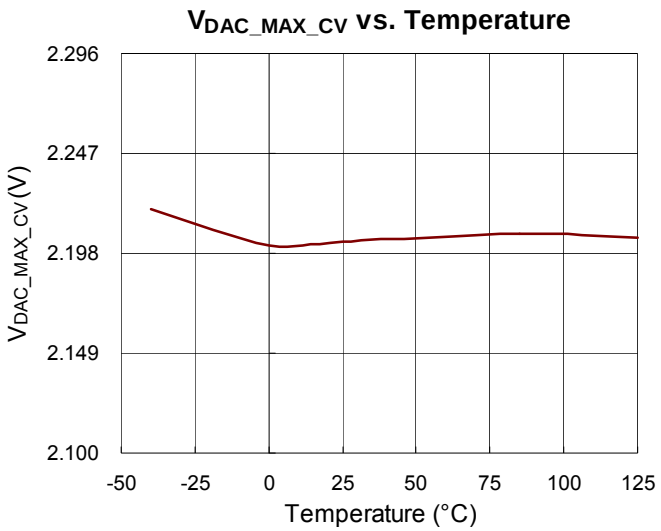


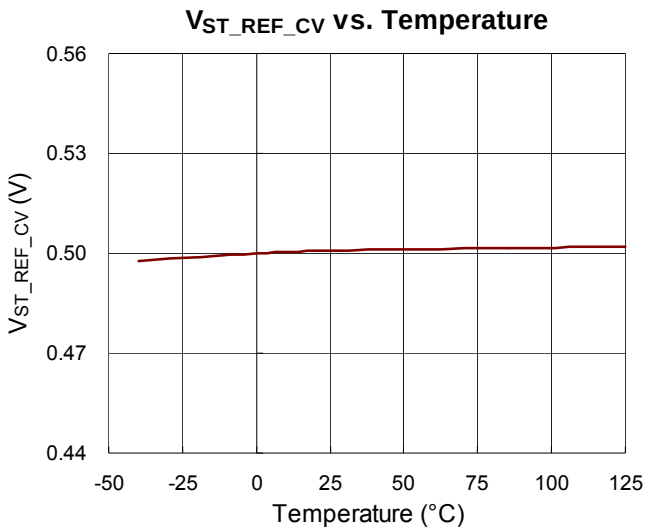


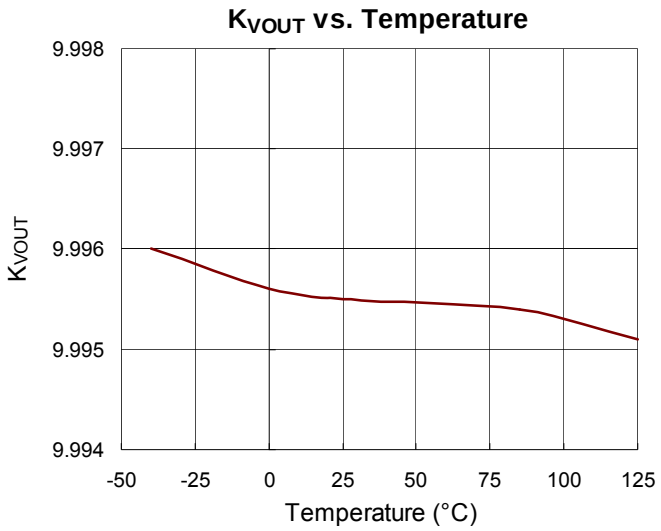


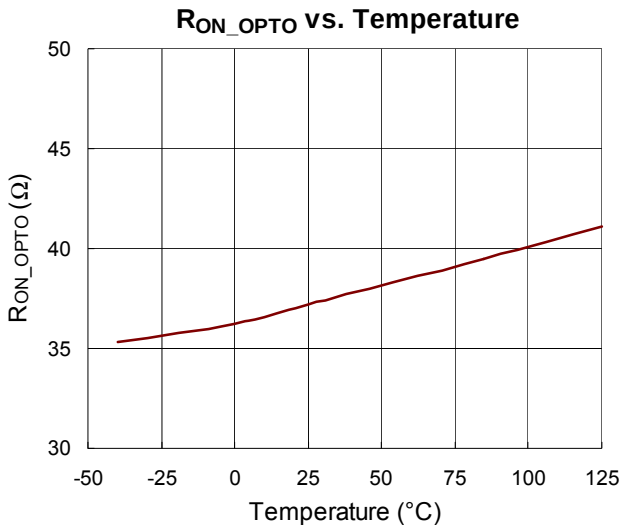


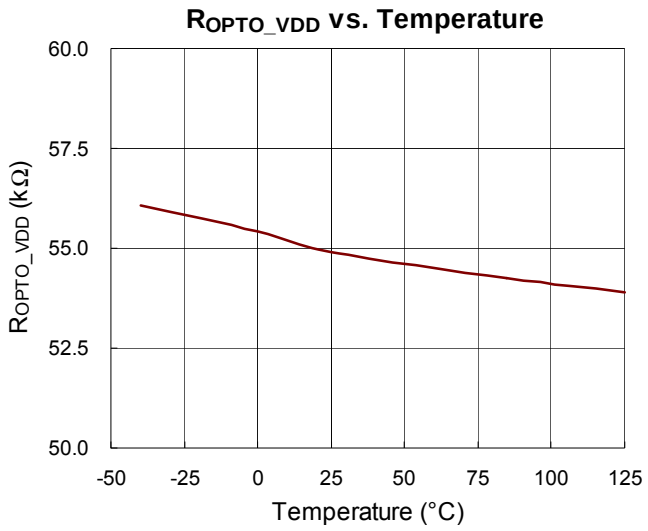


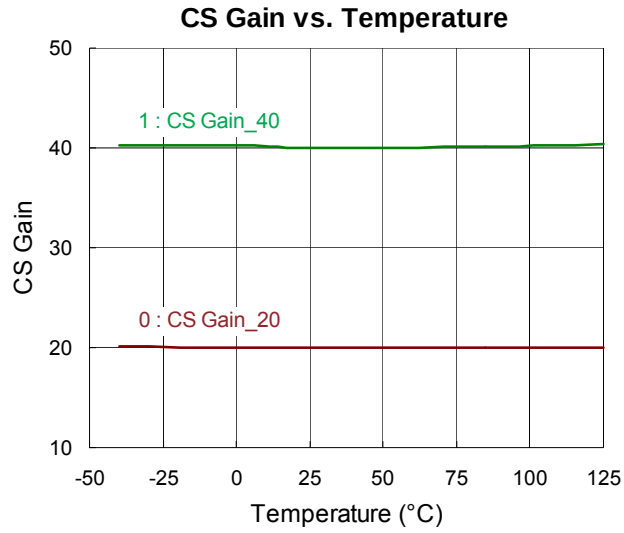


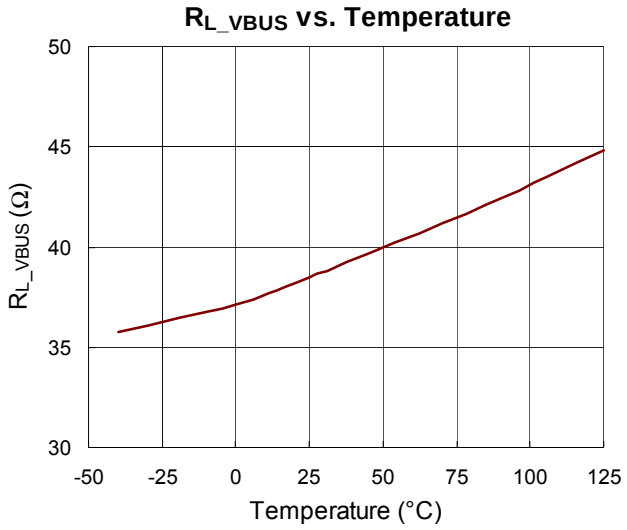


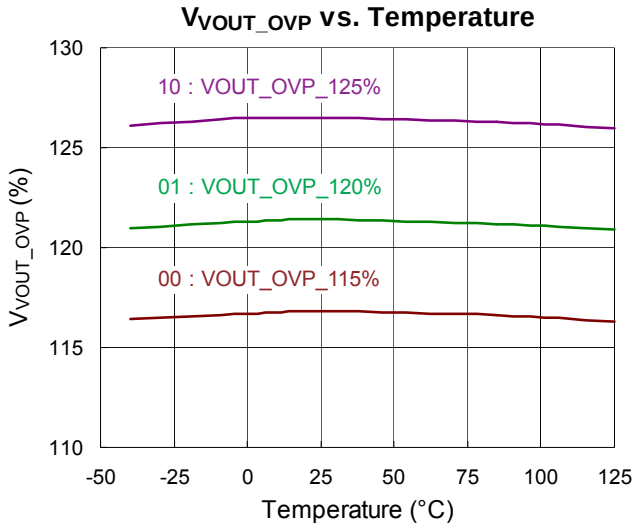


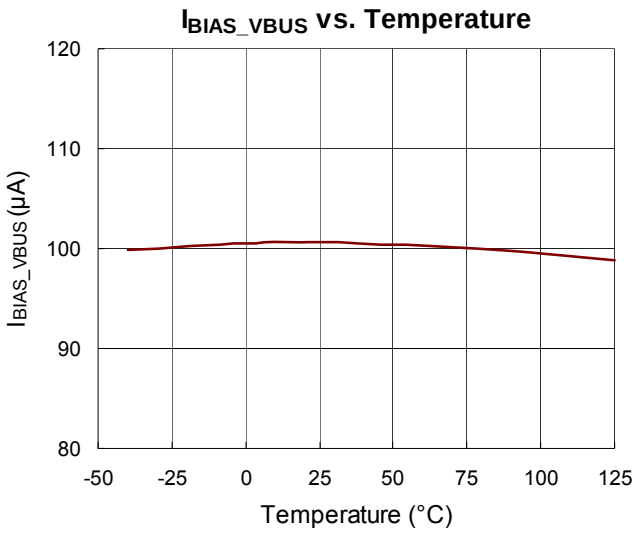


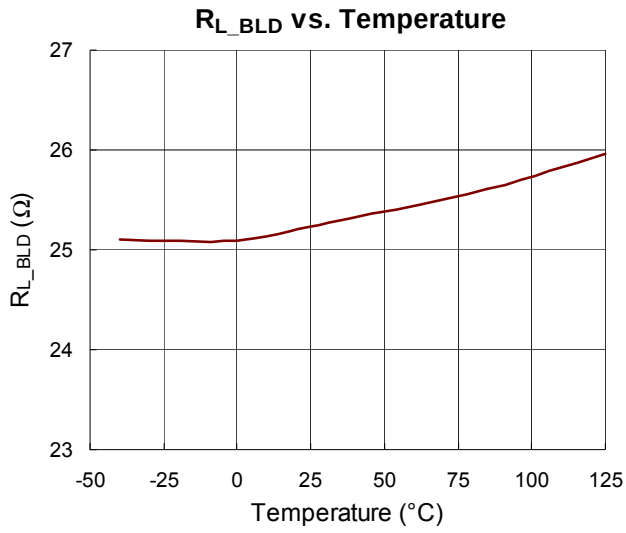


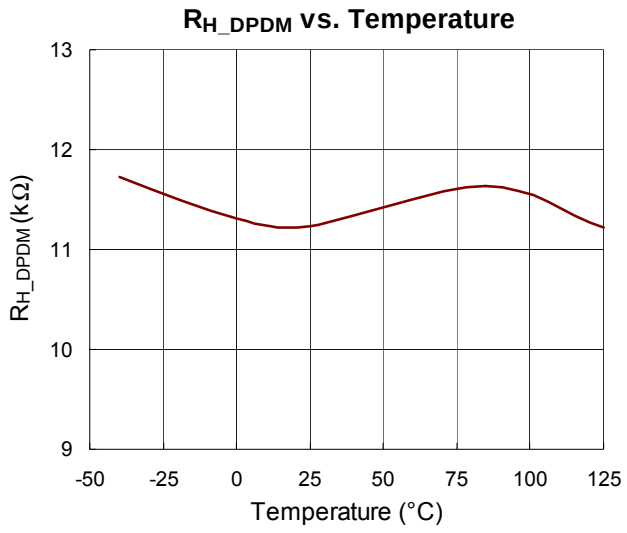


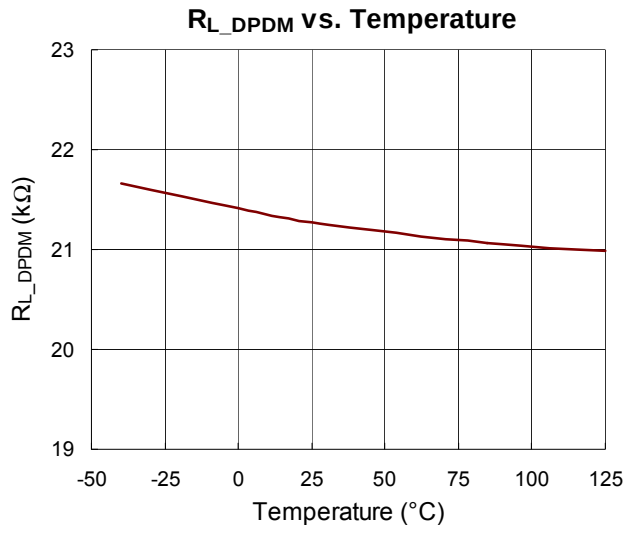


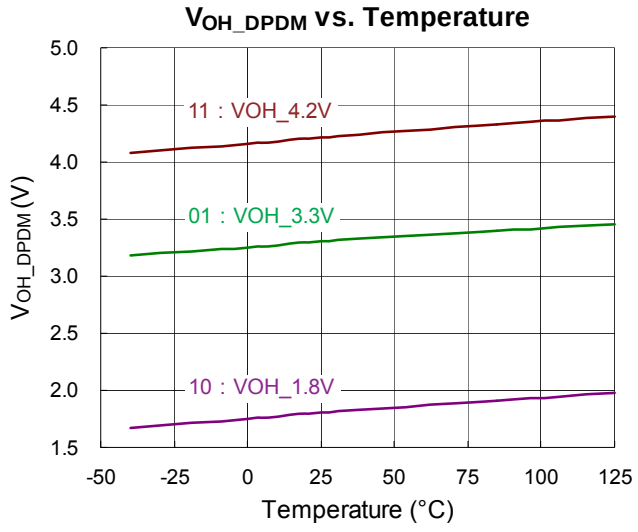


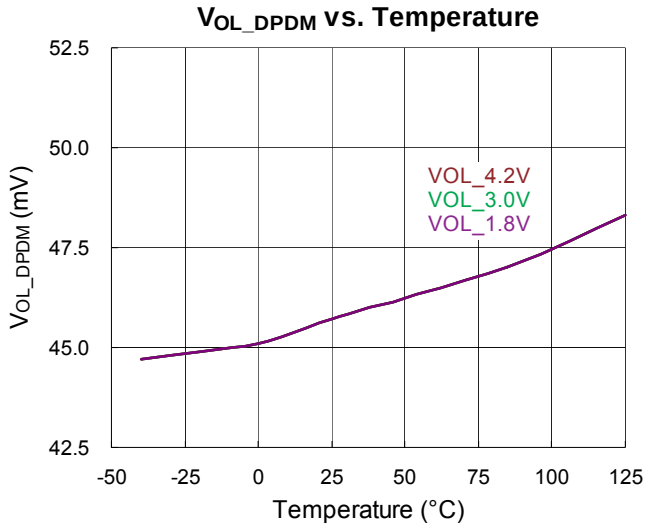


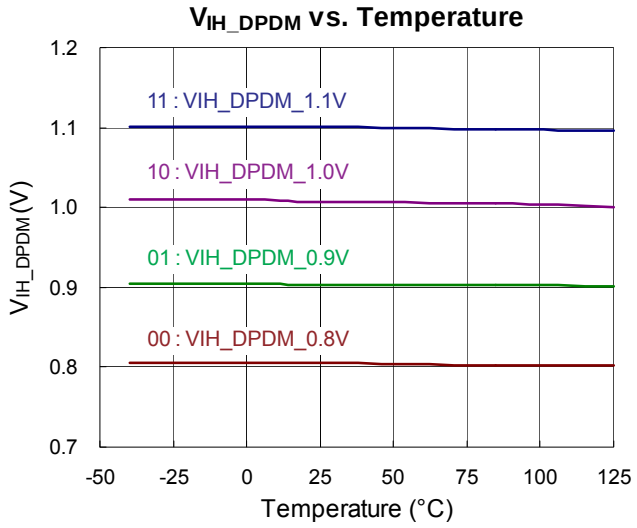


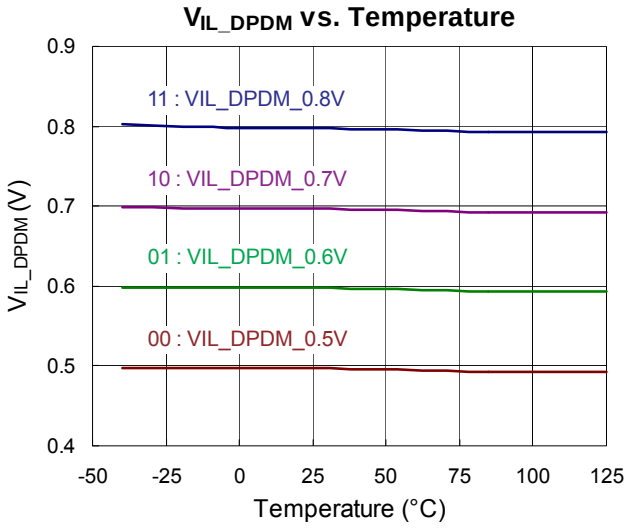


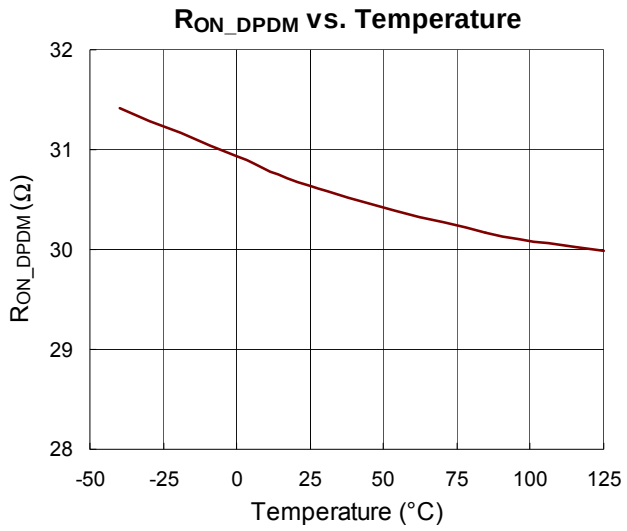


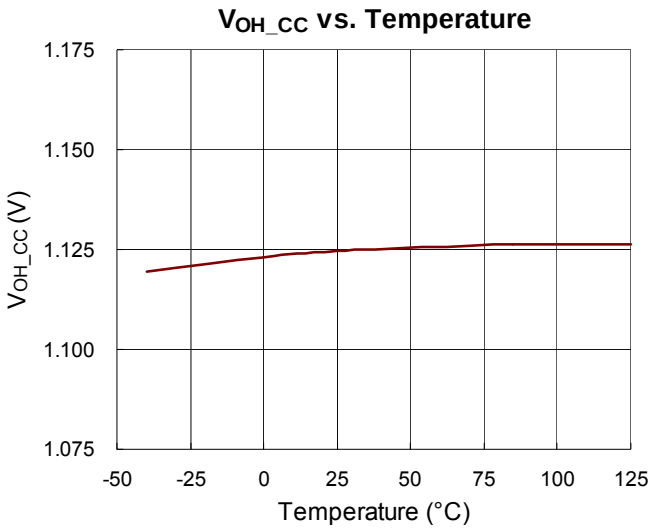


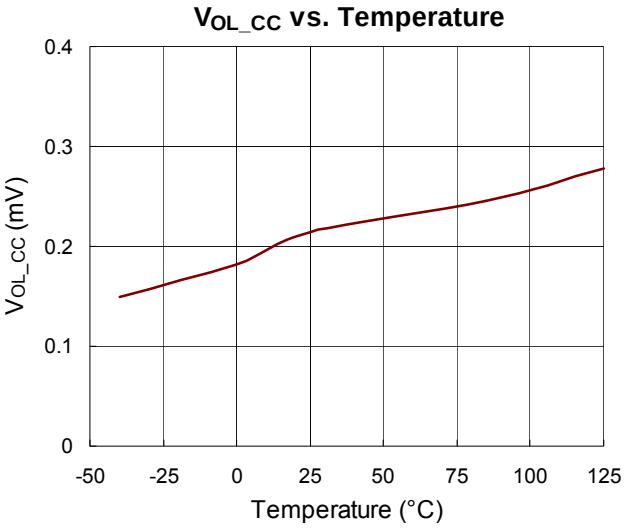


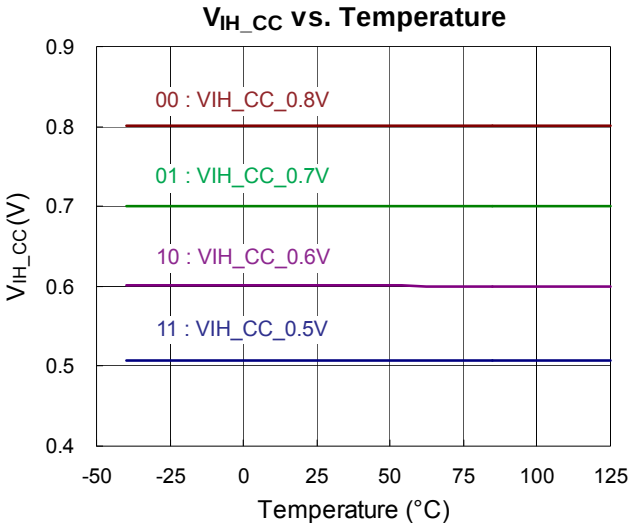


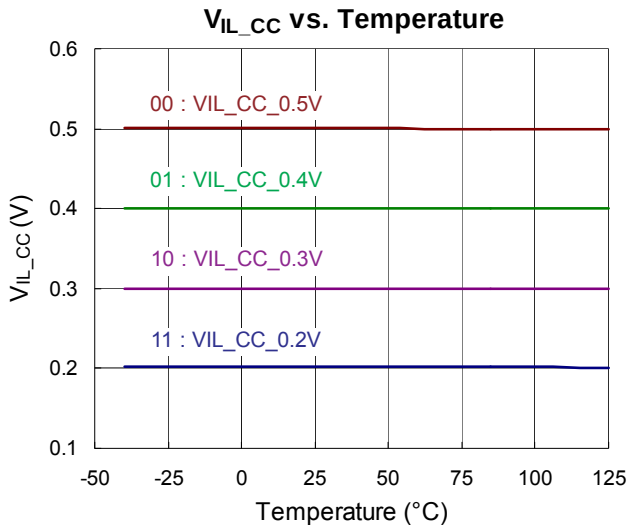


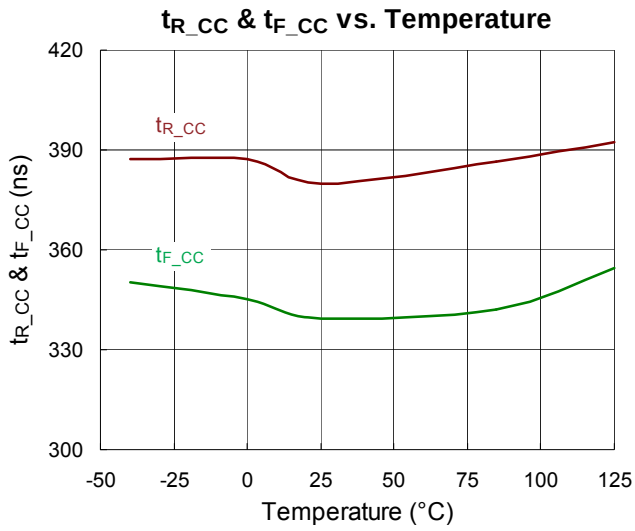


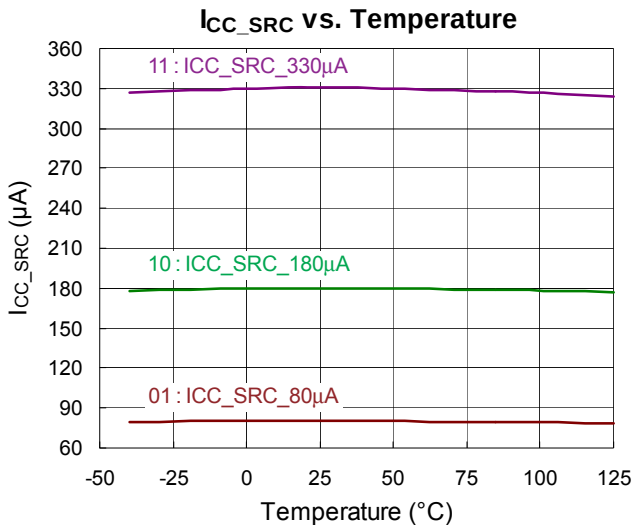


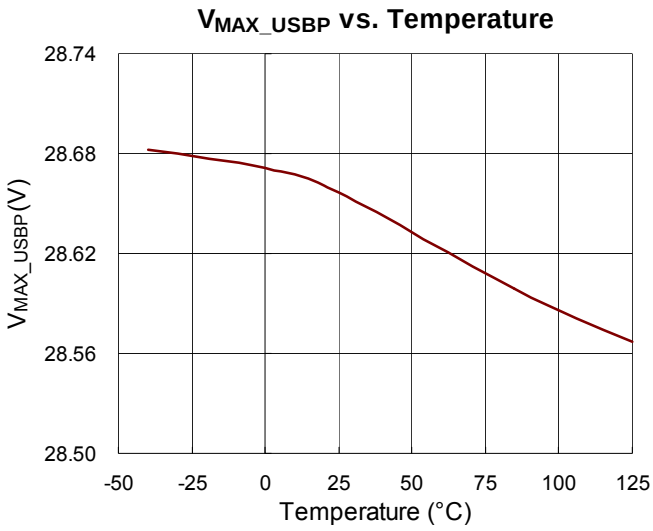












Application Information

Constant-Voltage (CV) Loop

As shown in Figure 5, the RT7202KJ incorporates an error amplifiers (EA) to regulate output voltage. The output voltage is determined as :

$V_{OUT} = K_{VOUT} \times V_{REF\_CV}$

where $K_{VOUT} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10$ (typ)

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, and its digital counterpart, which is controlled by the MCU, as shown in Functional Block Diagram.

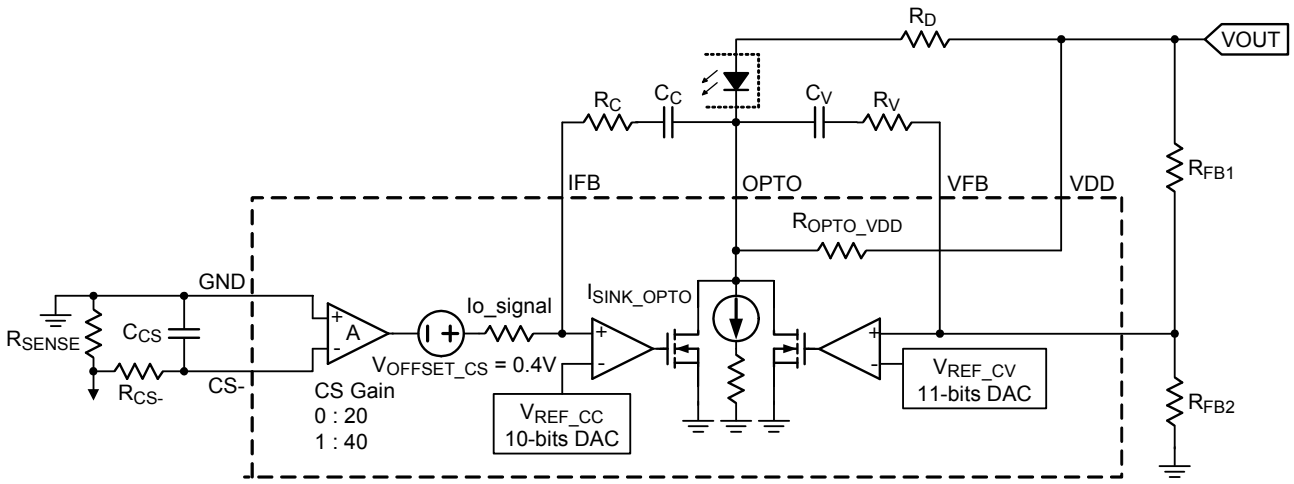


Figure 5. CV Loop and Current-Sense Amplifier

The OPTO driver sinks current through an optocoupler and an external resistor R_D from output voltage, and the optocoupler isolates the secondary side from the primary side and also provides the feedback compensation signal for the primary side. Note that for better linearity of the loop compensation range, R_D should be designed to cover for operation at the minimum output voltage.

$$\frac{V_{OUT\_MIN} - V_F - 0.3V}{R_D} \times CTR \geq I_{COMP\_MAX}$$

CTR : Current transfer ratio of the optocoupler

V_F : Forward voltage of the optocoupler

0.3V : The minimum OPTO voltage for the OPTO driver to sink 2mA.

I_{COMP_MAX} : The maximum COMP sourcing current of a traditional PWM controller in the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected the COMP pin in the PWM controller.

Constant-Current (CC) Loop and Current-Sense Amplifier

The RT7202KJ integrates a virtually-zero input-offset-voltage current-sense amplifier. The voltage gain of 20 or 40 can be set by the internal register. The amplified output current sense signal, sent to an ADC for A/D conversion, is monitored and processed by the MCU, and is also sent to the CC loop. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed by chargers' requirements. Both the constant-voltage and constant-current compensation loops are connected together at the OPTO pin.

External Cable Compensation Circuit

The RT7202KJ provide option for external CV resisters in order to conduct linear cable compensation. The cable compensation can be implemented by the compensation resister Rc of the application circuit as shown in Figure 6. The compensation voltage is determined as :

$V_{COMPENSATION} = I_{OUT} \times R_{SENSE} \times (R_{FB1} / R_{FB2})$

Power-Up Sequence

Figure 6 shows the timing diagram for the power-up sequence. When start-up, the default output is set at 5V. Once a Type-C cable is attached, the UFP will deliver voltage and current settings to the RT7202KJ for the MCU to decode and to program reference voltages, V_{REF_CV} for the CV, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, the RT7202KJ will enter power-saving mode, under which the RT7202KJ operates at ultra-low operating current and thus the total input power can be saved. If the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7202KJ will exit power-saving mode.

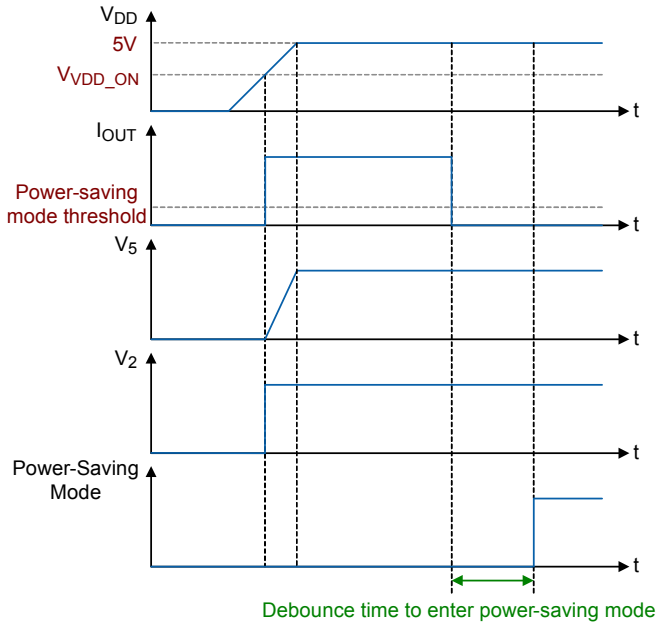
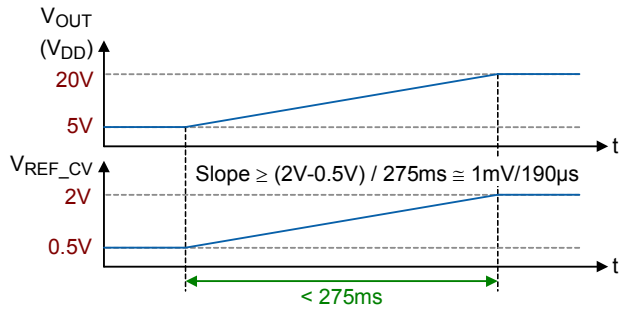


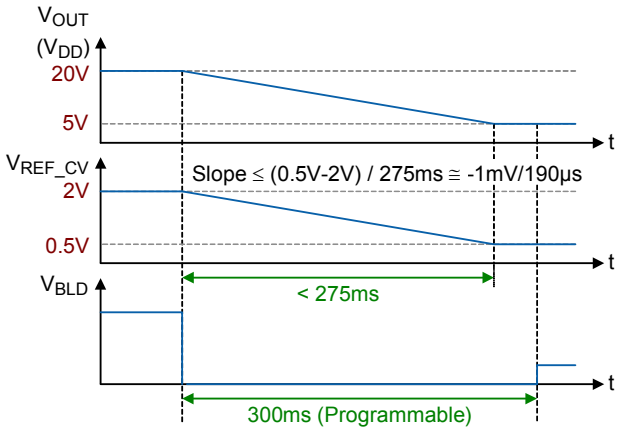
Figure 6. The Bias Voltages Sequence during Start-Up

Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and fall time of output voltages should be less than 275ms in accordance with the USB PD Specification, as shown in Figure 7.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 7. Output Voltage Transient Waveforms

During the time of V_{OUT} falling, as shown in Figure 7(b), the RT7202KJ will provide an extra discharging path for the output capacitor so that V_{OUT} can be settled in a shorter duration.

The RT7202KJ provides an open drain driver at the BLD pin as an active dummy load switch to discharge the output capacitor, as shown in the Figure 8 and turn on timing can be programmable. The designed R_{DUMMY} is as :

C_{OUT} x (R_{DUMMY} + R_{L_BLD}) x 2 < 275ms

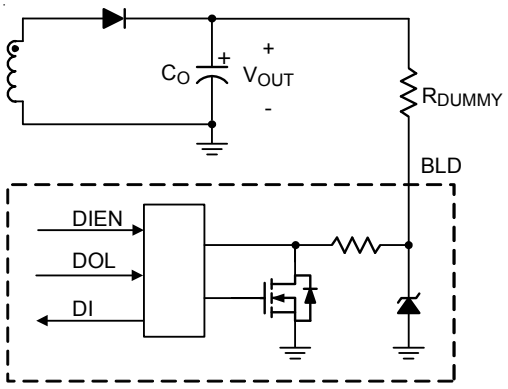


Figure 8. Application Circuit of an Active Dummy Load

Blocking MOSFET Control (USBP)

The RT7202KJ provides a push-pull driver for controlling external blocking N-MOSFET. The push-pull driver is not only can control N-MOSFET smooth turn-on to avoid V_{OUT} drops in the capacitive load condition but also provide quickly turn-off in fault condition.

Once the communication is set up with an UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector of the UFP is detected, the N-MOSFET will be turned on. If V_{OUT} over-voltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged by the V_{OUT} over-voltage condition. If V_{OUT} is shorted to GND, the N-MOSFET will also be turned off automatically so that output power can be limited.

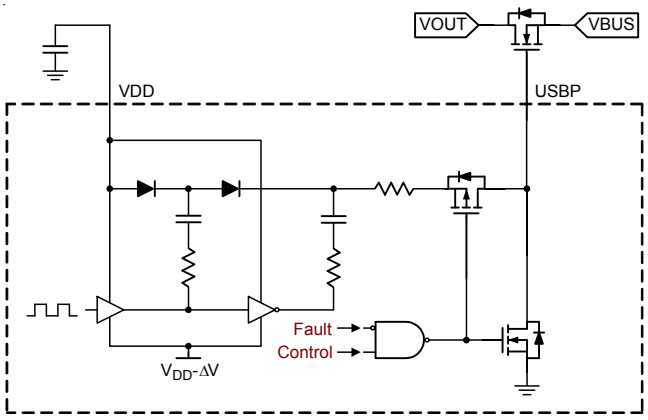


Figure 9. Blocking N-MOSFET Control

Output Over-Voltage Protection

As shown in the Figure 10 and Figure 11, the RT7202KJ provides a fast turn-off blocking N-MOSFET as a backup VOUT over-voltage protection, in case the optocoupler of the feedback loop is malfunction due to aging. If the internal voltage related to VDD is higher by the programmable threshold V_{VOUT_OVP}, the USBP pin will be pulled low. The USBP pin voltage will be latched low until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

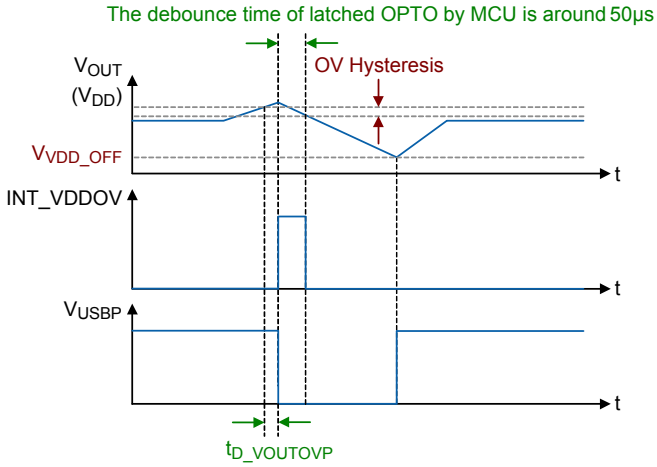


Figure 10. Timing Sequence of the OVP Pin Function

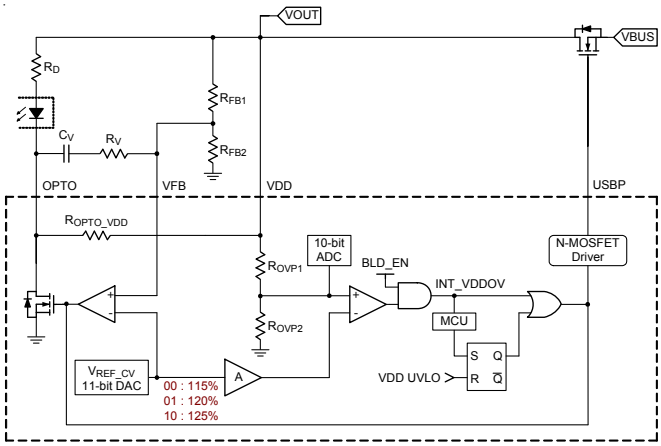


Figure 11. OVP Functional Diagram

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-16L 4x4 package, the thermal resistance, θ_{JA}, is 256.4°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board.

The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (256.4°C/W) = 0.39W for a WQFN-16L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 12 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

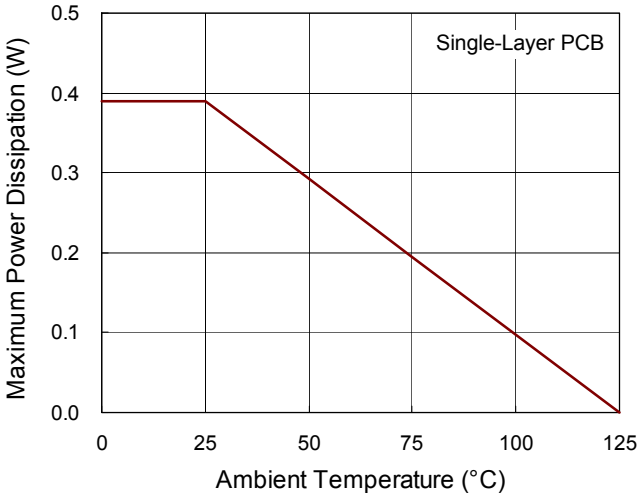
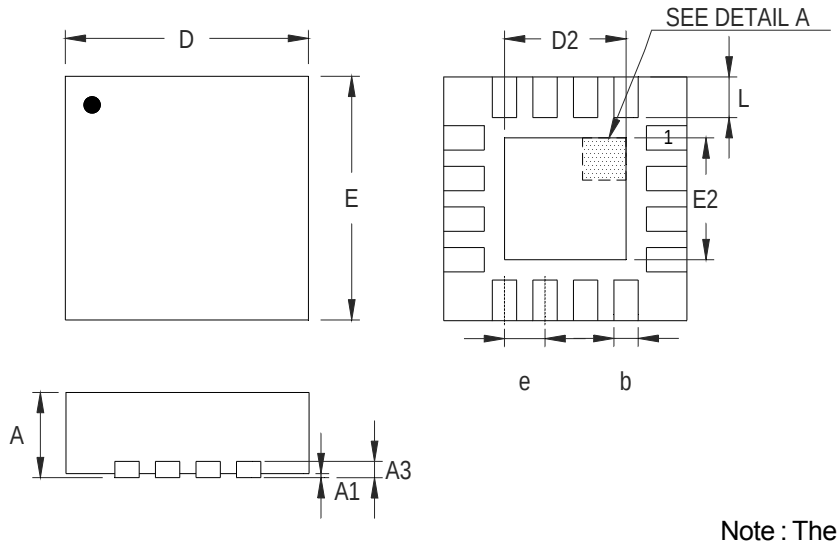
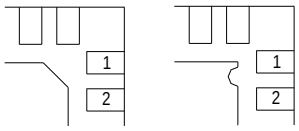


Figure 12. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

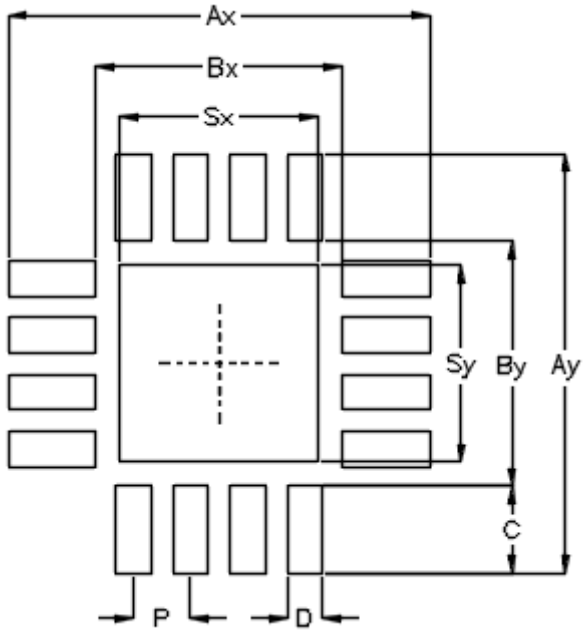
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.380	0.010	0.015
D	3.950	4.050	0.156	0.159
D2	2.000	2.450	0.079	0.096
E	3.950	4.050	0.156	0.159
E2	2.000	2.450	0.079	0.096
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

W-Type 16L QFN 4x4 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-16	16	0.65	4.80	4.80	2.80	2.80	1.00	0.40	2.25	2.25	±0.05

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Datasheet Revision History

Version	Date	Item	Description
P00	2018/12/5		First Edition