All-in-One USB PD and Bidirectional PWM Buck-Boost Controller

General Description

The RT7885 is a USB Power Delivery (USB PD) controller adopting Buck-Boost PWM control scheme and highly integrating functions specially for USB power bank applications, with that this controller is designed to operate in peak current mode with programmable current limit and switching frequency.

The RT7885 embeds an ARM Cortex™-M0 MCU so as to facilitate various functions of communication protocol, protections and customized requirements. Moreover, this RT7885 has built-in charge pumps for driving low-cost NMOS to control the power path. Therefore this IC provides the best USB PD solution for a power bank application with the lowest count of external components.

Applications

- USB PD Type-C Power Bank

Ordering Information

RT7885□□□-□

- □ (last): Programmed Firmware Code AABBX
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- □ (third): Package Type
  - QW : WQFN-60L 7x7 (W-Type)
- □ (second): Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- □ (first): RT7885 Version (Refer to Version Table)

Note :

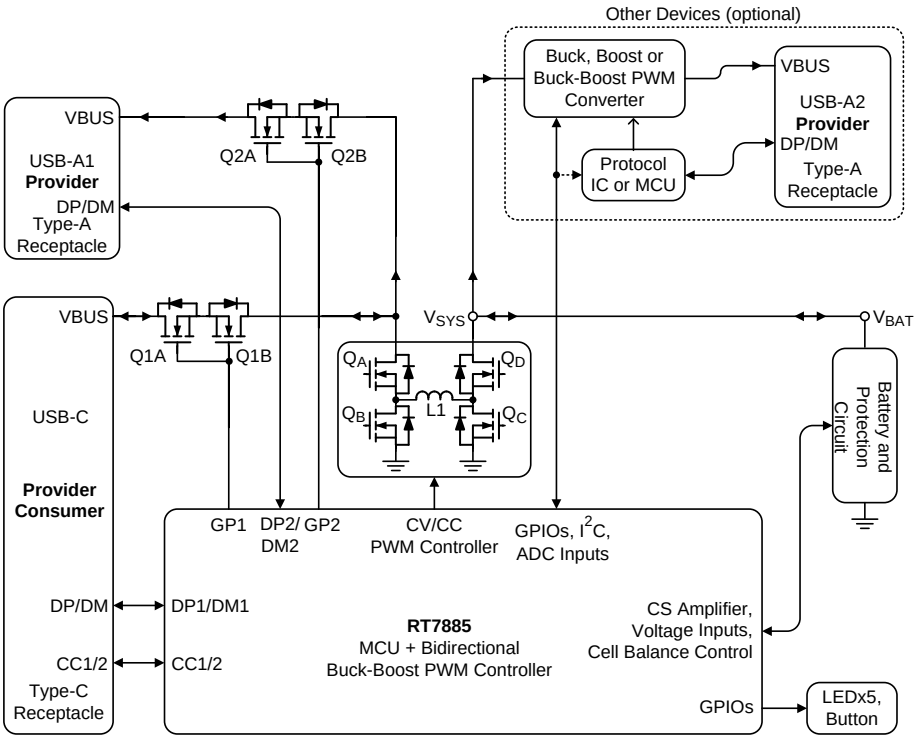
The products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

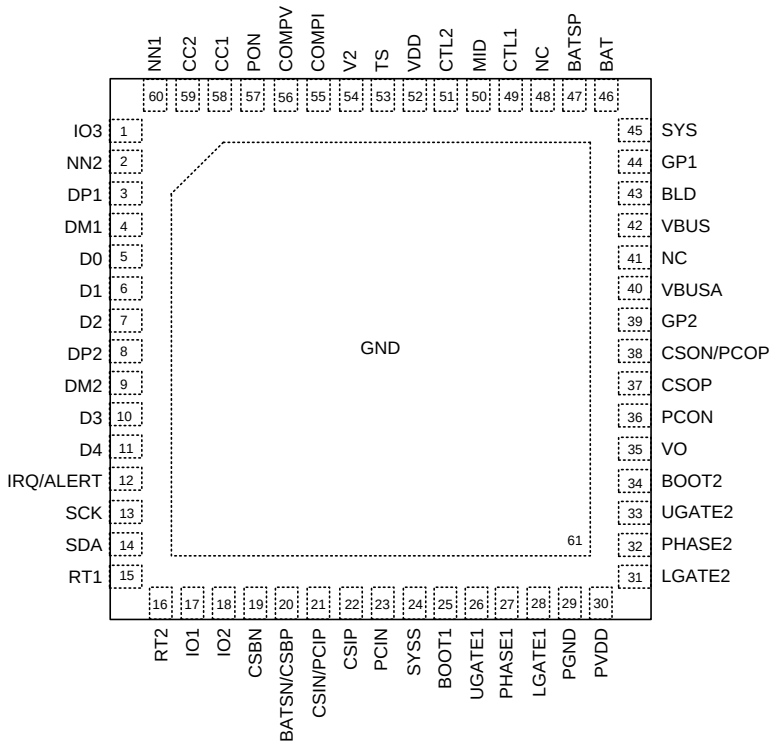
- **Communication Protocols**
  - **Support Type-C and USB Power Delivery (PD) Communication**
  - **Support Dual-Role Power (DRP) Application**
  - **Support Proprietary Protocols via DP and DM Interfaces**
- **Charging Operation for 2S to 4S Battery**
  - **CC and CV Charge, End of Charge, Re-Charge, and Charging Timeout Protection**
  - **Cell Balance Control**
- **Bi-directional Buck-or-Boost Operation :**
  - **Peak-Current Mode PWM Operation**
  - **Programmable PWM Switching Frequency**
  - **Programmable Constant Voltage and Constant Current Settings for Charger/Provider Mode Output**
  - **Pulse-Skipping Mode (PSM) for Light-Load Efficiency**
  - **Programmable Cable Voltage Drop Compensation**
- **2 Charge Pump Gate Drivers for N-MOSFETs**
- **Hardware and Firmware-Based Protections :**
  - **Adjustable Converter Input Current-Limit**
  - **Programmable Over-Voltage Protections (OVP) and Under-Voltage Protections (UVP)**
  - **Adjustable External OTP**
- **Master/Slave I^2C Interface, LED Drivers, GPIOs**
- **Built-in Bleeders for Quick VBUS Discharge**
- **Online Firmware Update via CC1/2 or Slave I^2C Interfaces**
- **WQFN-60L 7x7 Package**
- **USB PD PD3.0/PPS Certification Passed (TID 2319)**

Simplified Application Circuit



Pin Configuration

(TOP VIEW)



WQFN-60L 7x7

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

RT7885 Version Table

Version	RT7885A
Cell Balance Control	2 Cell

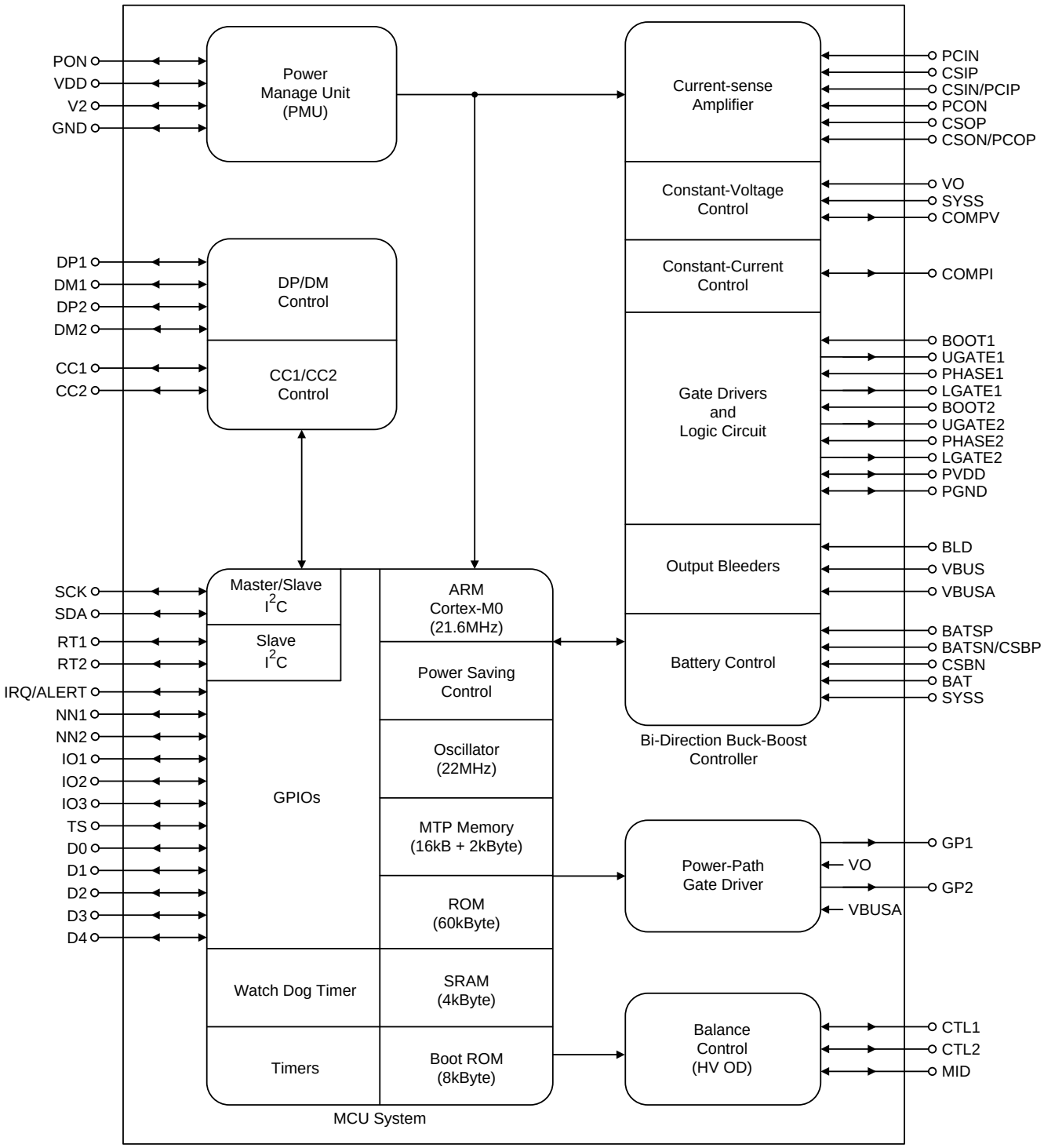
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	IO3	Open-drain/push-pull GPIO or analog input pin.
2	NN2	This pin can be set as an open-drain or push-pull GPIO pin.
3	DP1	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D+ pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin.
4	DM1	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D- pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin.
5	D0	Open-drain/push-pull GPIO or analog input pin.
6	D1	Open-drain/push-pull GPIO or analog input pin.
7	D2	Open-drain/push-pull GPIO or analog input pin.
8	DP2	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D+ pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin.
9	DM2	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. Connect this pin to D- pin of a USB connector. This pin can be set as an open-drain or push-pull GPIO pin.
10	D3	Open-drain/push-pull GPIO or analog input pin.
11	D4	Open-drain/push-pull GPIO or analog input pin.
12	IRQ/ALERT	Interrupt input/output pin. The RT7885 could do emergency control when it receives a low-level signal via this pin; an external MCU could check the slave I^2C registers to do emergency control when it receives a low-level signal via this pin. This pin can be set as an open-drain or push-pull GPIO pin.
13	SCK	Open-drain clock signal input/output pin of the Slave/Master I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
14	SDA	Open-drain data signal input/output pin of the Slave/Master I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
15	RT1	Open-drain/push-pull GPIO, analog Input or external over-temperature protection (EOTP) input pin. Connect an NTC from this pin to GND pin for the EOTP.
16	RT2	Open-drain/push-pull GPIO, analog input or external over-temperature protection (EOTP) input pin. Connect an NTC from this pin to GND pin for the EOTP.
17	IO1	Open-drain/push-pull GPIO or analog input pin.
18	IO2	Open-drain/push-pull GPIO or analog input pin.
19	CSBN	Negative input pin of the battery current-sense amplifier for battery charge/discharge current detection.

Pin No.	Pin Name	Pin Function
20	BATSN/CSBP	Negative input pin for measuring the battery voltage and positive input pin of the battery current-sense amplifier for battery charge/discharge current detection.
21	CSIN/PCIP	Positive peak-current signal input pin in PD provider operation and negative average-current signal input pin in charger operation.
22	CSIP	Positive average-current signal input pin in charger operation.
23	PCIN	Negative peak-current signal input pin in PD provider operation.
24	SYSS	Output feedback voltage input pin in charger operation. The voltage at this pin is monitored for programmable (8-bit) output under-voltage protection.
25	BOOT1	Positive power-rail pin of the 1st high-side gate driver. Connecting a bootstrap capacitor (0.1μF, typ.) between this pin and PHASE1 pin is recommended.
26	UGATE1	1st high-side gate driver output pin.
27	PHASE1	Negative power-rail pin of the 1st high-side gate driver.
28	LGATE1	1st low-side gate driver output pin.
29	PGND	Ground of the low-side gate drivers and one input pin of zero-current detection at the MOSFET (Q_B) controlled by LGATE1. Connecting this pin to source of the Q_B through a dedicated track is recommended.
30	PVDD	Bias voltage (5V typ.) input pin of low-side gate drivers. Connecting an external MLCC (1μF) from this pin to PGND pin is recommended.
31	LGATE2	2nd low-side gate driver output pin.
32	PHASE2	Negative power-rail pin of the 2nd high-side gate driver.
33	UGATE2	2nd high-side gate driver output pin.
34	BOOT2	Positive power-rail pin of the 2nd high-side gate driver. Connecting a bootstrap capacitor (0.1μF, typ.) between this pin and PHASE2 pin is recommended.
35	VO	Output feedback voltage input pin. The voltage at this pin is monitored for programmable (8-bit) output under-voltage protection.
36	PCON	Negative peak-current signal input pin in charger operation.
37	CSOP	Positive average-current signal input pin in PD provider operation and negative average-current signal input pin in charger operation.
38	CSON/PCOP	Negative average-current signal input pin in PD provider operation and positive peak-current signal input pin in charger operation.
39	GP2	Charge-pump gate driver output pin. It drives N-channel power MOSFETs to turn on/off the power-path connected with VO pin.
40	VBUSA	USB-A VBUS voltage input pin. The voltage at this pin is monitored for programmable (8-bit) USB-A VBUS over-voltage protection.
41, 48	NC	No internal connection.
42	VBUS	USB-C VBUS voltage input pin and input pin of the VBUS-to-VDD linear regulator. The voltage at this pin is monitored for programmable (8-bit) USB-C VBUS over-voltage protection.
43	BLD	Output pin of output bleeder. A pull-low n-channel MOSFET is built in for discharging the charge in output capacitors of the PWM converter. Connect this pin to converter output via an external resistor.
44	GP1	Charge-pump gate driver output pin. It drives N-Channel power MOSFETs to turn on/off the power-path connected with VO pin.
45	SYS	SYS pin.

Pin No.	Pin Name	Pin Function
46	BAT	Input pin of the BAT-to-VDD linear regulator.
47	BATSP	Positive input pin for measuring the battery voltage.
49	CTL1	High-voltage open-drain output and voltage-sensing input pin.
50	MID	Low-voltage open-drain output and voltage-sensing input pin.
51	CTL2	High-voltage open-drain output and voltage-sensing input pin.
52	VDD	Output pin of the BAT-to-VDD and VBUS-to-VDD linear regulator. Connecting an external MLCC (1μF) from this pin to GND pin is recommended.
53	TS	Voltage-sensing input pin.
54	V2	Output pin of the internal 1.8V linear regulator which supplies power for digital circuits. Connecting this pin with a 1μF MLCC is recommended.
55	COMPI	Constant-current (CC) loop error amplifier output pin. Connect an external RC network between this pin and GND for constant-current loop feedback compensation.
56	COMPV	Constant-voltage (CV) loop error amplifier output pin. Connect an external RC network between this pin and GND for CV loop feedback compensation.
57	PON	Power-on signal input pin. Pulling low this pin enables VDD and V2 linear regulators in standby mode.
58	CC1	Input/Output pin of the first configuration channel. Generally, connect this pin to USB-C CC1 terminal.
59	CC2	Input/Output pin of the second configuration channel. Generally, connect this pin to USB-C CC2 terminal.
60	NN1	This pin can be set as an open-drain or push-pull GPIO pin.
61	GND (Exposed-Pad)	Ground pad. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT7885 is a versatile USB Type-C Power Delivery (USB-C PD) controller adopting Buck-Boost PWM control scheme and highly integrating functions specially for power bank applications. This solution integrates four main functional blocks : MCU System, bidirectional PWM Buck-Boost Controller, Protections and CC1/2 Functions.

The MCU System embeds an ARM Cortex™-M0 MCU, multi-time programming (MTP) memory, ROM, SRAM, ADC (analog to digital converter), I^2C interfaces (slave and master) and GPIO (general purpose input or output) pins. The MCU System is programmed to perform power controls, customized functions, as a policy engine and a device policy manager. The GPIO pins can be used to control high-speed multiplexers or other customized functions.

The "Bidirectional PWM Buck-Boost controller" consists of an AnyVolt® constant-voltage (CV) control circuit, an AnyCurrent™ constant-current (CC) control circuit, an output current-sense amplifier, built-in gate drivers, charge-pump gate drivers and output bleeders. Generally, either the CV or the CC control circuit regulates the voltage or current for charger and provider mode through peak-current mode PWM operation. The diode emulation function and the pulse-skipping mode (PSM) are built in to improve power efficiency at light loads. The input/output current-sense amplifier (OCS-AMP) allows current-sense resistors as low as 5mΩ to 15mΩ for reducing power loss.

Not like P-channel MOSFET with higher cost, the charge-pump driver utilizes cost-effective N-channel MOSFETs for on/off control of output power-path. The output bleeders at BLD pins can be turned on to discharge output voltage during negative transition, hard reset process, or removal of USB-C connector.

The PD Safe® power delivery operation consists of over-voltage protection (OVP), under-voltage protection (UVP), and output CC regulation for provider output. The protection levels of the OVP and UVP can be set dynamically for each output voltage. In addition, the CC regulation level is also programmable and adaptive to the level of full-load current to full load current level.

The "CC1/2 Functions" block consists of the physical layer, three selectable levels of the pull-up current sources Ip (instead of resistors Rp), a controllable pull-down resistor Rd.

Under-Voltage Lockout (UVLO)

The RT7885 UVLO function continuously monitors bias voltages at the VDD, and V2 pins. When the supply voltages rise above the respective rising UVLO thresholds, the controller starts to work. The controller also monitors the bias voltage at the PVDD pin for UVLO function. When the supply voltages drop under UVLO thresholds, MCU or PWM controllers will be in "Under-Voltage Lockout" state to prevent any undesirable operation.

Pulse-Skipping Mode (PSM) with Diode Emulation

When a switch-mode converter operates in light load condition, most power loss is caused by switching losses. To reduce switching loss in light load condition, the switching frequency needs to be reduced, and this can be accomplished by entering pulse-skipping mode (PSM) and discontinuous conduction mode (DCM).

A Diode Emulation Mode (DEM) is also a necessary function to avoid delivering energy from converter output to converter input during dynamic output voltage control. The DEM function is equipped with two zero-current detection (ZCD) circuits for the low-side and high-side MOSFETs respectively controlled by the LGATE1 and UGATE2 pins: The Source-to-Drain voltage (V_{SDB}, detected via PGND and PHASE1 pins) of the low-side MOSFET is compared with a zero-current threshold (V_{TH_ZCDB}). When the V_{SDB} drops below the V_{TH_ZCDB} voltage, the RT7885 turns off the low-side MOSFET thereby avoiding reverse inductor current. In DEM operation, the behavior of the low-side MOSFET resembles a diode. The second ZCD circuit compares the Source-to-Drain voltage (V_{SDD}, detected via PHASE2 and PCON pins) of the high-side MOSFET with a zero-current threshold (V_{TH_ZCDD}) to achieve the DEM function.

Cable Voltage Drop Compensation (CDC)

In a power delivery system with both a Provider and a Consumer, the Provider with the RT7885 AnyVolt®

feature can slightly adjust its CV output voltage to compensate voltage drop across the cable. A PD controller of the Consumer can request higher VBUS voltage from the Provider through PD communication to achieve an accurate application voltage.

VBUS/VBUSA/SYSS Over-Voltage Protection (VBUS/VBUSA/SYSS OVP)

The RT7885 features VBUS/VBUSA/SYSS over-voltage protections for bidirectional PWM applications. When a fault occurs and the voltage on each pin exceeds its OVP threshold voltage, the PWM controller is then turned-off. The OVP threshold voltage for each pin is programmable to meet various application requirements.

VO Under-Voltage Protection (VO UVP)

The RT7885 features the VO under-voltage protection. When a fault occurs and the voltage for each pin falls below its UVP threshold voltage, the PWM controller is turned off. The UVP threshold voltage for each pin is programmable to meet various application requirements.

AnyCurrent™ Constant-Current (CC) Regulation

Robustness is essential in USB PD system operation, therefore the AnyCurrent™ CC regulation is adopted which allows one to set the most suitable CC level for a PD system. In addition, the RT7885 integrates a current-sense amplifier to sense output current for CC regulation in provider mode. The amplifier will accurately sense the current-sense voltage between the CSOP and CSON pins. The recommended current-sense voltage range for CC regulation is from 10mV to 58mV which is programmed by an internal 9-bit DAC with 0.1174mV/step resolution.

Power-Path Gate Driver for Driving N-Channel MOSFETs

The RT7885 integrates power-path gate drivers to control external output blocking MOSFETs between the output of the PWM converter and the USB-C VBUS terminal. Built-in charge pumps are employed to supply the gate driver to switch the external N-channel power MOSFETs, by which a power system will receive the benefit of cost-effectiveness with comparing to the P-channel MOSFETs used in counterparts.

Average Input Current Regulation (AICR)

The RT7885 provides an average input current regulation control loop for the charger mode. The control loop will adjust the charger current with limiting the charger input current not to exceed a certain level. However, the input current level can be set based on the input source current capability.

Minimum Input Voltage Regulation (MIVR)

For input voltage regulation, the RT7885 possesses a control loop to obtain the minimum input voltage regulation in the charger mode. In practice, it is not always clear what kind of power source is connected, it would happen that the charger draws too much current from the power source, which then would cause an overload of system. To avoid this condition, the control loop could be activated which monitors the charger input voltage and decreases the input charge current when the input voltage drops below a certain level.

Online Firmware Update via CC1/CC2 or Slave I^2C Interface

The embedded MTP memory allows the RT7885's firmware to be updated by an EC (Embedded Controller) or AP (Application Processor) through the I^2C slave interface.

Moreover, the RT7885 provides firmware programmable design features, which greatly eases the design efforts during product development stage. End users are also allowed to update the firmware through CC1/CC2.

Absolute Maximum Ratings (Note 1)

- V2 to GND ---------- –0.3V to 2.5V
- VDD to GND, PVDD to GND ---------- –0.3V to 6.5V
- NN1, NN2 to GND ---------- –0.3V to 6.5V
- VBUS, VBUSA, CSOP, CSON/PCOP, PCON, VO, BLD to GND ---------- –0.3V to 25V
- SYSS, SYS, CSIP, CSIN/PCIP, PCIN, BAT, BATSP, CTL1, CTL2 to GND ---------- –0.3V to 22V
- CSOP to CSON Voltage ($V_{CSOP-CSON}$), PCOP to PCON Voltage ($V_{PCOP-PCON}$) ---- –5V to 5V
- CSIP to CSIN Voltage ($V_{CSIP-CSIN}$), PCIP to PCIN Voltage ($V_{PCIP-PCIN}$) ---------- –5V to 5V
- GP1, GP2 to GND ---------- –0.3V to 33V
- PON, COMPV, COMPI, BATSN/CSBP, CSBN to GND ---------- –0.3V to 6.5V
- MID to GND ---------- –0.3V to 6.5V
- I^2C Pins (SCK, SDA, IRQ/ALERT), DPDM Pins (DP1, DM1, DP2, DM2) ---------- –0.3V to 6.5V
- GPIO Pins (IO1, IO2, IO3, RT1, RT2, TS, D0, D1, D2, D3, D4) to GND ---------- –0.3V to 6.5V
- CC1, CC2 to GND ---------- –0.3V to 25V
- BOOT1/2 to PHASE1/2 ($V_{BOOT-PHASE}$) ---------- –0.3V to 6.5V
- UGATE1/2 to PHASE1/2 ---------- –0.3V to $V_{BOOT-PHASE}$ + 0.3V
- PHASE1 to GND (DC) ---------- –0.3V to 22V
  (<20ns) ---------- –5V to 27V
- PHASE2 to GND (DC) ---------- –0.3V to 25V
  (<20ns) ---------- –5V to 30V
- LGATE1/2 to PGND ---------- –0.3V to V_{PVDD} + 0.3V
- PGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-60L 7x7 ---------- 3.92W
- Package Thermal Resistance (Note 2)
  WQFN-60L 7x7, θ_{JA} ---------- 25.5°C/W
  WQFN-60L 7x7, θ_{JC} ---------- 6.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 1.5kV

Recommended Operating Conditions (Note 4)

- PWM Converter Input Voltage (V_{BUS}) Range
  in Charger (PD Consumer) Operation ---------- 3V to 22V
- PWM Converter Output Voltage (V_{SYS}) Range in Charger Operation ---------- 3V to 18V
- PWM Converter Input Voltage (V_{SYS}) Range in PD Provider Operation ---------- 3V to 18V
- PWM Converter Output Voltage (V_{BUS}) Range in PD Provider Operation ---------- 3V to 22V

- VDD Supply Voltage, VDD ---------- 3V to 5.5V
- PVDD Supply Voltage, PVDD ---------- 4.5V to 5.5V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°C

Electrical Characteristics

(V_{VDD} = V_{PVDD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD and V2 Linear Regulators (VDD LDO and V2 LDO), and Under-Voltage Lockout (UVLO)							
VDD Output Voltage (5.0V Typ.)	V_{REG_VDD}	I_O = 0mA to 60mA	V_{VBUS} = 0V, V_{BAT} ≥ 5.5V or V_{VBUS} ≥ 5.5V, V_{BAT} = 0V	4.8	5.0	--	V
VDD Short-Circuit Current	I_{SC_VDD}			70	125	--	mA
V2 Output Voltage	V_{REG_V2}	I_{V2} = 0A		1.6	1.8	2.0	V
V2 Short-Circuit Current	I_{SC_V2}	V2 = GND		20	50	--	mA
VDD UVLO Voltage Threshold		VDD rising, not in deep-green mode		--	3	3.2	V
VDD UVLO Voltage Hysteresis				--	200	--	mV
V2 UVLO Voltage Threshold		V_{V2} rising (Note 5)		--	1.4	--	V
V2 UVLO Voltage Hysteresis		(Note 5)		--	150	--	mV
PVDD UVLO Threshold		V_{PVDD} rising		--	4	4.2	V
PVDD UVLO Hysteresis				--	200	--	mV
VBUS and BAT Operating Currents and Leakage Currents							
Input Current in Standby Mode		V_{BAT} = 12V, VDD LDO = off, cable detections = on		--	100	150	μA
Input Current in Green Mode		V_{BAT} = 12V, VDD LDO = on, cable detections = on, in PSM without switching, Digital output pins = open	MCU = on, Memory = off	--	5	8	mA
Input Current in Normal Mode			MCU = on, Memory = on	--	10	15	mA
MCU Section							
MCU Clock Frequency	f_{MCU}			19.4	21.6	23.8	MHz
PWM Controller – Programmable Oscillator and Maximum On-Time							
Oscillator Frequency Range	f_{OSC}	Programmable (9-bit)		200	--	1000	kHz
Oscillator Frequency Accuracy				–10	--	10	%

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Maximum On-time Range	t_{ON_MAX}	Programmable (7-bit), 46.3ns/step		0.32	--	5.88	μs
PWM Controller – Constant-Voltage(CV) and Constant-Current(CC) Output Levels in PD Provider Operation							
CV Regulated Voltage Range at VO Pin	V_{REG_VO}	11-bit DAC, 10.986mV/step, R_{ratio_VO} = 0.08V/V		3	--	22	V
CV Regulated Voltage Accuracy at VO Pin		V_O = 5V/9V/12V/15V/20V		–1.5	--	1.5	%
CC Regulated Voltage Range between CSOP and CSON Pins	V_{REF_CC1}	Programmable (9-bit), V_{CSOP} and V_{CSON} > 3V	117.2μV/step, G_{CSA_VBUS} = 20	3	--	58	mV
CC Reference Voltage Accuracy between CSOP and CSON Pins		V_{REF_CC1} = 10mV/30mV/50mV, G_{CSA_VBUS} = 20		–1	--	1	mV
PWM Controller – Constant-Voltage(CV) and Constant-Current(CC) Output Levels in Charger Operation							
CV Regulated Voltage Range at SYSS Pin	V_{REG_SYSS}	11-bit DAC, 8.789mV/step, R_{ratio_SYSS} =0.1V/V		3	--	17.5	V
CV Regulated Voltage Accuracy at SYSS Pin		V_{SYSS} = 12.9V		–1	--	1	%
CC Regulated Voltage Range between CSIP and CSIN Pins	V_{REF_CC2}	Programmable (9-bit), V_{CSIP} and V_{CSIN} > 3V	117.2μV/step, G_{CSA_SYSS} = 20	3	--	58	mV
CC Regulated Voltage Accuracy between CSIP and CSIN Pins		V_{REF_CC2} = 10mV/30mV/50mV, G_{CSA_SYSS} = 20		–1	--	1	mV
Minimum Regulated Voltage at VO Pin	V_{REF_MINVO}	7-bit DAC, 146.5mV/Step, R_{ratio_VO} = 0.08V/V		4	--	18.5	V
Minimum Regulated Voltage Accuracy at VO Pin		V_{REG_MINVO} = 8.06V		–250	--	250	mV
Sinking CC Regulated Voltage Range between CSON and CSOP Pins	V_{REF_CC4}	Programmable (9-bit), V_{CSOP} and V_{CSON} > 3V	117.2μV/step, G_{CSA_VBUS} = 20	3	--	54	mV
Sinking CC Regulated Voltage Accuracy between CSON and CSOP Pins		V_{REF_CC4} = 10mV/30mV/50mV, G_{CSA_VBUS} = 20		–2	--	2	mV
PWM Controller – Constant-Voltage(CV) and Constant-Current(CC) Error Amplifiers							
Trans-Conductance of COMPV Error Amplifier	Gmv	I_{COMPV} = ±20μA		382	550	718	μA/V
COMPV Maximum Output Voltage		COMPV = open		3.2	3.5	3.8	V
Trans-Conductance of COMPI Error Amplifier	Gmi	I_{COMPI} = ±20μA		382	550	718	μA/V
COMPI Maximum Output Voltage		COMPI = open		3.2	3.5	3.8	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PWM Controller – Input Current Comparison							
PCIP-to-PCIN or PCOP-to-PCON Maximum Input Current-Sense Voltage Threshold Range	V_{TH_CSMAX}	Programmable (5-bit), 5.357mV/step		--	--	140	mV
Leading Edge Blanking(LEB) Time of Input Peak/Over-Current Comparator	t_{LEBA}	From V_{UGATE1} rising edge (PD provider) or V_{UGATE2} rising edge (charger), programmable (2bit + 1bit).	01 +1	--	400	--	ns
LEB Time of Input Peak/Over-Current Comparator	t_{LEBC}	From V_{LGATE2} rising edge (PD provider) or V_{LGATE1} rising edge (charger), programmable (2bit).	10	--	250	--	ns
PWM Controller – Pulse-Skipping Mode(PSM) Operation with Zero-Current Detection(ZCD)							
PSM Voltage Threshold Range at COMPV or COMPI Pin	V_{TH_PSM}	Programmable (6-bit), 31.25mV/step		0.4	--	2.2	V
MOS-D ZCD Voltage Threshold	V_{TH_ZCDD}	To compare the PHASE2-to-PCON voltage (PD provider) or PHASE1-to-PCIN voltage (charger). (Note 5)		--	4	--	mV
MOS-B ZCD Voltage Threshold	V_{TH_ZCDB}	To compare the PGND-to-PHASE1 voltage (PD provider) or PGND-to-PHASE2 voltage (charger). (Note 5)		--	4	--	mV
MOS-D ZCD Leading-Edge Blanking (LEB) Time	t_{LEBD}	Programmable, from V_{UGATE2} rising edge (PD provider) or V_{UGATE1} rising edge (charger). (Note 5)	10	--	350	--	ns
MOS-B ZCD LEB Time	t_{LEBB}	Programmable, from V_{LGATE1} rising edge (PD provider) or V_{LGATE2} rising edge (charger). (Note 5)	10	--	250	--	ns
PWM Controller – Gate Drivers							
UGATE1/2 Pull-high Resistance		$V_{BOOT1/2-PHASE1/2}$ = 5V, $V_{BOOT1/2-UGATE1/2}$ = 0.1V		--	1.7	--	Ω
UGATE1/2 Pull-low Resistance		$V_{UGATE1/2-PHASE1/2}$ = 0.1V		--	0.8	--	Ω
LGATE1/2 Pull-high Resistance		V_{PVDD} - $V_{LGATE1/2}$ = 0.1V		--	1.7	--	Ω
LGATE1/2 Pull-low Resistance		$V_{LGATE1/2}$ = 0.1V		--	0.8	--	Ω
Dead-Time at UGATE1 Falling Edge				--	40	--	ns
Dead-Time at LGATE1 Falling Edge		(Note 5)		--	40	--	ns
Dead-Time at LGATE2 Falling Edge		(Note 5)		--	40	--	ns

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Dead-Time at UGATE2 Falling Edge				--	40	--	ns
System Protections – Over-Voltage, Under-Voltage, Over-Current and External Over-Temperature Protections (OVP, UVP, OCP and EOTP)							
VBUS/VBUSA/VO OVP Voltage Threshold Range	V_{TH_OV1}	Programmable (8-bit), 97.656mV/step at VBUS, VBUSA or VO pin, R_{ratio_VO} = 0.08V/V		5.47	--	24.9	V
VBUS/VBUSA/VO OVP Voltage Threshold Accuracy		V_{TH_OV1} = 5.96V/24V		–5	--	5	%
PCON/PCIN OVP Voltage Threshold	$V_{TH\_PCIONOV}$	V_{PCON} =15V, R_{ratio} = 0.08, V_{PCIN} = 12V, R_{ratio} = 0.1	00	105	110	115	%
			01	110	115	120	
			10	115	120	125	
			11	120	125	130	
VO/SYSS/BATSP UVP Voltage Threshold Range	V_{TH_VOUV}	Programmable (8-bit), 97.656mV/step, R_{ratio_VO} = 0.08V/V		3.03	--	20.02	V
	V_{TH_SYSSUV}	Programmable (8-bit), 78.125mV/step, R_{ratio_SYSS} = 0.1V/V		3.03	--	17.97	V
	$V_{TH\_BATSPUV}$	Programmable (8-bit), 55.804mV/step, R_{ratio_BATSP} = 0.14V/V		3.03	--	14.28	V
VO/SYSS/BATSP UVP Voltage Threshold Accuracy		V_{TH_VOUV} = 3.03V/20.02V		–5	--	5	%
		V_{TH_SYSSUV} = 3.03V/17.97V		–5	--	5	
		$V_{TH\_BATSPUV}$ = 3.03V/14.28V BATSP pin to BATSN pin		–6.5	--	6.5	
VBUSA OVP Voltage Threshold Range	V_{TH_OV2}	Programmable (7-bit), 117.19mV/step at VBUSA pin, R_{ratio_VBUSA} = 0.08V/V		5.51	--	14.88	V
VBUSA OVP Voltage Threshold Accuracy		V_{TH_OV2} = 5.51V/14.88V		–5	--	5	%
CTL2 OVP Voltage Threshold	V_{TH_OV3}	Programmable	00	--	5.83	--	V
			01	--	6.00	--	
			10	--	6.17	--	
			11	--	6.33	--	
CTL2 OVP Voltage Threshold Accuracy				–5	--	5	%
VBUSA UVP Voltage Threshold	--	V_{VBUSA} falling		2.85	3.00	3.15	V
CTL2 UVP Voltage Threshold	--	V_{CTL2} falling		2.85	3.00	3.15	V
RT1/2 Current Source for EOTP			11	--	100	--	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
RT1/2 Current Source for EOTP Accuracy		RT1/2 Current Source = 100μA		–5	--	5	%
RT1/2 Voltage Detection Range		11-bit ADC, Resolution = 1.318mV/step		0.1	--	2.7	V
TS Voltage Detection Range		11-bit ADC, Resolution = 3.296mV/step		0.25	--	5.5	V
USB PD Controller – CC1/2 Voltage Detections, BMC Transmitter/Receiver							
CC1/2 Pull-Up Current Source – 1	Ip1	For Default USB Power		--	80	--	μA
CC1/2 Pull-Up Current Source – 2	Ip2	For 1.5A @ 5V		--	180	--	μA
CC1/2 Pull-Up Current Source – 3	Ip3	For 3.0A @ 5V		--	330	--	μA
CC1/2 Pull-Down Resistor	Rd			4.59	5.1	5.61	kΩ
CC1/2 Maximum Output Voltage	--	CC1/2 = open		--	V_{VDD} - 0.7V	--	V
Transmitter High-Level Output Voltage Range	--			1.05	--	1.2	V
Transmitter Low-Level Output Voltage Range	--			0	--	75	mV
Receiver High-Level Input Voltage Range	--	Programmable	00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Receiver Low-Level Input Voltage Range	--	Programmable	00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
Rising Time of the Transmitter Output Voltage	--	From 10% to 90%, C_L = 200pF to 600pF		300	--	--	ns
Falling Time of the Transmitter Output Voltage	--	From 90% to 10%, C_L = 200pF to 600pF		300	--	--	ns
NN1/2 Current-Limit Threshold	--	NN1/2 = GND		--	50	--	mA
DPDM Interface (DP1, DM1, DP2 and DM2 Pins) in Source Role Operation							
On-Resistance of DP1/2-to- DM1/2 Switch	--	For BC1.2 and QC		--	--	40	Ω
Internal Pull-High Resistance	R_{UP_DPDM}			7.5	10	12.5	kΩ
Internal Pull-Low Resistance	R_{DWN_DPDM}			16	20	24	kΩ

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High-Level Output Voltage	V_{OH_DPDM}	VDD = 5V, R_L = 15kΩ	00	V_{VDD} - 0.5	V_{VDD} - 0.3	V_{VDD} - 0.1	V
			01	3.1	3.3	3.5	
			10	1.6	1.8	2.0	
Low-Level Output Voltage	V_{OL_DPDM}	VDD = 5V, R_L = 15kΩ		--	--	0.3	V
Voltage Offset Selection	V_{IN_LEV}	Programmable, for SCP	1	--	0.4	--	V
Receiver Upper Input Voltage Threshold	V_{REF2H_DPDM}	Programmable, pin voltage is rising, for SCP	00	0.7 + V_{IN_LEV}	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	V
			01	1.3 + V_{IN_LEV}	1.4+ V_{IN_LEV}	1.5 + V_{IN_LEV}	V
			10	1.8 + V_{IN_LEV}	1.9+ V_{IN_LEV}	2.0 + V_{IN_LEV}	V
			11	2.0 + V_{IN_LEV}	2.1+ V_{IN_LEV}	2.2 + V_{IN_LEV}	V
Receiver Lower Input Voltage Threshold	V_{REF2L_DPDM}	Programmable, pin voltage is falling, for SCP	00	0.5 + V_{IN_LEV}	0.6+ V_{IN_LEV}	0.7 + V_{IN_LEV}	V
			01	1.0 + V_{IN_LEV}	1.1+ V_{IN_LEV}	1.2 + V_{IN_LEV}	V
			10	1.7 + V_{IN_LEV}	1.8+ V_{IN_LEV}	1.9 + V_{IN_LEV}	V
			11	1.8 + V_{IN_LEV}	1.9+ V_{IN_LEV}	2.0 + V_{IN_LEV}	V
Charge-Pump Gate Drivers (GP1 and GP2) and Bleeders							
On resistance of the GP1/2 Pull-Low MOSFET	--			--	175	--	Ω
Maximum GP1 Voltage	--	V_{VO} = 20V, $R_{GP1\text{-}to\text{-}GND}$ ≥ 2MΩ		V_{VO} + 2 x V_{VDD} - 5V	V_{VO} + 2 x V_{VDD} - 3V	V_{VO} + 2 x V_{VDD} - 1V	V
Maximum GP2 Voltage	--	V_{VBUSA} = 12V, $R_{GP2\text{-}to\text{-}GND}$ ≥ 2MΩ		V_{VBUSA} + 2 x V_{VDD} - 5V	V_{VBUSA} + 2 x V_{VDD} - 3V	V_{VBUSA} + 2 x V_{VDD} - 1V	V
On-Resistance of the BLD Pull-Low MOSFET	--	Pull-low NMOS is on, sinking I_{BLD} = 10mA		--	30	40	Ω
VBUS Pull-Low Resistance	--	Pull-low NMOS is on, V_{VBUS} = 5V		--	1.2	2	kΩ
VBUSA Pull-Low Resistance	--	Pull-low NMOS is on, V_{VBUSA} = 5V		--	1.2	2	kΩ
Digital Input and Output – I^2C Pins (SCK, SDA, ALERT/IRQ) and GPIO Pins (IO1 to IO3, D0 to D4, RT1 to RT2, TS and NN1 to NN2)							
I^2C/GPIO High-Level Input Voltage Range	--	For the pins configured as input pins		1.5	--	--	V
I^2C/GPIO Low-Level Input Voltage Range	--	For the pins configured as input pins		--	--	0.4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I^2C/GPIO High-Level Output Voltage	--	Sourcing current = 2mA, for the pins configured as push-pull output pins.	--	V_{VDD} - 0.8	--	V
I^2C/GPIO Low-Level Output Voltage	--	Sinking current = 2mA	--	--	0.3	V
Digital Input and Output – Push-Button Input and Cell Balance Control						
PON Internal Pull-high Voltage	--	PON = open	--	V_{VDD} - 0.7V	--	V
PON Threshold Voltage	--	(Note 5)	--	1	--	V

Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

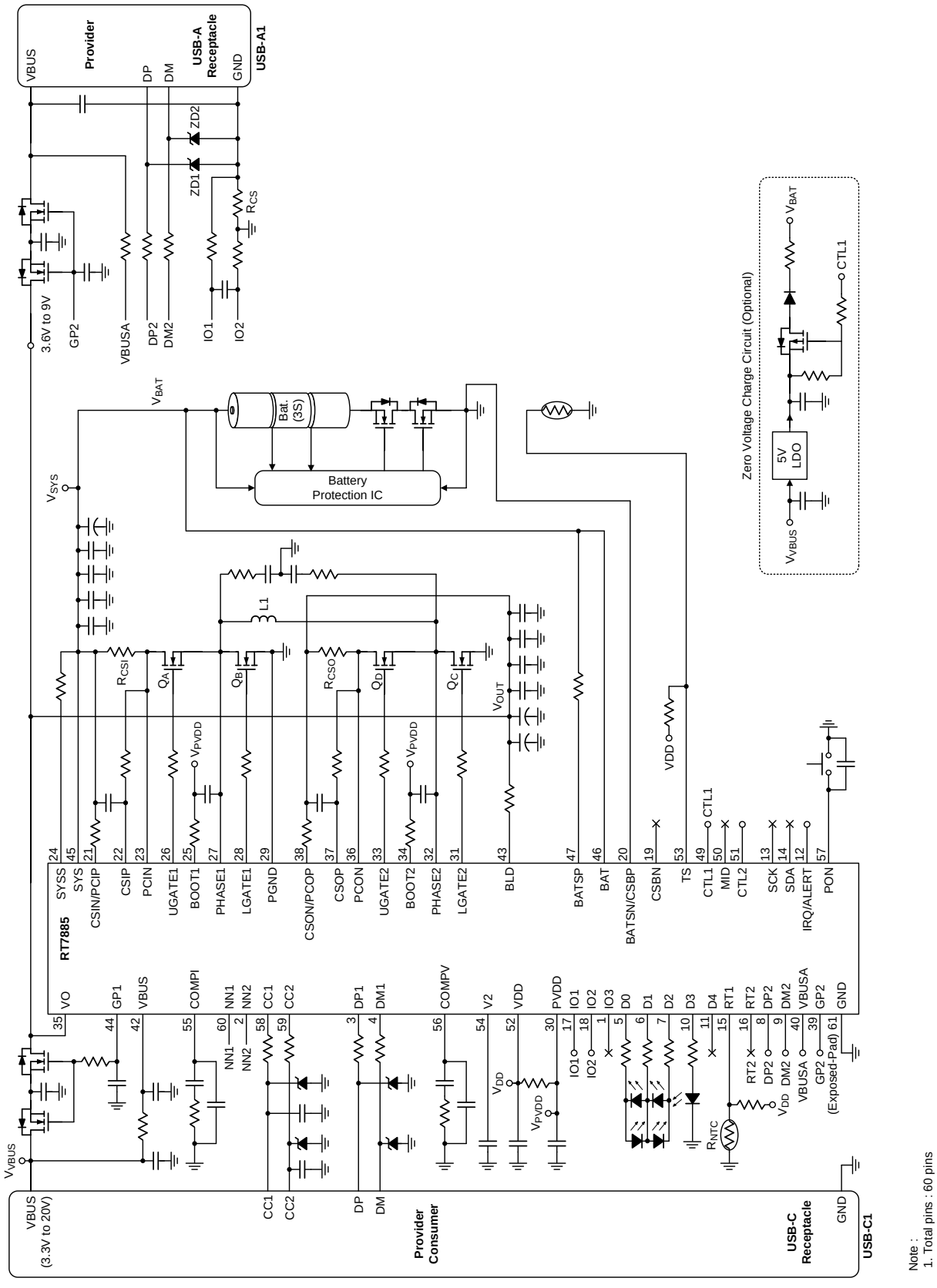
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

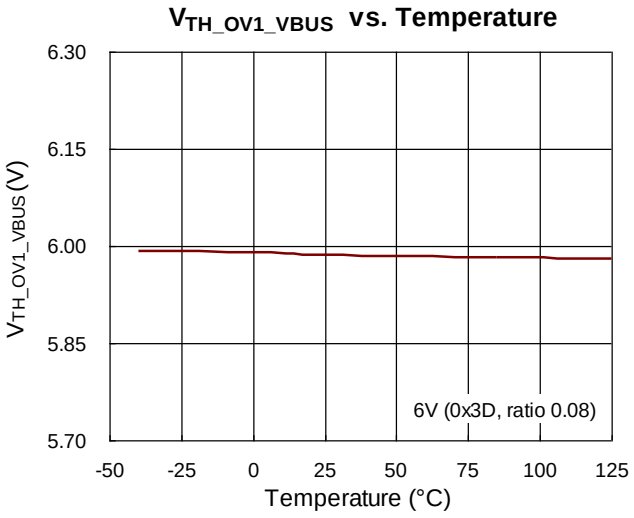
Note 5. Guaranteed by design.

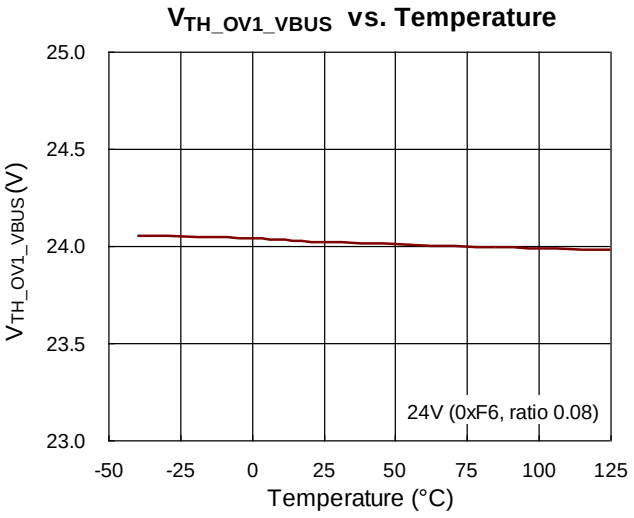
Typical Application Circuit

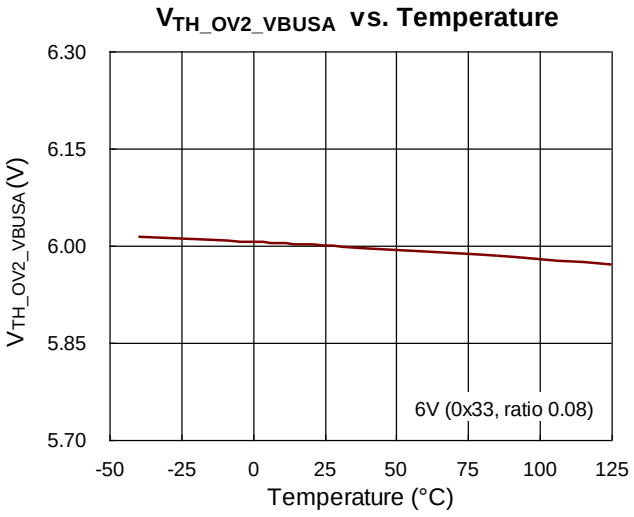
1C1A Application Circuit

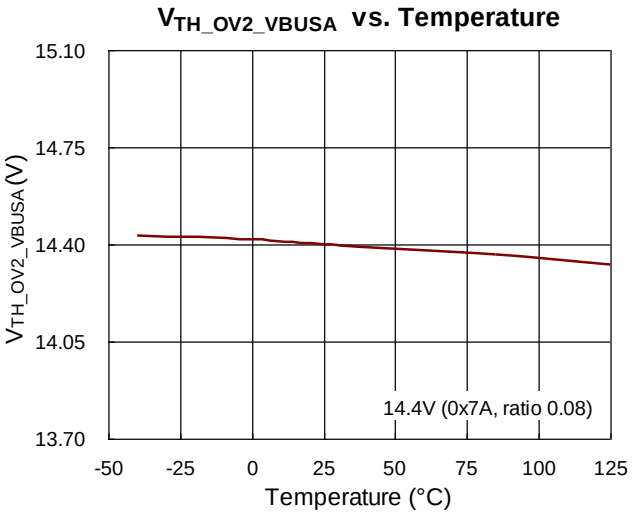


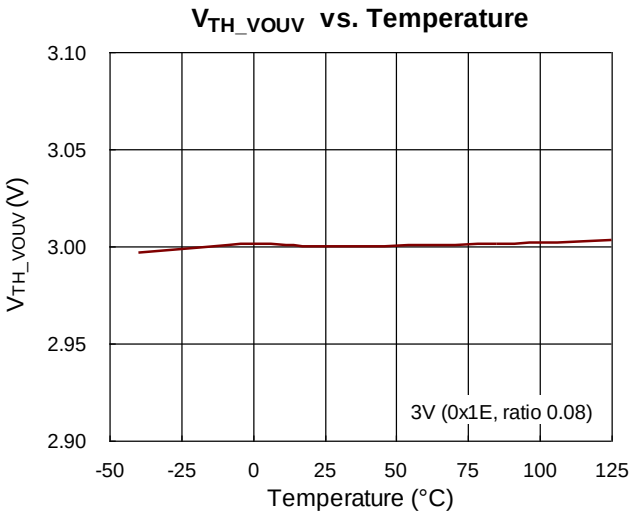
Typical Operating Characteristics

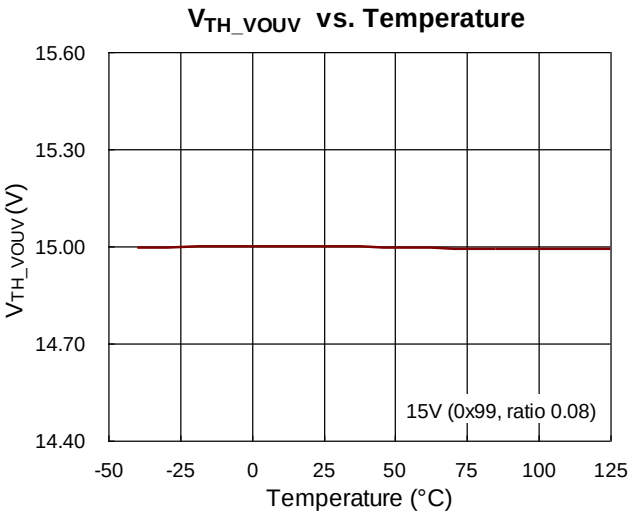


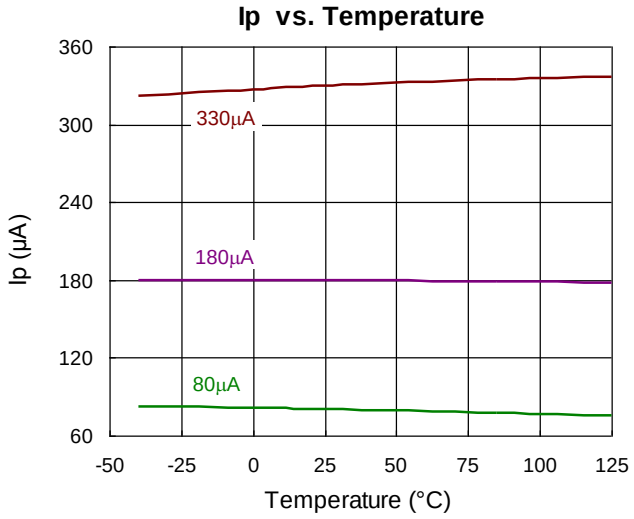


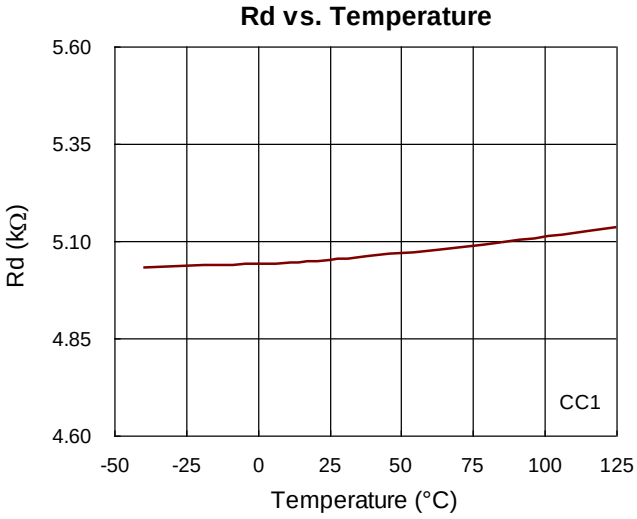


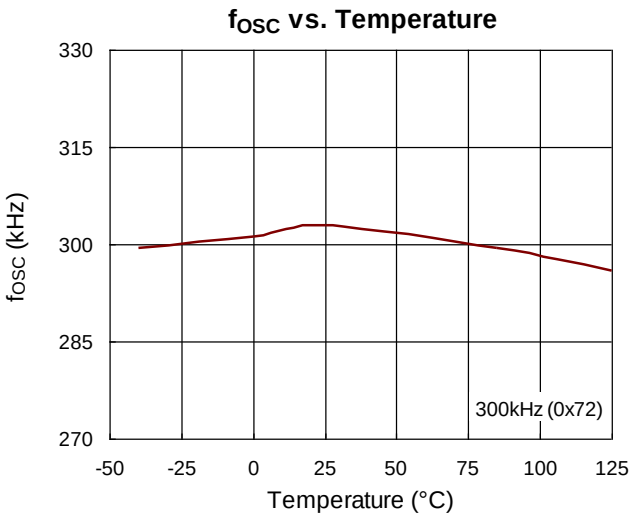


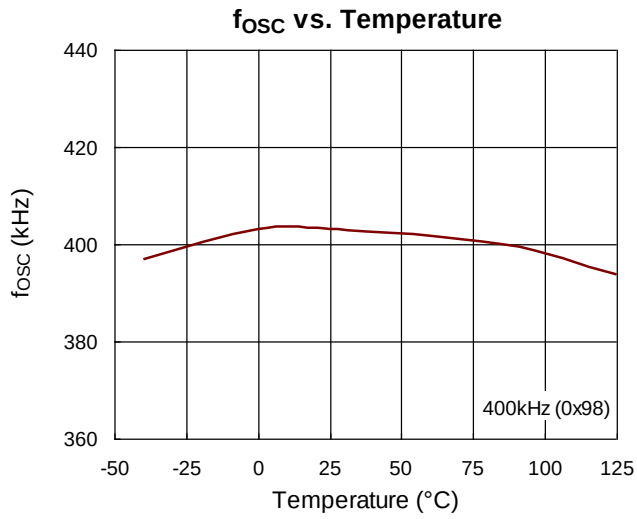


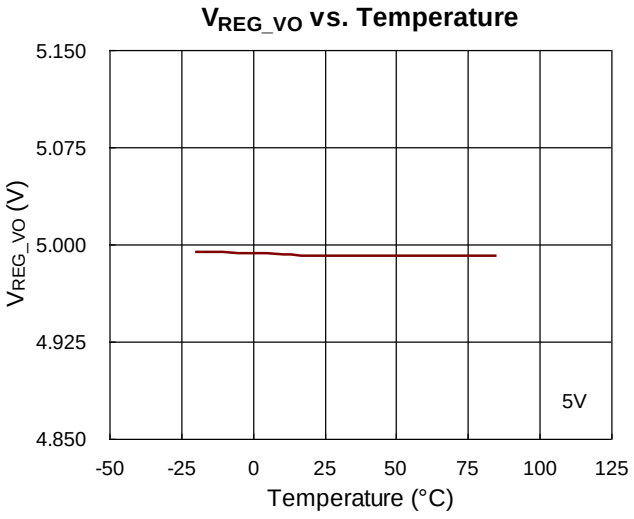


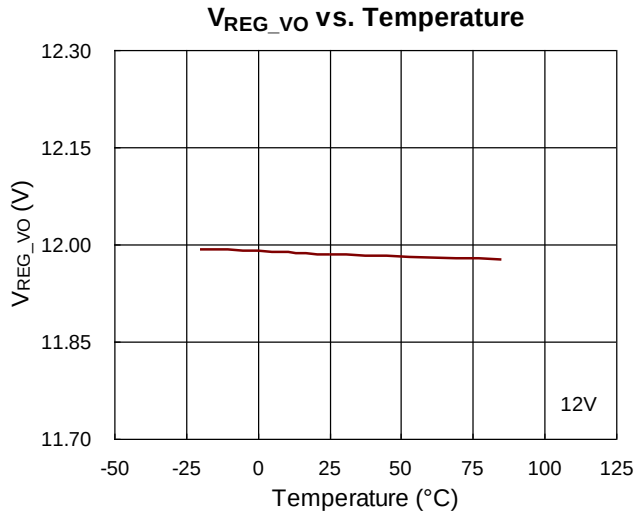




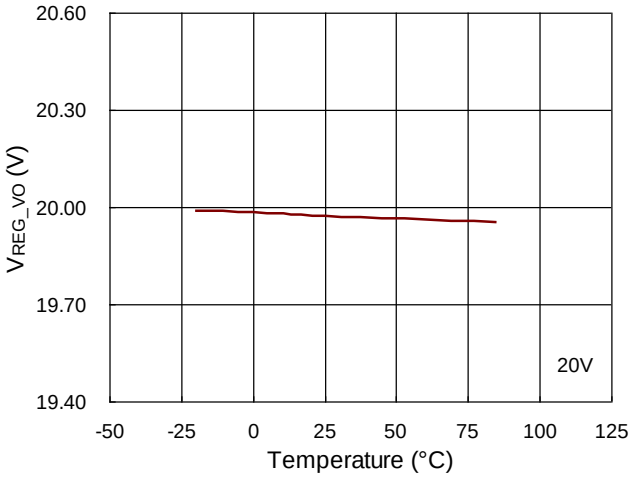




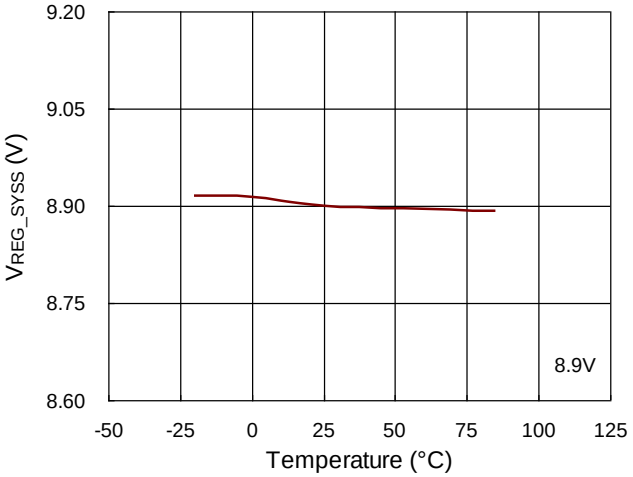




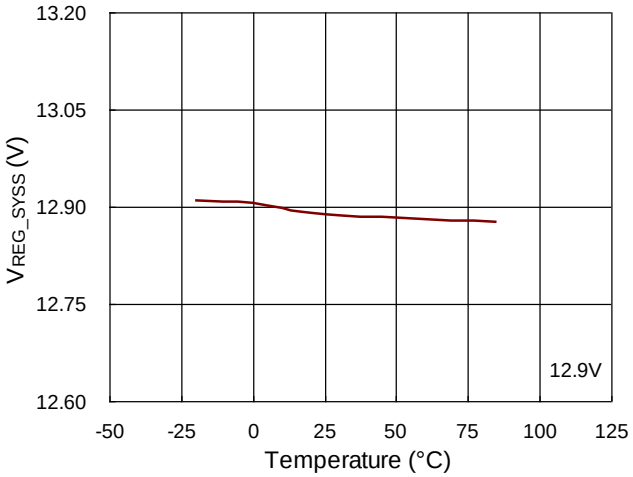
V_{REG_VO} vs. Temperature



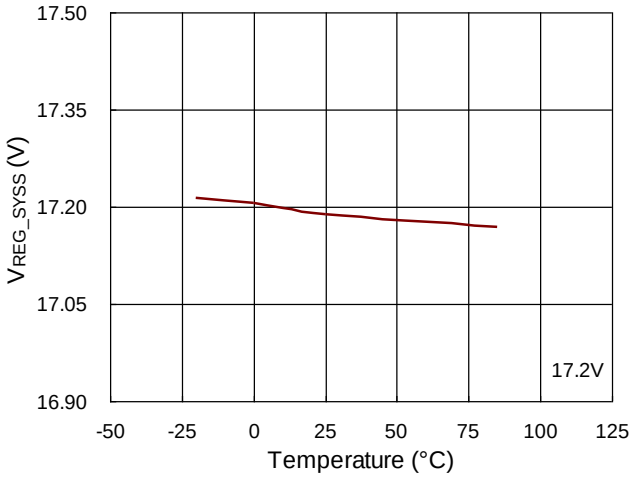
V_{REG_SYSS} vs. Temperature



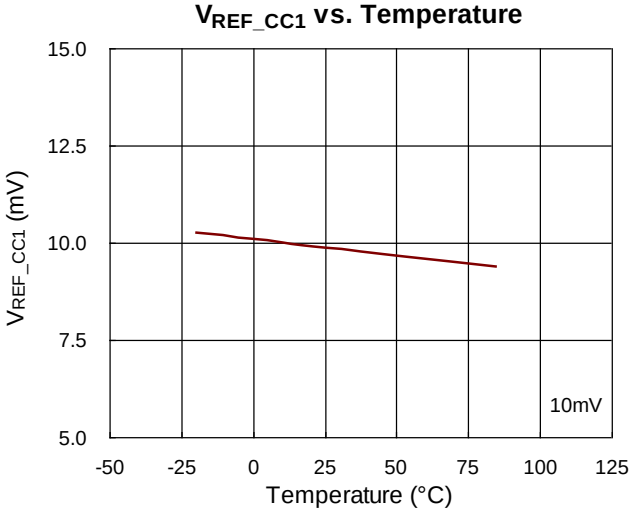
V_{REG_SYSS} vs. Temperature



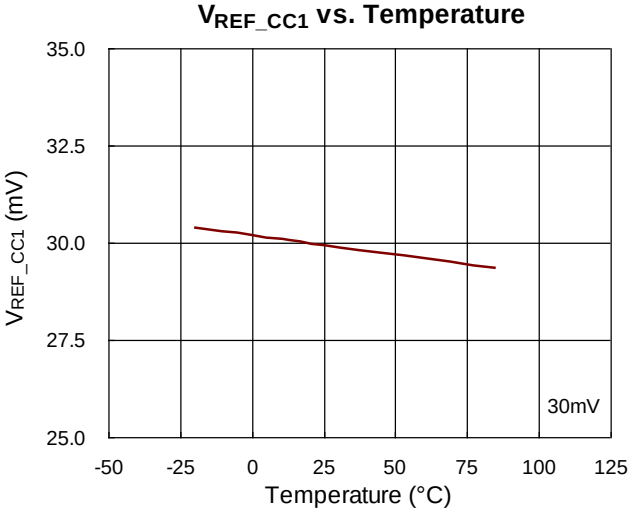
V_{REG_SYSS} vs. Temperature

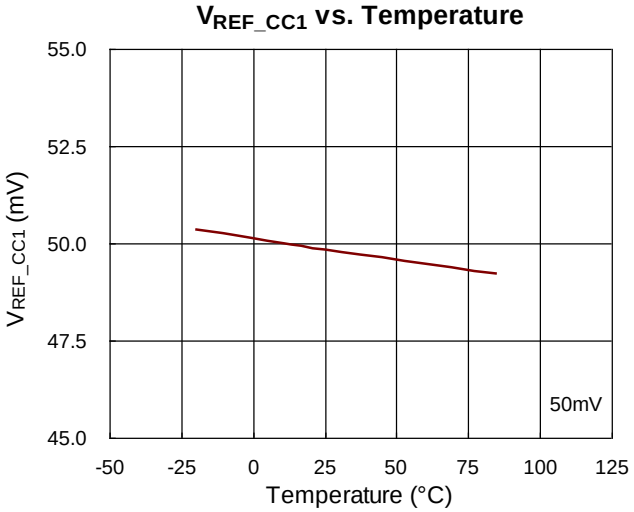


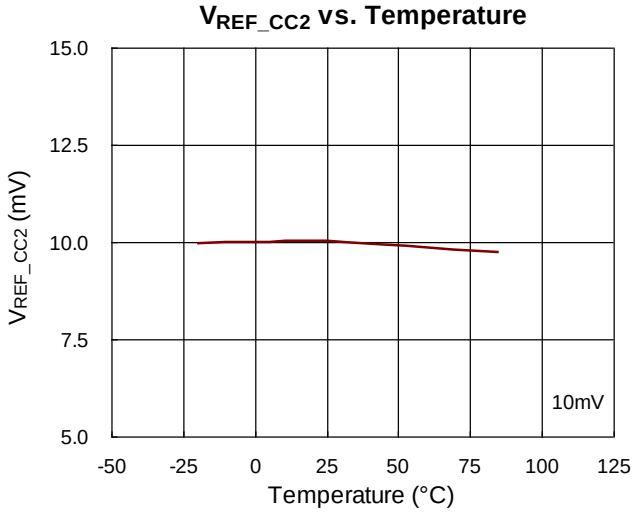
V_{REF_CC1} vs. Temperature

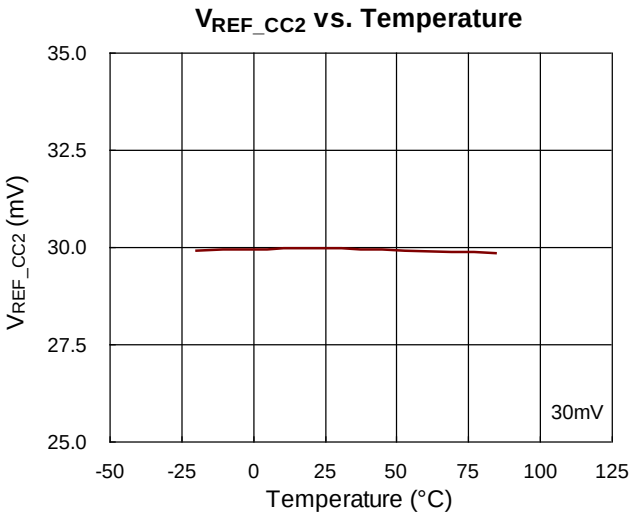


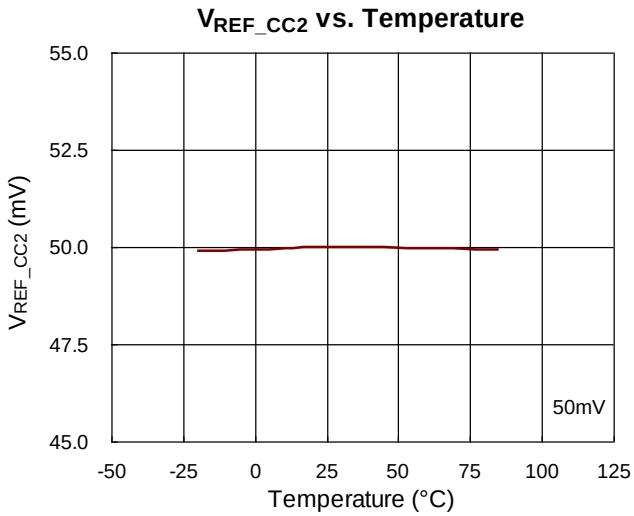
V_{REF_CC1} vs. Temperature

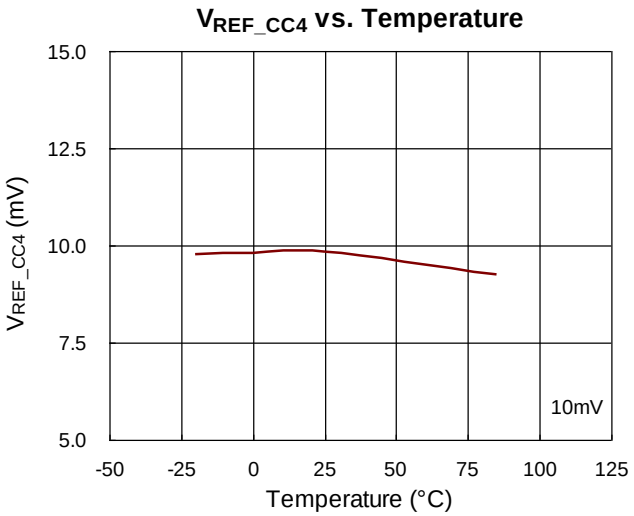


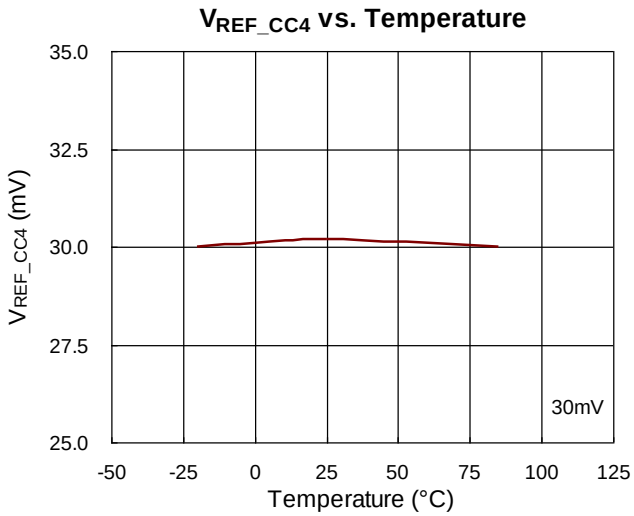


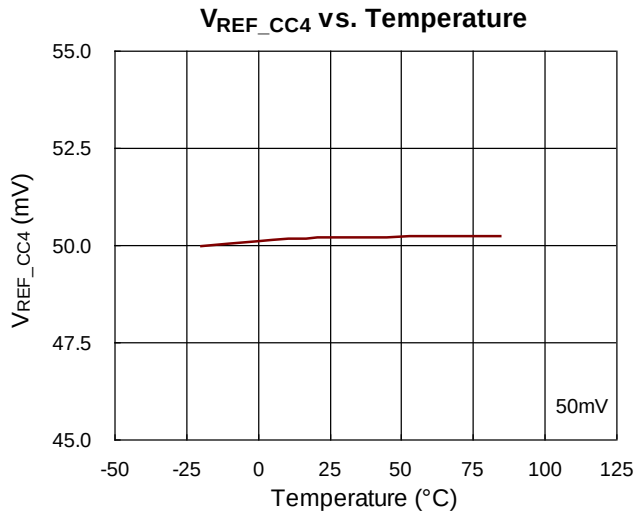


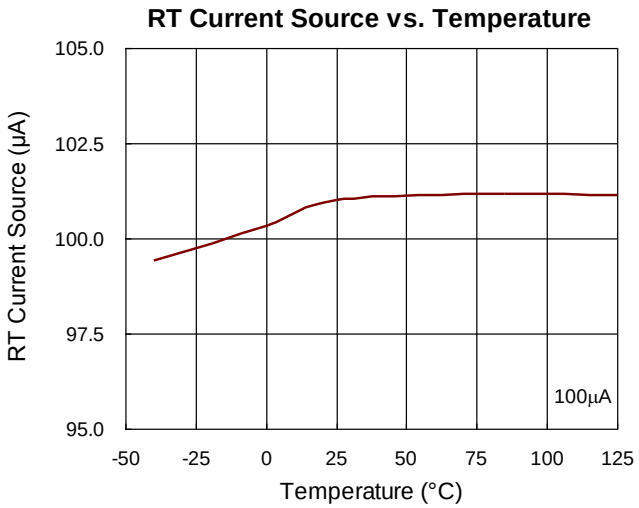


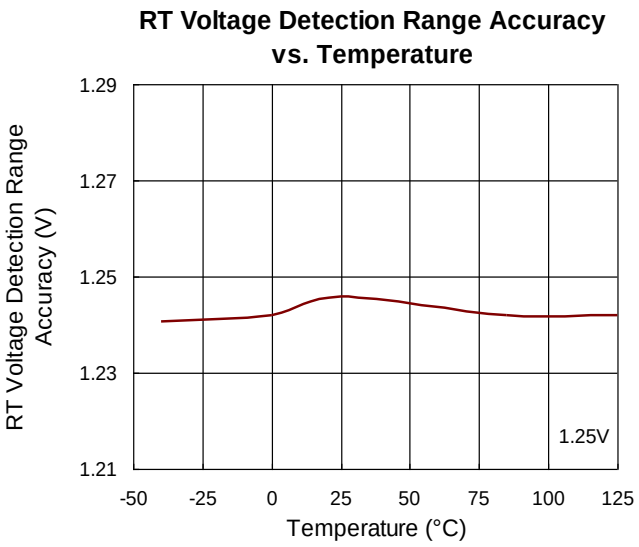


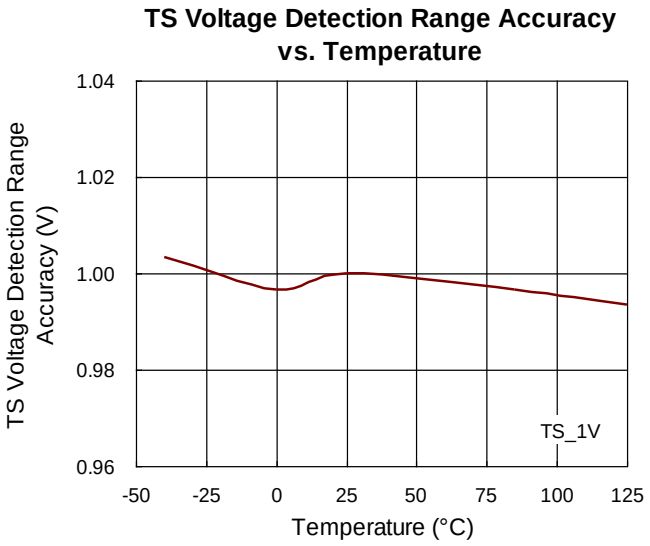


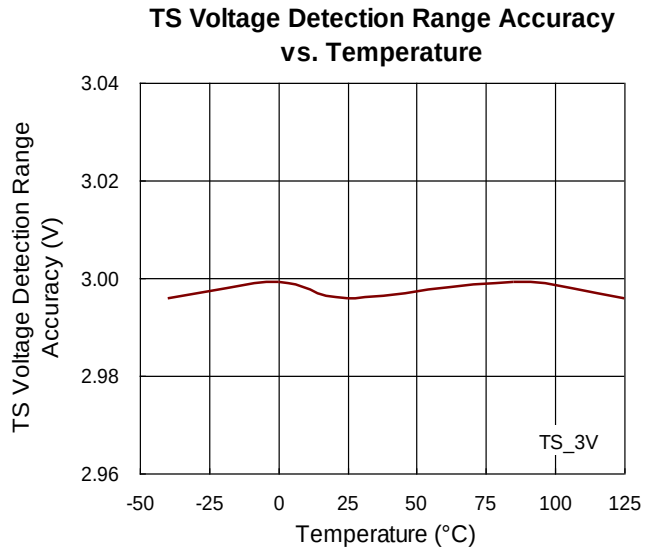


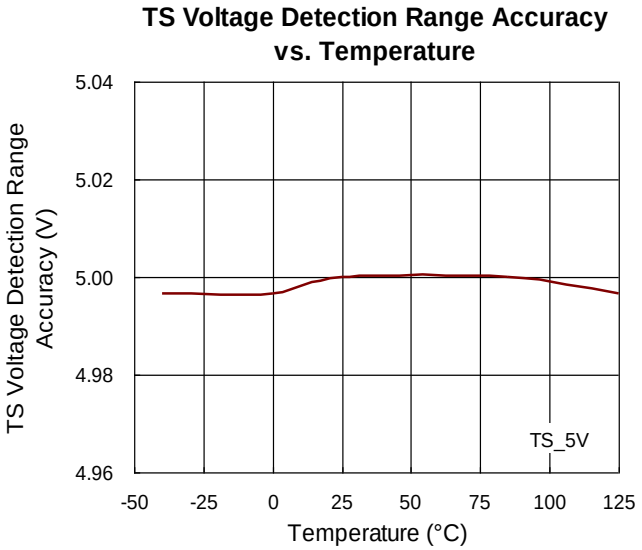




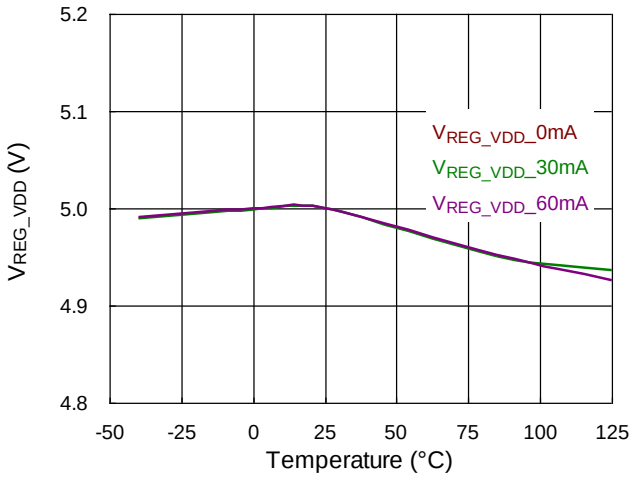




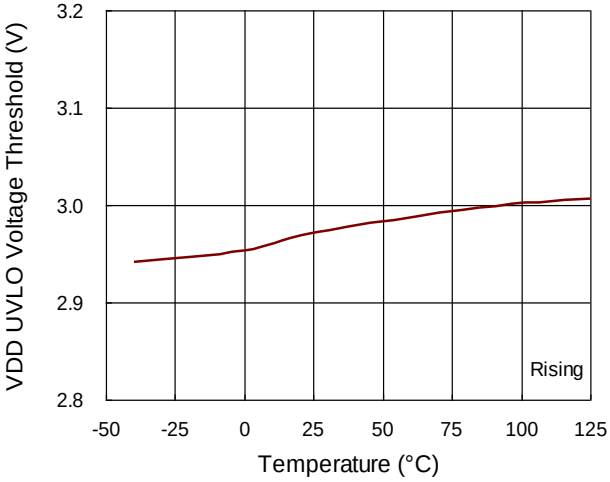




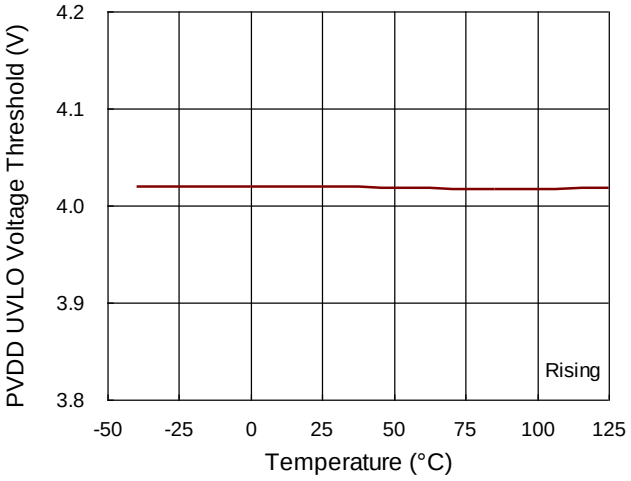
V_{REG_VDD} vs. Temperature



VDD UVLO Voltage Threshold vs. Temperature



PVDD UVLO Voltage Threshold vs. Temperature



Application Information

Calculating Output Discharge Time

Figure 1 shows the functional block diagram of the built- in output bleeders at BLD pins. The BLD bleeder consists of an external resistor (R_{BLD_EXT}) and a pull-low MOSFET (Q_{BLD1}) for discharging the capacitors at the output of the PWM converter. The discharge time (t_{DIS_COUT}) of the capacitor connected to the output of the PWM converter is determined by the following equation :

$$t_{DIS\_COUT} = \left(R_{BLD\_EXT} + R_{ON1}\right) \times C_{OUT} \times \ln\left(\frac{V_{OUT\_INI}}{V_{OUT\_FIN}}\right)$$

where :

- R_{BLD_EXT} is the resistance of the external resistor.
- R_{ON1} is on-resistance of the internal MOSFET Q_{BLD1}.
- C_{OUT} is the total capacitance connected to the output of the PWM converter.
- V_{OUT_INI} is the initial voltage of the PWM converter before discharging.
- V_{OUT_FIN} is the final voltage of the PWM converter after discharging.

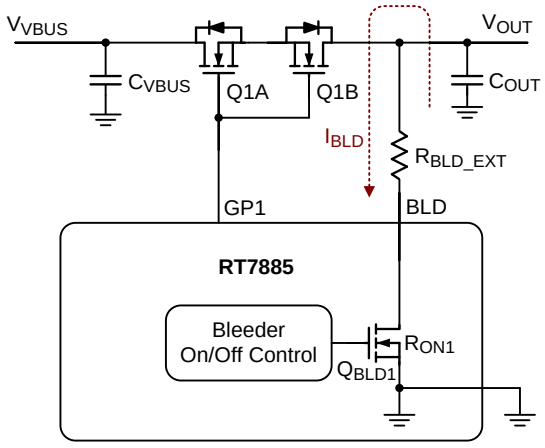


Figure 1. Functional Diagram of the Output Bleeders

Using Charge-Pump Gate Driver for Power-Path On/Off Control

Figure 2 shows the application schematic of a power-path on/off control, in which N-channel MOSFETs of low on-resistance driven by the built-in charge pump gate driver are employed to switch-on or switch-off the power-path. As shown in Figure 2, the selectable power-paths are located between the PWM converter output from the USB-C VBUS, or from the USB-A VBUSA terminal. If the internal control signal goes high, the GP voltage (V_{GP}) will be pulled high to turn on the power MOSFETs and connect the power-path. If the internal control signal goes low, V_{GP} will be pulled low by a built-in MOSFET to disconnect the power-path.

Note that both power inputs (VO/VDD and VBUSA/VDD) are needed for the charge pump. VO pin must be connected the PWM converter output and VBUSA pin must be connected USB-A terminal.

An optional MLCC capacitor (C_{GP}) can be used to reduce the V_{GP} rising rate and the surge current in the power path when the power MOSFETs being switched on. As the power MOSFETs being switched off, the parasitic inductor and capacitors, on the power path may cause voltage ringing at the drain of N-channel MOSFETs. An optional gate resistor (R_{GP}) can be added to reduce the falling rate of the power-path current and prevent voltage spikes. A 1μF MLCC capacitor (C_{MID}) between the source terminals to ground is necessary so as to prevent oscillation due to such dual-MOSFET connection.

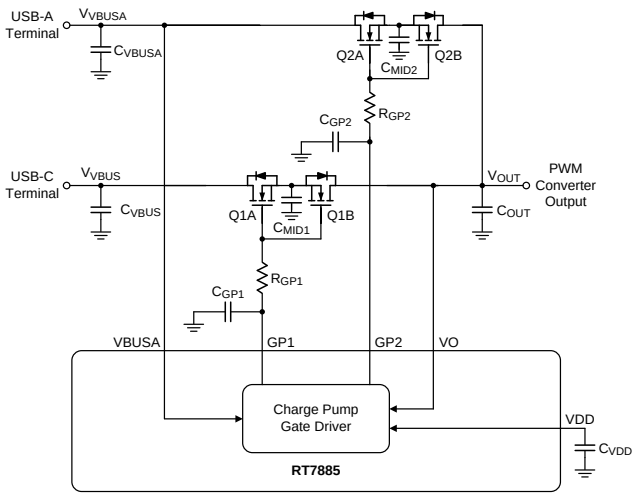


Figure 2. Functional Diagram of the Power-Path Control

VDD Bias Voltage Generation

In Figure 3, there are two input pins (BAT, and VBUS) to supply bias voltage to VDD pin for the RT7885 internal circuits. The RT7885 features multi-inputs and auto-selection design, including built-in high-voltage linear regulators, providing high flexibility in power bank applications.

An input power selection circuit can select input pins (BAT or VBUS) automatically or via software settings to generate the VDD voltage. When the linear regulator is enabled, it regulates the VDD voltage, 5V (Typ.), from BAT or VBUS pins.

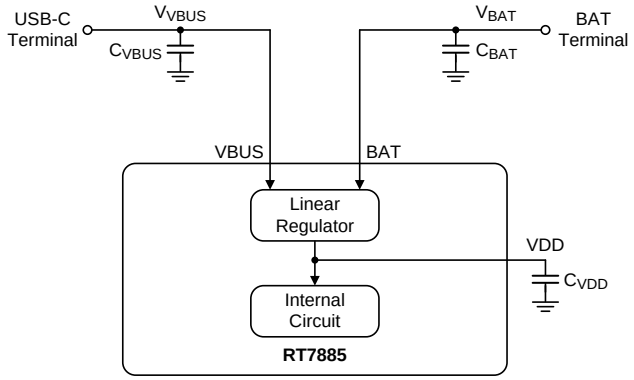


Figure 3. VDD Bias Voltage Generation

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-60L 7x7 package, the thermal resistance, θ_{JA}, is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (25.5°C/W) = 3.92W for a WQFN-60L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

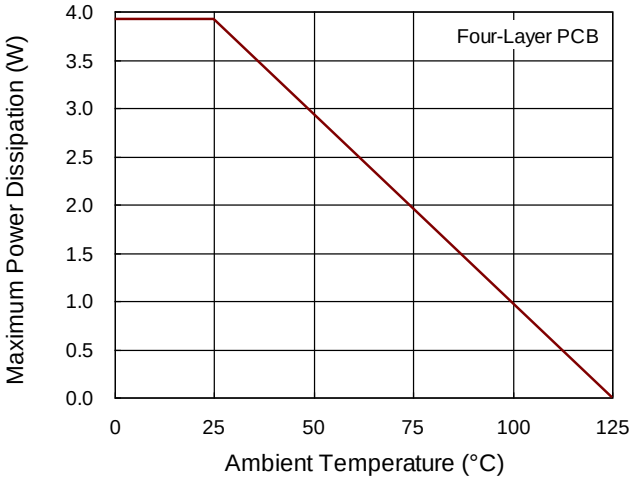


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

- Connect the IC GND pin and the exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via a low-impedance path. The exposed pad is also used to dissipate the heat into PCB.
- Connect the decoupling MLCCs near the pins of VDD, V2, PVDD, VBUS and VBUSA. Connect the MLCCs to the pins and IC-ground via low impedance paths.
- Connect the decoupling MLCC from the BOOT1/2 pin to the PHASE1/2 pin via a short and low-impedance path.
- Connect the PGND and PHASE1/2 pins to Source and Drain of low-side power MOSFET (controlled by LGATE1/2) via dedicated and low-impedance paths.

- Connect the PHASE1/2 and PCIN/PCON pins to Source and Drain of high-side power MOSFET (controlled by UGATE1/2) via dedicated and low-impedance paths.
- Connect the GND pin to GND terminals of the USB Type-C connector via dedicated and low-impedance path.
- Connect the capacitor close to CSIP/CSIN and CSOP/CSON pins. The paths of current sense pin (CSIN/PCIP, PCIN, CSIP, CSON/PCOP, PCON, CSOP) must be directly connected to the terminals of current sense resistors (R_{CSI}/R_{CSO}) using Kelvin connections as shown in the layout in Figure 5.

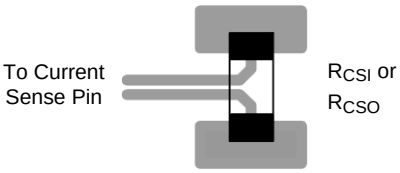


Figure 5. Kelvin connections for R_{CSI} or R_{CSO}

- Figure 6 is a recommended placement of the PWM Buck-Boost power-stage. Two critical current-loop paths "from C_{IN1} → R_{CSI} → Q_A → Q_B to C_{IN1}" and "from C_{O1} → R_{CSO} → Q_D → Q_C to C_{O1}" must be as short as possible to minimize the switching noise at CSIN/PCIP, PCIN, CSIP, CSON/PCOP, PCON, CSOP, PHASE1, and PHASE2 pins. The short paths also reduce radiated EMI. It's necessary to use an MLCC (10μF/50V, X5R/X7R) for the input capacitor (C_{IN1}) and output capacitor (C_{O1}). For reducing input and output voltage ripples during heavy load operation, it is recommended to add more MLCCs or solid input and output capacitors. To improve heat dissipation, increase the PCB areas for Drains of high-side and low-side MOSFETs.

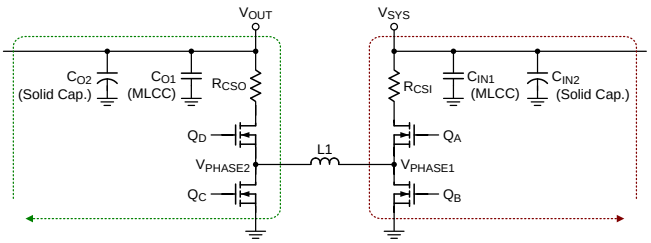


Figure 6. Recommended PCB Layout of the Power Stage

- Place the CV/CC loop compensation networks near the COMPV/COMPI pins and the IC-ground.
- To prevent the switching noises, separate the following signals from the switching nodes and the switching-current paths connected with PHASE pin :
  - Input and output current-sense signals;
  - CC1 and CC2 signals;
  - CV-loop feedback signal;
  - CV and CC compensation networks.
- For improving ESD immunity, connect MLCCs close to the GND and VBUS terminals of the USB Type-C connector and the GND and VBUSA terminals of the USB Type-A connector. Connect the capacitors to the VBUS/VBUSA and GND terminals through the low-impedance paths.
- BAT pin and VBUS pin are input pins of internal linear regulator to supply VDD bias voltage. BAT and VBUS paths are recommended to be thick and short.
- It is recommended to use the 4-layer PCB layout and the middle layers are as GND as possible to minimize the switching noise.
- Place R-C snubber circuit next to the inductor (L1) to reduce the slew rate of the inductor current to avoid switching noise, as shown in Figure 7.

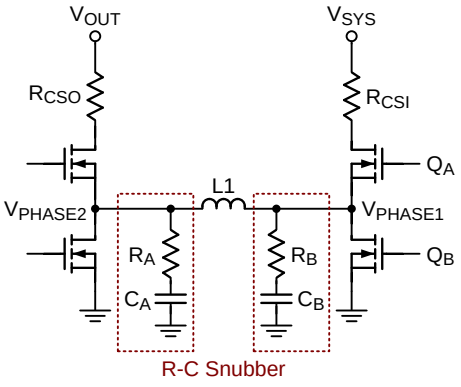


Figure 7. R-C Snubber Circuit

- It is recommended to adjust the slew rate of V_{PHASE1} and V_{PHASE2} appropriately to be close to or less than 0.3V/ns to avoid switching noise, as shown in Figure 8.

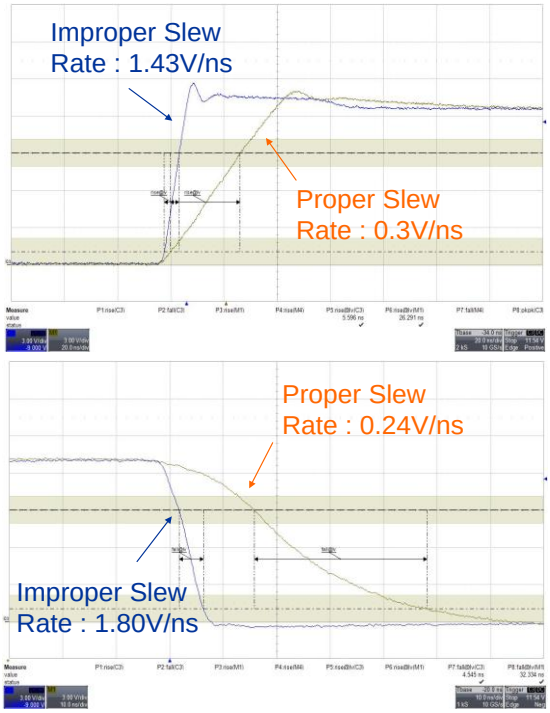
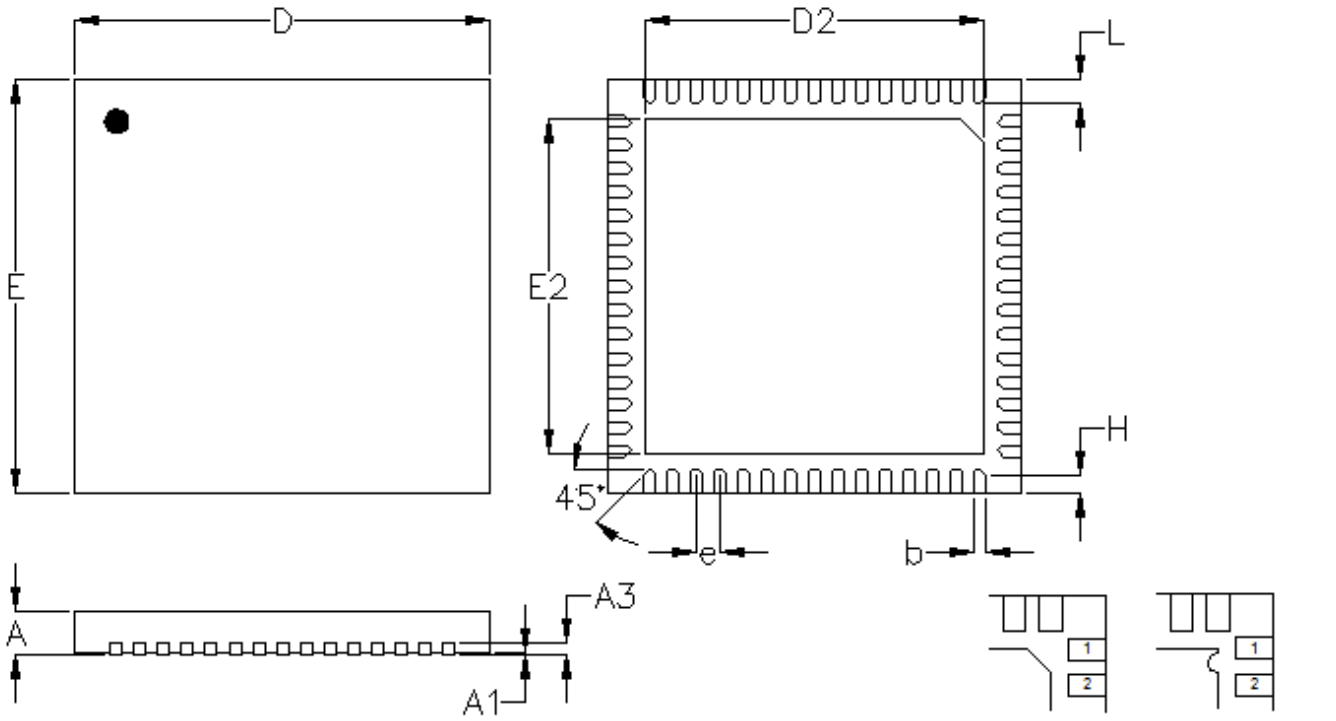


Figure 8. Recommended the slew rate of V_{PHASE1} and V_{PHASE2}

Outline Dimension



DETAIL A

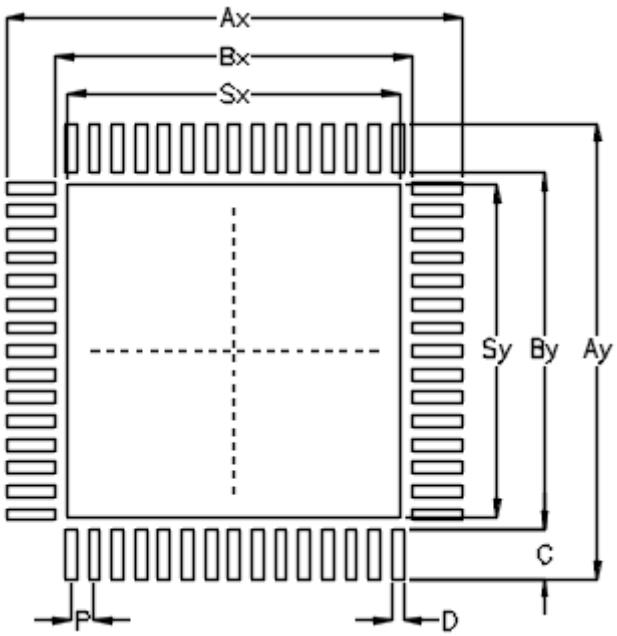
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-60	60	0.40	7.80	7.80	6.10	6.10	0.85	0.20	5.70	5.70	±0.05

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