50W Highly Integrated Wireless Receiver

Descriptions

The CPS4057 is a highly efficient, Qi-compliant, single-chip wireless power receiver/transmitter IC. It supports up-to 50W applications at receiver (Rx) mode and up-to 15W at transmitter (Tx) mode, which is particularly suitable for cell phone and portable device applications.

CPS4057 improves the system efficiency with integrated low $R_{DS(ON)}$ full-bridge synchronous rectifier to convert AC power received from the wireless transmitters.

The integrated ultra-low dropout linear (LDO) regulator offers the best performance in battery operated applications.

CPS4057 integrates an ARM MCU and an MTP memory to offer user programmability, together with advanced power management circuits to achieve extremely low standby power.

CPS4057 integrates accurate fault protections including over temperature, over current and over voltage protection to ensure the safe operations. A junction temperature sensor is also used for temperature sensing and advanced compensation.

The CPS4057 is available in a WLCSP-110 4.06mm x 4.47mm x 0.6mm (0.25mm ball, 0.4mm pitch) package. This product is rated over an operating temperature range of -40 to 85℃.

Features

- WPC 1.2.4 compliant wireless power receiver
- Support up to 50W at receiver mode and 15W at transmitter mode
- Q detector at Tx mode to improve FOD performance.
- Embedded ARM core, 32kB MTP to maximize the system design flexibility
- Fully synchronous rectifier with low $R_{DS(ON)}$
- Dedicated remote temperature sensing
- Abundant GPIO pins and Open-Drain buffers
- Support I^2C interface for system configuration and user programmability
- Comprehensive protections
  - 12-bit ADC for comprehensive input and output power monitoring
  - Rectifier over-voltage protection (OVP)
  - LDO over current protection (OCP)
  - Over temperature protection (OTP)
- Available in WLCSP-110 package

Applications

- Fast charge cellphone
- Tablets
- Other WPC compliant receivers

Order Information

Device	Package	Shipping
CPS4057	WLCSP-110	2000/Tape&Reel

Content

1 Description

1.1 Typical Application and Function Diagram

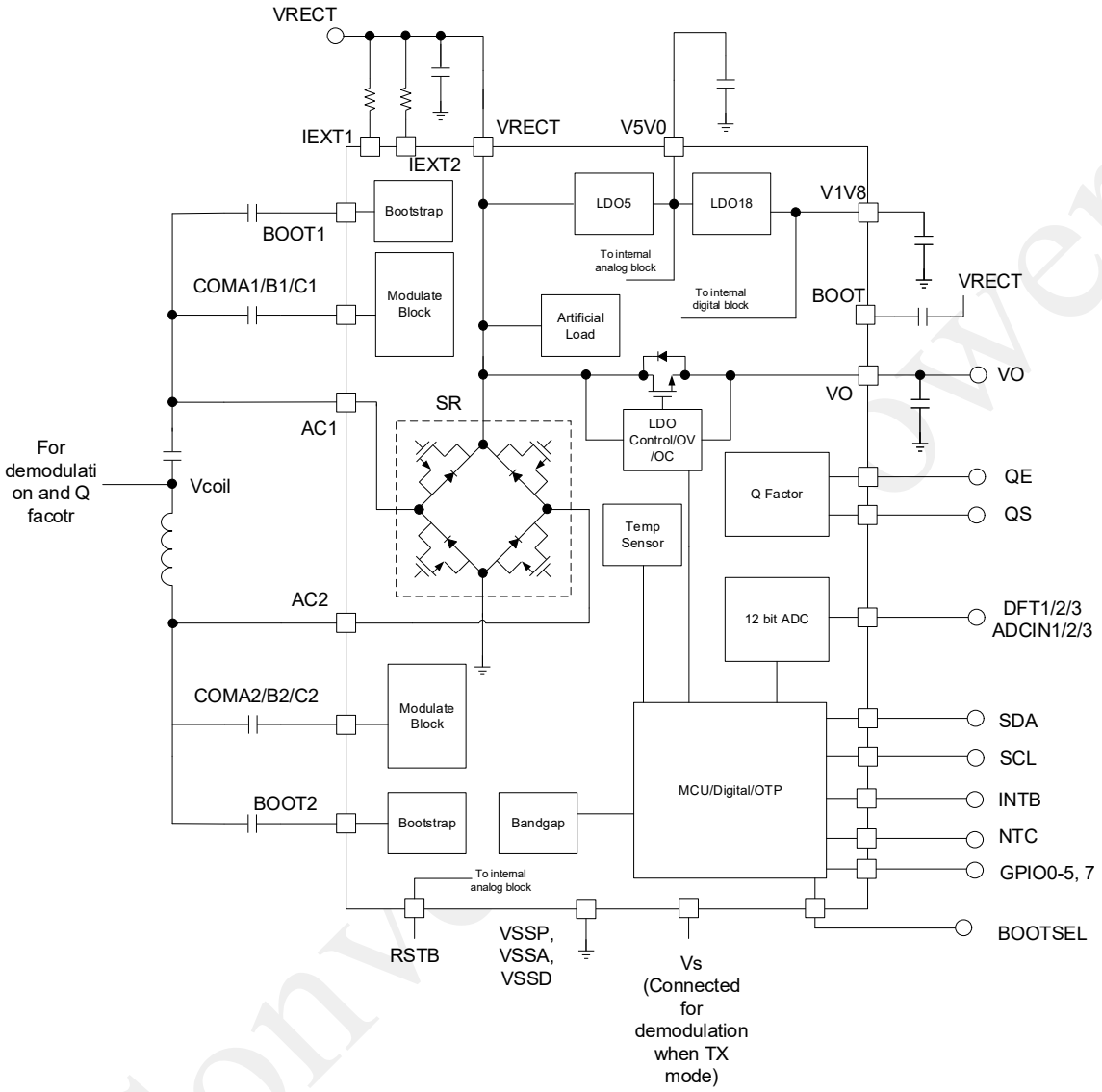


Figure 1 Block Diagram

1.2 Pins Diagram

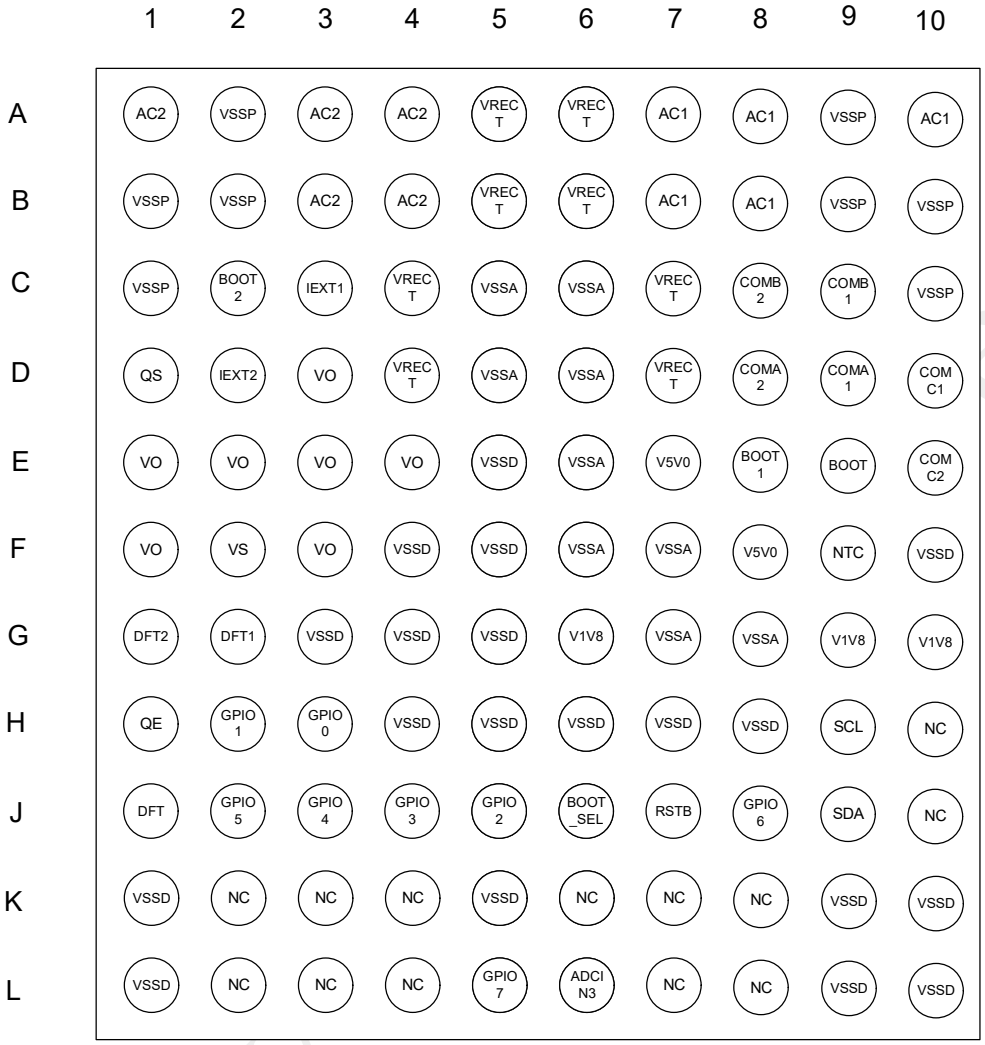


Figure 2 CPS4057 Pin-out (Top view)

1.3 Pin Description

Table 1 Pin Description

Pin	Name	Type	Function
A7,A8,A10 B7,B8	AC1	A I/O	AC1 input power for rectifier.
A1,A3,A4 B3,B4	AC2	A I/O	AC2 input power for rectifier.
A5/6, B5/6, C4,C7,D4,D7,	VRECT	A O	Full bridge Rectifier output. Place at least 2x22uF capacitor to GND.
D3,E1/2/3/4, F1,F3	VO	P O	Low dropout regulator output. Place a decouple 10uF capacitor.
G6,G9,G10	V1V8	P O	Internal 1.8V linear regulated output voltage for internal use. Place a 1uF capacitor to GND. Do not load this pin.
E7,F8	V5V0	P O	Internal 5V linear regulated output voltage for internal use. Place a 4.7uF capacitor to GND. Do not load this pin.
C5/6,D5/6,E6, F6/7,G7/8	VSSA	A GND	Analog Ground for intenral analog blocks.
E5,F4/5,G3/4/5, H4/5/6/7/8, K5,F10,K1,L1 K9/10,L9/10	VSSD	D GND	Digital Ground for intenral digital blocks.
A2,A9,B1/2, B9/10,C1,C10	VSSP	A GND	Power Ground.
E9	BOOT	A O	Bootstrap capacitor for main LDO. Suggest place a 3.3nF capacitor between BOOT and VRECT.
E8	BOOT1	A O	Bootstrap capacitor for AC1. Suggest place a 22nF capacitor between BOOT1 and AC1.
C2	BOOT2	A O	Bootstrap capacitor for AC2. Suggest place a 22nF capacitor between BOOT2 and AC2.
D9	COMA1	A O	Open-drain FET for transmitter modulation, connect a suitable capacitor to AC1.
D8	COMA2	A O	Open-drain FET for transmitter modulation, connect a suitable

			capacitor to AC2.
C9	COMB1	A O	Open-drain FET for transmitter modulation, connect a suitable capacitor to AC1.
C8	COMB2	A O	Open-drain FET for transmitter modulation, connect a suitable capacitor to AC2.
D10	COMC1	A O	Open-drain FET for transmitter modulation, connect a suitable capacitor to AC1.
E10	COMC2	A O	Open-drain FET for transmitter modulation, connect a suitable capacitor to AC2.
C3	IEXT1	A O	Internal Current Sink output pin.
D2	IEXT2	A O	Internal Current Sink output pin.
F2	VS	A I	Demodulate pin for TX mode.
H1	QE	A O	Q factor excitation output.
D1	QS	A I	Q factor sense input.
F9	NTC	A I	NTC input. Connect a tap of external resistor divider.
G2	DFT1/ADCIN1	A I/O	ADC input port. It can be configured as design for test pin.
G1	DFT2/ADCIN2	A I/O	ADC input port. It can be configured as design for test pin.
L6	ADCIN3	A I/O	ADC input port.
J6	BOOT_SEL	D I	Boot loader selection. Default 0 boot from ROM, 1 boot from flash.
H3	GPIO0	D I/O	General purpose I/O port.
H2	GPIO1	D I/O	General purpose I/O port.
J5	GPIO2	D I/O	General purpose I/O port.
J4	GPIO3	D I/O	General purpose I/O port.
J3	GPIO4	D I/O	General purpose I/O port.
J2	GPIO5	D I/O	General purpose I/O port.
J8	GPIO6/INT	D O	General purpose I/O port.
L5	GPIO7	D I/O	General purpose I/O port.
H9	SCL	D I	SCL of I2C serial interface.
J9	SDA	D I/O	SDA of I2C serial interface.
J7	RSTB	D I	Logic low enabled reset mode. Pull high will enable active mode. Float it will auto pull high to V1V8.
J1	DFT	A O	Analog Design For Test
H10,J10,	NC		Not connected.

K2/3/4,K6/7/8, L2/3/4,L7/8			

2 Specification

2.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Pin	Min	Max	Unit
Power voltage	AC1/2, COMA1/2, COMB1/2, COMC1/2	-0.3	30	V
Power voltage	VRECT, IEXT1/2	-0.3	30	V
Power voltage	BOOT1/2	-0.3	AC1/2 +6	V
Power voltage	BOOT	-0.3	V_{RECT}+ 6	
Power voltage	VO	-0.3	26	V
Demodulate	VS	-0.3	6	V
Q Factor	QS	-0.3	30	V
Logic voltage	GPIO	-0.3	2	V
Logic voltage	GPOD	-0.3	6	V
Control pin voltage	RSTB	-0.3	6	V
All Other Pin		-0.3	6	V
Maximum RMS Current from pin	COMA1/2, COMB1/2, COMC1/2		0.5	A
Maximum RMS current from pin	IEXT1/2		1	A
Maximum RMS Current from pin	AC1/2		3	A

Note: These are the stress ratings only. Stresses that exceeds the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at these or any other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

2.2 ESD Ratings

Table 3 ESD Information

Parameter	Value	Unit	Note
ESD tolerance	2000	V	Human Body Model (HBM)
	500	V	Charge Device Model (CDM)

2.3 Recommended Operation Conditions

Table 4 Recommended operation range

Parameter		Minimum	Typical	Maximum	Unit
V_{RECT}	Power voltage range		20	24	V
V_{5V}	Logic voltage range	-	5	5.5	V
V_{GP}	GPIO port Voltage	0		1.8	V
V_{OD}	Open drain port Voltage	0		5.5	V
T_J	Junction temperature	-40	-	125	°C
T_A	Ambient Operation temperature	-40	-	85	°C
T_{STG}	Storage temperature	-55	-	155	°C
T_{BUMP}	Maximum Soldering Temperature			260	°C

2.4 Electronics Characteristics

VRECT=20V, T_J=-40°C to 125°C.Co=10uF Typical values are at room temperature unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Quiescent Current						
I_{VRECT_SUPPLY}	Supply current	RSTB=low, no load		5.0		mA
I_{REST}	RESET current	RSTB=low	0.5	2		mA
Input Supply						
V_{RECT}	VRECT voltage		3.5	12	26	V
V_{RECT_UVLO}	VRECT UVLO threshold		2.3	2.5	2.7	V
$V_{RECT\_UVLO\_HYS}$	VRECT UVLO threshold hysteresis			0.2		V
$V_{RECT\_OV\_PRT}$	VRECT OV protection threshold, programmable		15		27	V
$V_{RECT\_OV\_PRT\_HYS}$	VRECT OV protection hysteresis, programmable		3		10	V
LDO1P8						
V_{OUT18}	LDO1P8 output voltage	I_{OUT18}=10mA	1.78	1.8	1.82	V
I_{OUT18_max}	LDO1P8 max load current		20			mA
LDO5						
V_{OUT5}	LDO5 output voltage	I_{OUT5}=10mA, V_{RECT}>6V	4.2	5		V
I_{OUT5_max}	Max load current		40			mA
Main Low Drop-out LDO Regulator						
I_{OUT}	Output current capability			3		A
V_{OUT}	Output voltage, programmable		3.5		24	V
I_{LDO_Limit}	LDO current limit, programmable	Programmable, step = 75mA, 5-bit Reg.	1.1		3.5	A
SR_{LDO_PU}	LDO start up slew-rate, programmable		5		40	mV/us
VDrop	Dropout Voltage	IO=1A, from VRECT to VO, (Fully on)		50		mV
Synchronize Rectifier						
R_{on}	On-resistance	V_{BST}=5V,		30		mΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		V_{RECT}=20V				
Thermal protection						
T_{SD}	T_J shutdown temperature			140		℃
T_{SD-HYS}	T_J shutdown hysteresis			20		℃
T_{WN}	T_J thermal warning, programmable			120		℃
T_{WN_HYS}	T_J thermal warning hysteresis			20		℃
VRECT Current Sense						
$ISEN_{ACC}$	I_{RECT} sense accuracy	I_O from 500mA to 3A	-1		+1	%
CSR_{ACC}	Current sense range		0		3.5	A
$I_{EXT1/2\_Limit}$	sink current limit			1		A
VRECT Voltage Sense						
$VRECTSEN_{ACC}$	VRECT voltage sense accuracy	V_{RECT} From 3.5V to 24V	-1		+1	%
VSR_{RECT}	V_{RECT} sense range		4		28	V
ADC Converter						
N	Resolution			12		Bit
Channel	Number of ADC channels			12		
RSTB						
V_{IH}	RSTB input threshold high		1.1			V
V_{IL}	RSTB input threshold low				0.7	V
RSTBILKG	RSTB pin leakage	RSTB=0		2		μA
GPIOx						
V_{IH}	Input threshold high		1.1			V
V_{IL}	Input threshold low				0.7	V
V_{OH}	Output logic high	Sink 4mA	1.44			V
V_{OL}	Output logic low	Source 8mA			0.36	V
I_{LKG_GPIO}	Leakage current	Input mode		± 0.1		μA
ODx (Input and output)						
V_{IH}	Input threshold high		1.1			V
V_{IL}	Input threshold low				0.7	V
V_{OL}	Output logic low	Source 8mA			0.36	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{LKG_GPOD}	Leakage current	Input mode		± 0.1		μA
SCL, SDA						
V_{IH}	Input threshold high		1.1			V
V_{IL}	Input threshold low				0.7	V
I_{LKG}	Leakage current		-1		1	μA
V_{OL}	Output logic low	Source 8mA			0.36	V
F_{SCL}	I^2C clock frequency				400	kHz
T_{LOW}	Clock low period			1.3		μs
T_{HIGH}	Clock high period			0.6		μs

3 Function Description

3.1 General Descriptions

CPS4057 is a highly integrated wireless power receiver/transmitter IC. It supports high efficiency AC-DC voltage regulation, secure bi-directional communication with wireless power transmitters (ASK/FSK), flexible interface ports to application processor as well as reliable over-voltage/current/temperature protections. A junction temperature sensor is used for temperature sense and advanced compensation. It also supports Tx mode for reversing wireless charging power from the output (Vo), which is particularly suitable for cell phone and other portable applications.

It includes a full-bridge synchronized rectifier, ultra-low dropout linear regulator, communication modulator/de-modulator, a multi-channel 12-bit ADC, ARM processor core and on-chip MTP memory to maximize software flexibility. Firmware can be programmed and updated through the I^2C interface with CPS program tool called E-link.

The CPS4057 is available in a WLCSP-110 4.06mm x 4.47mm x 0.6mm (0.25mm ball, 0.4mm pitch) package. This product is rated over a junction temperature range from -40℃. to 85℃.

3.2 WPT Modes

CPS4057 supports bi-directional wireless charging, which can operate in receiver or transmitter mode.

Rx Mode

At receiver (Rx) mode, alternating wireless power is picked up by the integrated full wave synchronized rectifier from AC1/AC2 pins. The rectified DC voltage/energy is stored on the capacitors connected to VRECT pins and the capacitors also serve as a low-pass filter to reduce the ripples on VRECT. Then the integrated LDO will provide a programmable, regulated output voltage V_{OUT} for the subsequent system load such as a charger.

Tx Mode

CPS4057 also supports transmitter (Tx) mode. In order to achieve reverse wireless charging with one-chip solution, the CPS4057 modules will be re-used or re-configured in Tx mode. CPS4057 shall set LDO into the bypass mode and reuse the rectifier power FETs as power inverter for DC-AC conversion. ASK de-modulation circuits will be enabled for communication purposes. The voltage/current sensing are re-used for V/I monitoring and FOD.

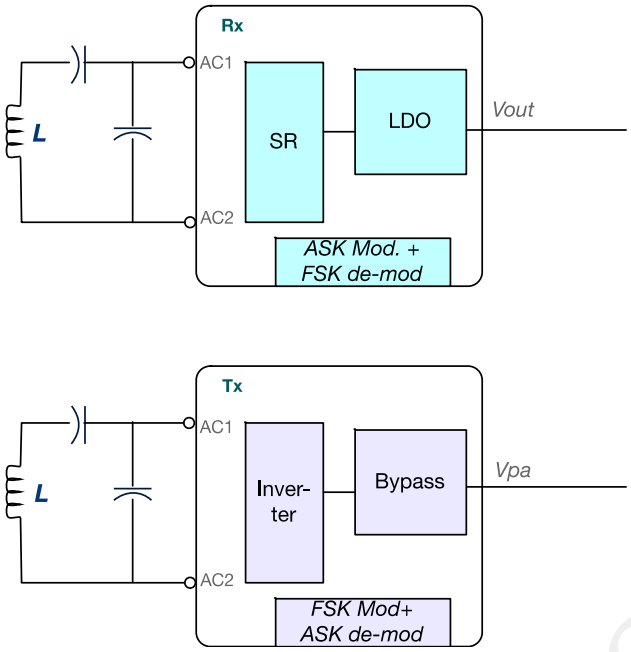


Figure 3 CPS4057 in Rx/Tx modes

For Both Rx/Tx, the wireless charging protocols are fully implemented by CPS4057 firmware. It can support standard WPC Qi v1.2.4 spec, BPP/EPP mode, as well as proprietary charging.

Figure 4 below illustrates the relationship among Qi BPP phases. The solid arrows indicate transitions which Tx initiates; and the dash-dotted arrows indicate transitions that the Rx initiates. The implementation and transition of each phase is accomplished by CPS4057.

In a wireless charging system, power transmitter make power available via DC to AC inverter and build a power path via a pair of coupled inductors between Tx and Rx. The full wave rectifier in CPS4057 (AC to DC) receive power and stored in Vrect-GND capacitors. Before Vrect voltage rising up to UVLO of Vrect, the rectifier works in passive mode (all 4 FETs are off). As VRECT rises above UVLO, the full-bridge rectifier would switch to various modes to maintain reliable connection and optimal efficiency. Vrect voltage is measured by ADC and feedback control error package to Tx to adjust the Tx power.

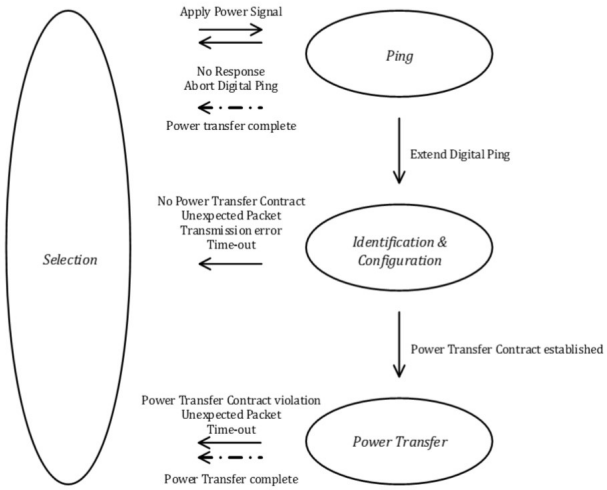


Figure 4 WPC Tx state diagram

3.3 RSTB

CPS4057 internal circuitry is gated by RSTB pin. When RSTB=0, the whole chip enters reset mode for minimal power consumption. Only internal LDOs (include V5V0 and V1V8) are active when RSTB=0. CPS4057 shall exit reset mode and enter Rx or Tx mode when VRECT rises above UVLO and RSTB is pulled to high.

3.4 Synchronized Rectifier

During Rx start up, the rectifier works in passive mode (all 4 FETs are off). As VRECT rises above UVLO, the full-bridge rectifier switches to synchronized operation for maximum efficiency.

At least 40uF capacitor is recommended to minimize the voltage ripple.

In Tx mode, the power FETs will be controlled by PMW registers and work in power inverter mode. The ON/OFF state is controlled by internal PWM signal.

3.5 Main LDO

CPS4057 integrates a main low-dropout regulator (LDO) to regulate the rectifier output voltage and provide the power required by battery charger. The output voltage of this main LDO is programmable.

LDO will enable its over-current and over-voltage protection independently to the operation mode. When LDO triggers current limit, it enters in over current protect state. Over current interrupt will be reported to system.

3.6 OVP

CPS4057 has V_{RECT} voltage monitoring and protection for robust applications. Over-voltage thresholds can be programmed from 15V to 27V.

In the event that V_{RECT} voltage rises above pre-set threshold, CPS4057 shall turn-on power dissipation path for protection purpose. It can enable internal IEXT1/IEXT2 switch and notify Tx to reduce the transmitted

power. CPS4057 also offers other over-voltage protection mechanisms through SW configuration. The protections are released when the V_{RECT} voltage falls below the recovery threshold.

3.7 Artificial Load

CPS4057 contains an SW-configurable internal current load from VRECT to ground. During power up, CPS4057 shall apply a certain load current (artificial load) for robustness of system communication. The artificial load is also used in EPP light load calibration stage.

3.8 Internal Voltage/Current Sense

The power loss based FOD is based on the Received Power (RP) reported by Rx and the transmitted power that is measured by Tx. This requires accurate power sensing at Vrect/Irect (VPA/IPA in Tx mode). Also, the power loss may increase due to Rdson increment as die temperature rises, dynamic Ploss compensation can be implemented based in SW.

The current sense circuit is used for main LDO current monitoring and over current protection. For FOD performance, the current sense accuracy is +/-1%. Current sensing is bi-directional for Rx/Tx mode applications.

3.9 LDO5 and LDO1P8

The CPS4057 has two internal low-dropout regulators for internal circuitry. LDO5 provides supply source for all internal analog and digital circuits. LDO1P8 provides 1.8V supply source for internal digital core.

Both LDOs require at least a 1uF decoupling low-ESR ceramic capacitor. Please do not use this to supply any external devices.

3.10 Over-Temperature Protection and External Temp. Sensing

CPS4057 supports on-die over-temperature protection and external temperature sensing through any analog input pin. If junction over temperature condition is detected, CPS4057 shall disable the main LDO and send out an “EPT” (end power transfer) packet to Tx to terminate the power delivery thus prevent junction temperature rising.

3.11 Q Factor Detect

CPS4057 integrates Q factor detection circuity. It shall be used to figure out the load property. CPS4057 excites a pulse to LC tank through QE pin. And the self-resonating waveform on QS pin is processed by internal analog blocks to determine the time taken to decay to a pre-determined level, effectively measuring the Q factor.

4 WPT Communication Interface

4.1 Load Modulation – ASK (Rx mode)

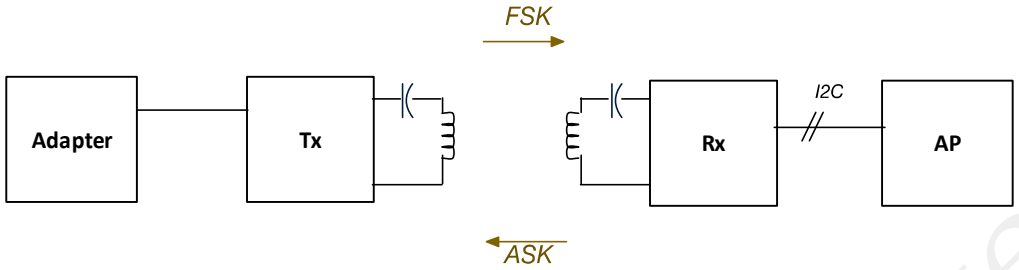


Figure 5 Example of WPT in-band communication (Bi-directional)

Receiver-to-transmitter communication is accomplished by modulating the load seen by transmitter's coil. CPS4057 includes two sets of load modulation switches for enhanced modulation and stable in-band communications. When the LM switches are enabled, AC1 and AC2 will be connected to a capacitor or a resistor to GND, which modulates the impedance seen by the coil. The amplitude change in the coil current/voltage can be detected by the transmitter de-modulation circuitry. The communication protocol is implemented in CPS4057 firmware. (Figure 6)

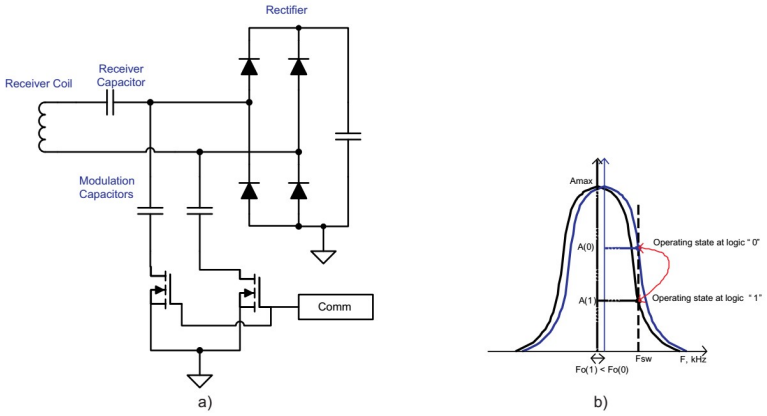


Figure 6 Receiver Capacitive Modulation Circuit

Per WPC spec, CPS4057 uses bi-phase encoding scheme for data communication. The data-rate is at 2kbp.(Figure 7)

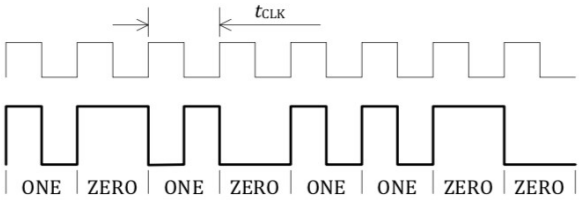


Figure 7 Example of bi-phase encoding

4.2 Frequency Detector and De-modulation (Rx mode)

The power transmitter communicates to the power receiver using Frequency Shift Keying (FSK), in which the transmitter modulates the operating frequency of the Power Signal. CPS4057 contains frequency detector and FSK demodulation circuitry to effectively de-code this in-band communication.

CPS4057 shall detect frequency and decode FSK in AC operation range from 90kHz to 300kHz. The reported frequency accuracy needs to be within +/-1%.

In WPC protocol, FSK is served as a response to ASK request. The bi-directional communication is initiated by receiver and the communication channel won't be blocked in any circumstance.

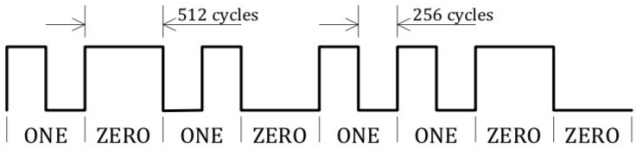


Figure 8 WPC FSK Bit-encoding scheme

4.3 ASK De-modulation (Tx mode)

To the transmitter, the Rx load modulation appears as an impedance change which results in measurable variations of the transmitter's coil voltage and current. CPS4057 also contains reliable ASK de-modulation circuits when this IC is set in Tx mode. CPS4057 detects the modulated signal, processes internally, and pass the received packets to MCU.

CPS4057 uses VS pin as voltage demodulation input (Figure 9) and the current demodulation signal is sensed from Vo to VRECT internally.

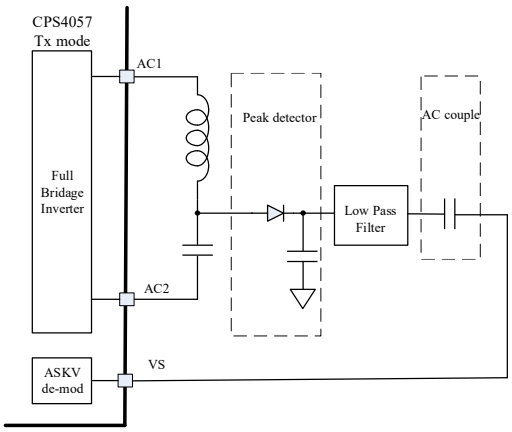


Figure 9 Voltage de-modulation circuit diagram

5 IO Interfaces

5.1 I²C Interface

CPS4057 provides an I²C interface that works as in slave mode, which is compatible with the data transfer modes as defined in the I²C bus. This interface adds flexibility to the device by making most functions and parameters programmable through the I²C host.

5.2 GPIO and GPOD

CPS4057 has seven General Purpose IO (GPIO) ports and three General Purpose Open Drain (GPOD) ports for additional user configuration purposes.

5.3 Analog Input

On CPS4057, any GPIO can be configured as an analog input pin, and mux-ed to internal ADC for sensing purpose. The common configurations of analog inputs for wireless charging receivers are:

- Received power gain
- Received power offset
- External temperature sensing (TS)

The received power gain and offset can be used for adjusting foreign object detection. These parameters are critical to Qi compliance and inter-operability test, and highly depends on receiver coil selection as well as product design.

6 Typical Application Schematic

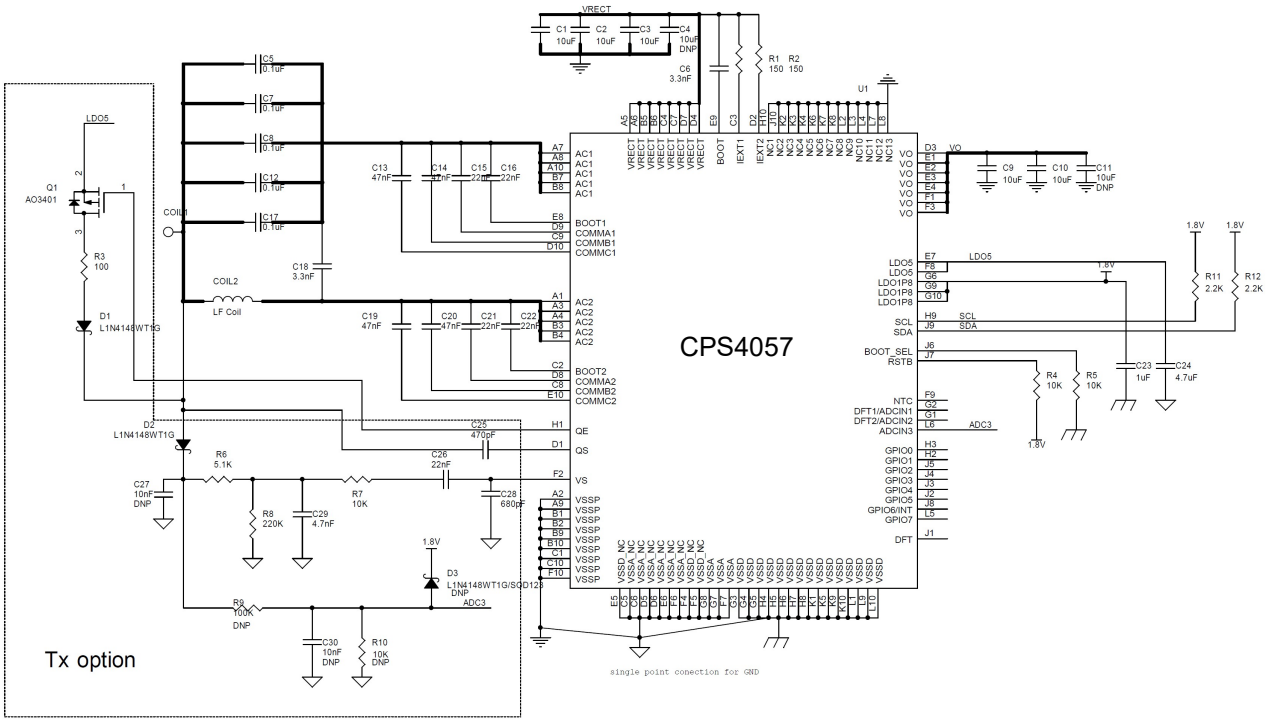
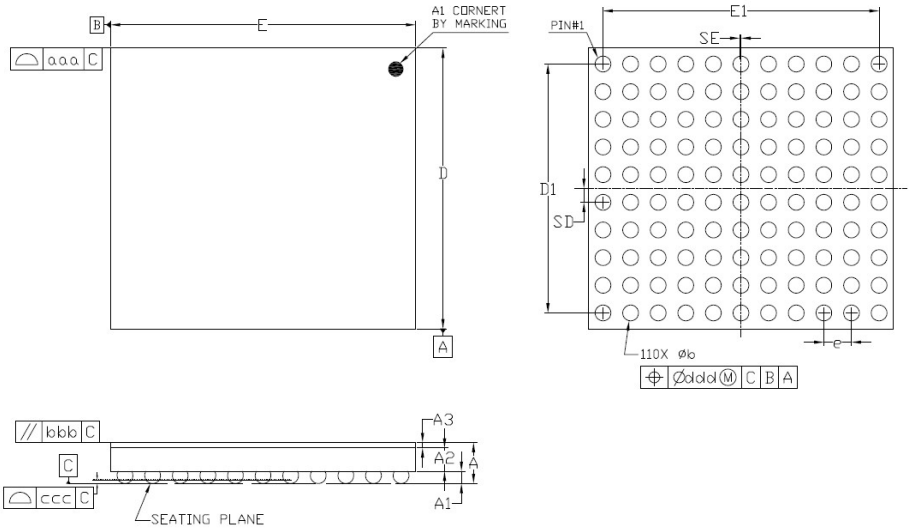


Figure 6 Typical application schematic

7 Package Information

WLCSP-110



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.490	0.540	0.590
A1	0.155	0.175	0.195
A2	0.315	0.340	0.365
A3	0.020	0.025	0.030
D	4.015	4.030	4.045
E	4.375	4.390	4.405
D1	3.550	3.600	3.650
E1	3.950	4.000	4.050
b	0.200	0.230	0.260
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

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