# Programmable USB Type-C PD Controller

## Hynetek Semiconductor Co., Ltd.

# HUSB311

## FEATURES

- **Dual-Role Port PD Compatible**
- **Attach/Detach Detection as Host, Device or DRP**
- **Current Capability Definition and Detection**
- **Cable Recognition**
- **Dead Battery Support**
- **VCONN Path Control**
- **Ultra-low Power Mode for Attach Detection**
- **Simple I²C Interface with Indication Pin**
- **Dual Slave Address for Dual Port Application**
- **BIST Mode Supported**
- **Programmable Default Settings**
- **9-Ball WLCSP (WLCSP-9B) and 14-Lead QFN (QFN-14L) Packages**

## APPLICATIONS

Smartphones
Tablets
Laptops
Monitors

## GENERAL DESCRIPTION

The HUSB311 is a USB Type-C PD controller that complies with the latest USB Type-C and PD3.0 standards. It implements the USB Type-C port power control for VCONN, USB Type-C CC control and sensing and USB PD Message delivery. HUSB311 has programmable $R_p$ and $R_d$ settings for each CC line. It does the USB type-C detection including attach and orientation. HUSB311 integrates a complete BMC encoding including a receiver and transmitter. With this physical layer of the USB BMC power delivery protocol, HUSB311 is able to handle the PD protocol and support any power up to 100W and perform role swap as needed. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

HUSB311 uses I²C to communicate with the TCPM via employing an INT signal for requesting attention.

## TYPICAL APPLICATION CIRCUIT

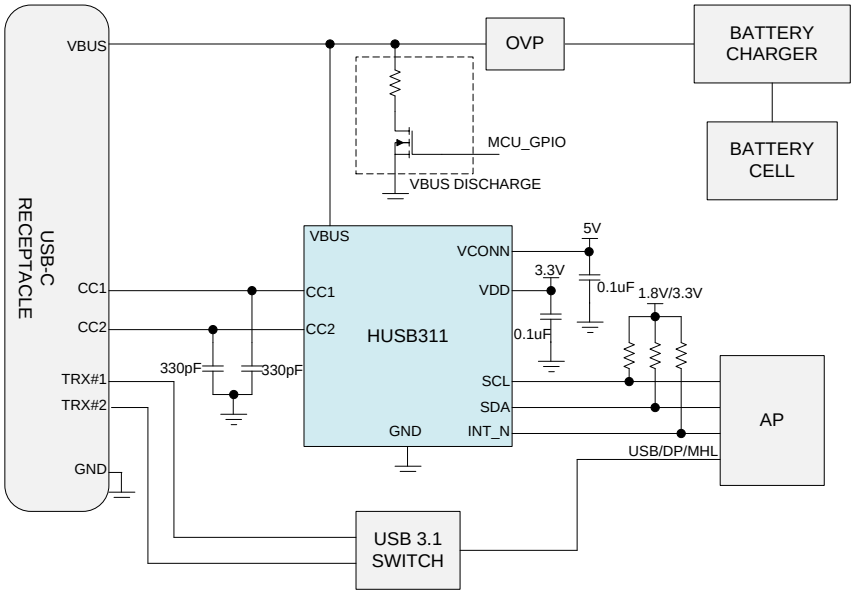



*Figure 1. HUSB311 Typical Application Circuit*

# TABLE OF CONTENTS



## REVISION HISTORY

| Version | Date | Owner | Descriptions |
|---|---|---|---|
| Rev. 2.0 | 08/2021 | Yingyang Ou | Initial version |
| Rev. 2.1 | 12/2021 | Yingyang Ou | Update Package TOP Marking<br>Add CDM ESD Rating<br>Update Thermal Resistance |
| Rev. 2.2 | 01/2022 | Yingyang Ou | Update HUSB311_ALA to HUSB311_BLA |
| Rev. 2.3 | 03/2022 | Yingyang Ou | Update HUSB311_BLA Package Top Marking |

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

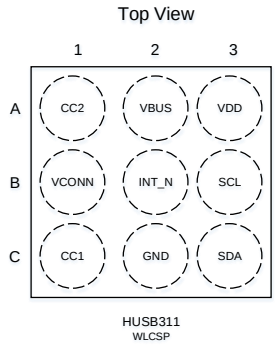



*Figure 2. HUSB311_ACC Pin Assignment*

**Table 1. HUSB311_ACC Pin Function Descriptions**

| Pin No. | Pin Name | Type[1] | Description |
|---|---|---|---|
| A1 | CC2 | I/O | Type-C connector Configuration Channel (CC2) pins. Initially used to determine when a attach event has occurred and what the orientation detected. |
| A2 | VBUS | A | VBUS input pin for attach and detach detection when operating as a Sink port (Device). |
| A3 | VDD | P | Input supply voltage. |
| B1 | VCONN | P | Regulated input pin connected to correct CC pin as VCONN to power Type-C full-featured cables and other accessories. |
| B2 | INT_N | O | Active low and open drain type interrupt output used to prompt the processor to read the registers. |
| B3 | SCL | I | $I^2C$ serial clock signal connected to the $I^2C$ master. The address is 0x4E or 0x3E. |
| C1 | CC1 | I/O | Type-C connector Configuration Channel (CC1) pins. Initially used to determine when a attach event has occurred and what the orientation detected. |
| C2 | GND | A | Ground plane. |
| C3 | SDA | I/O | $I^2C$ serial data signal connected to the $I^2C$ master. |

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O=Output Pin

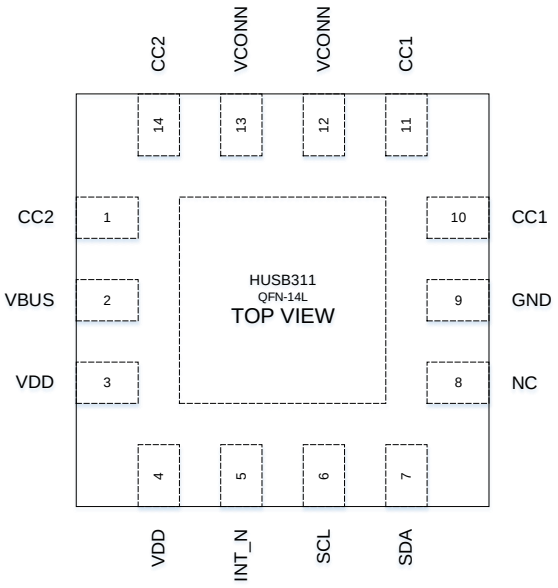



*Figure 3. HUSB311_BLA Pin Assignment*

**Table 2. HUSB311_BLA Pin Function Descriptions**

| Pin No. | Pin Name | Type[1] | Description |
|---|---|---|---|
| 1,14 | CC2 | I/O | Type-C connector Configuration Channel (CC2) pins. Initially used to determine when a attach event has occurred and what the orientation detected. |
| 2 | VBUS | A | VBUS input pin for attach and detach detection when operating as a Sink port (Device). |
| 3,4 | VDD | P | Input supply voltage. |
| 12,13 | VCONN | P | Regulated input pin connected to correct CC pin as VCONN to power Type-C full-featured cables and other accessories. |
| 5 | INT_N | O | Active low and open drain type interrupt output used to prompt the processor to read the registers. |
| 6 | SCL | I | $I^2C$ serial clock signal connected to the $I^2C$ master. The address is 0x4E or 0x3E. |
| 10,11 | CC1 | I/O | Type-C connector Configuration Channel (CC1) pins. Initially used to determine when a attach event has occurred and what the orientation detected. |
| 8 | NC | A | Not connected pin. This pin can be floating or connected to GND directly. |
| 9 | GND | A | Ground plane. |
| 7 | SDA | I/O | $I^2C$ serial data signal connected to the $I^2C$ master. |

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O=Output Pin

# RECOMMENDED OPERATING CONDITIONS

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Input Voltage | 3.0 V to 5.5 V |
| VCONN Input Voltage | 3.3 V to 5.5 V |
| VCONN Supply Current | 0 to 600 mA |
| VCONN Supply Voltage | 3 V to 5.5 V |
| Operating Temperature Range (Junction) | −40 °C to 125 °C |
| Ambient Temperature Range | −40 °C to 85 °C |

# SPECIFICATIONS

$V_{DD}$ = 3.3 V and $T_A$ = 25 °C for typical specifications, unless otherwise noted.

**Table 4.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| GENERAL PARAMETERS | | | | | | |
| Supply Voltage | $V_{DD}$ | | 3 | | 5.5 | V |
| Supply UVLO Voltage | $V_{UVLO\_R}$ | Rising edge | | 2.7 | | V |
| | $V_{UVLO\_F}$ | Falling edge | | 2.64 | | V |
| DRP Toggle Current consumption | $I_{Q\_DRP}$ | CC1/2 are togging and not attached. VCONN=5V, VDD current | | 33 | | μA |
| | $I_{VCN5V\_DRP}$ | CC1/2 are togging and not attached. VCONN=5V, VCONN current | | 20 | | μA |
| | $I_{Q\_DRP1}$ | CC1/2 are togging and not attached. VCONN=0V | | 33 | | μA |
| Operation Current | $I_{CC\_OPR}$ | CC is attached with $R_p$ and in Bus Idle status | | 2 | | mA |
| Type C CC Logic | | | | | | |
| Pull-down Voltage in Dead Battery Mode with Source Default $R_p$ | $V_{RDB\_DEF}$ | Source Default $R_p$ is 80μA±20% | 0.25 | | 1.5 | V |
| Pull-down Voltage in Dead Battery Mode with Source 1.5A $R_p$ | $V_{RDB\_1.5A}$ | Source Default $R_p$ is 180μA±8% | 0.45 | | 1.5 | V |
| Pull-down Voltage in Dead Battery Mode with Source 3A $R_p$ | $V_{RDB\_3A}$ | Source Default $R_p$ is 330μA±8% | 0.85 | | 2.5 | V |
| Rd in Active Mode | $R_d$ | VDD>$V_{UVLO}$, CC is configured as $R_d$ | 4.6 | 5.1 | 5.6 | kΩ |
| Attach Detection Threshold in Sink Mode | vRd_Snk | With $R_p$ is connected externally, CC is configured as $R_d$ | 0.25 | | 2.04 | V |
| Default Pull up current source in Source Mode | $I_{RP\_DEF}$ | CC is configured as Default $R_p$ | 64 | 80 | 96 | μA |
| 1.5A Pull up current source in Source Mode | $I_{RP\_1P5}$ | CC is configured as 1.5A $R_p$ | 166 | 180 | 194 | μA |
| 3A Pull up current source in Source Mode | $I_{RP\_3P0}$ | CC is configured as 3A $R_p$ | 304 | 330 | 356 | μA |
| Attach Detection Threshold in Source Mode | vRd_Src | With $R_d$ is connected externally, CC is configured as Default $R_p$ | 0.25 | | 1.5 | V |
| | | With $R_d$ is connected externally, CC is configured as 1.5A $R_p$ | 0.45 | | 1.5 | V |
| | | With $R_d$ is connected externally, CC is configured as 3A $R_p$ | 0.85 | | 2.45 | V |
| PD BMC | | | | | | |
| Bit Rate | $f_{BitRate}$ | | 270 | 300 | 330 | kbps |
| Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate | $p_{BitRate}$ | | | | 0.25 | % |
| Time from the end of last bit of a Frame until the start of the first bit of the next Preamble | $t_{InterFrameGap}$ | | 25 | | | μs |
| Time before the start of the first bit of the Preamble when the transmitter shall start driving the line | $t_{StartDrive}$ | | -1 | | 1 | μs |
| Time to cease driving the line after the end of the last bit of the Frame | $t_{EndDriveBMC}$ | | | | 23 | μs |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fall Time | $t_{Fall}$ | 10 % and 90 % amplitude points, with CC pin load of 200pF and 5.1KΩ in parallel | 300 | | | ns |
| Time to cease driving the line after the final high-to-low transition | $t_{HoldLowBMC}$ | | 1 | | | μs |
| Rise Time | $t_{Rise}$ | 10 % and 90 % amplitude points, with CC pin load of 200pF and 5.1KΩ in parallel | 300 | | | ns |
| Voltage Swing | vSwing | With CC pin load of 1.2nF and 5.1KΩ in parallel | 1.05 | 1.125 | 1.2 | V |
| TX Output Impedance | $z_{Driver}$ | BMC Tx output impedance while HUSB311 is driving the CC line | 33 | 50 | 75 | Ω |
| Time window for detecting non-idle | $t_{TransitionWindow}$ | | 12 | | 20 | μs |
| Receiver Input Impedance | $z_{BMCRx}$ | | 1 | | | MΩ |
| VCONN Source Control | | | | | | |
| VCONN FET Conduction Resistance | $R_{VCN}$ | | | | 1 | Ω |
| VCONN OC Threshold | $I_{VCN\_OC}$ | | | 650 | | mA |
| VCONN Present Threshold | $V_{VCN\_PRS}$ | | 2 | | 2.4 | V |
| Time for VCONN to turn on | $t_{VCN\_ON}$ | VCONN=5V and EN_VCONN=1b | | 300 | | μs |
| VBUS Detection | | | | | | |
| VBUS Present Threshold | $V_{BUS\_PRS\_F}$ | Assert VBUS_PRESENT bit | | 3.8 | | V |
| | $V_{BUS\_PRS\_R}$ | Set VBUS_PRESENT bit | | 4 | | V |
| VBUS vSave0V | vSafe0V | To trigger VBUS_80 interruption | | 0.8 | | V |
| VBUS Measure Range | $V_{BUS\_M\_RG}$ | | 4 | | 22 | V |
| VBUS Measure Step | $LSB_{VBUS\_M1}$ | VBUS=4-10V | | 0.5 | | V |
| | $LSB_{VBUS\_M2}$ | VBUS=10-20V | | 1 | | V |
| $I^2C$ Electrical Characteristics | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | | 50 | | 1000 | kHz |
| $I^2C$ Bus Supply Range | $V_{DD\_I2C}$ | | 1.5 | | 3.6 | V |
| Low Level Input Voltage | $V_{IL}$ | | | | 0.4 | V |
| High Level Input Voltage | $V_{IH}$ | | 1.2 | | | V |
| Low Level Output Voltage | $V_{OL}$ | Open Drain Output, Sink Current=2mA | | | 0.4 | V |
| Input Current Each IO Pin | $I_I$ | With $0.9V_{DD}$ applied | -10 | | 10 | μA |
| Pulse width of spikes that must be suppressed by the input filter | $t_{sp}$ | | | | 50 | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | | μs |
| Data Set-Up Time | $t_{SU:DAT}$ | | 50 | | | ns |
| Leakage Current Each IO Pin | $I_{LKG}$ | With VDD_$I^2C$ on each pin, VDD=5V | -1 | | 1 | μA |
| INT_N PIN | | | | | | |
| Leakage Current | $I_{LKG}$ | | -1 | | 1 | μA |
| Low Level Output Voltage | $V_{OL}$ | Sink Current=2mA | | | 0.4 | V |

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| VBUS | −0.3 V to 30 V |
| CC1,CC2 | −0.3 V to 24 V |
| VDD, VCONN, INT_N, SCL, SDA | −0.3 V to 6 V |
| Junction Temperature | 150 °C |
| Storage Temperature Range | −65 °C to 150 °C |
| Soldering Conditions | JEDEC J-STD-020 |
| Electrostatic Discharge (ESD) | |
| Human Body Model | ±2000 V |
| Charged Device Model | ±500 V |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC}$ is the junction to case thermal resistance.

**Table 6. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| QFN-14L | 106 | 10.8 | °C/W |
| WLCSP-9B | 118.3 | 68.9 | °C/W |

## ESD CAUTION

**Electrostatic Discharge Sensitive Device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# FUNCTIONAL BLOCK DIAGRAM

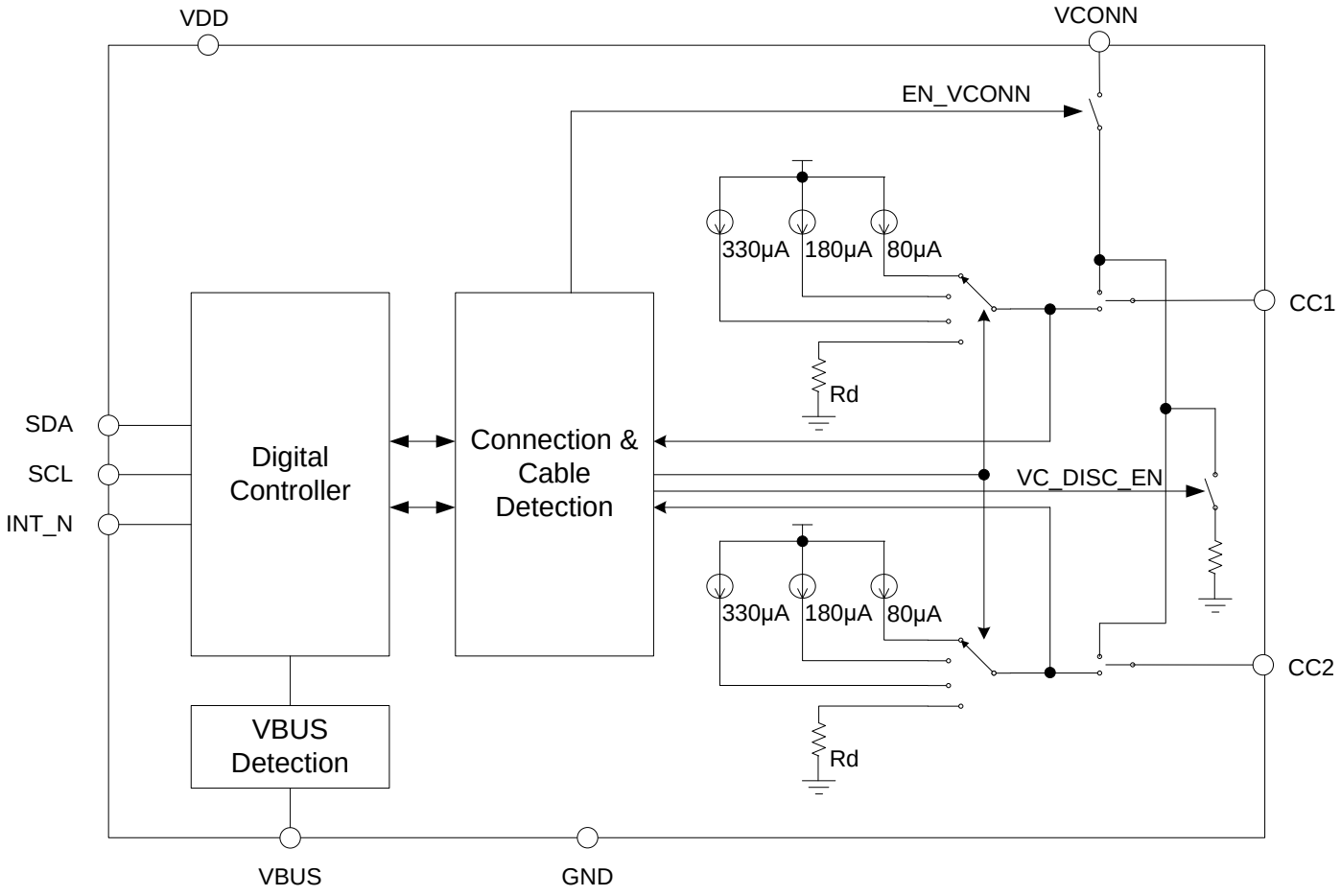



*Figure 4. HUSB311 Functional Block Diagram*

# THEORY OF OPERATION

HUSB311 is a USB type C Port Controller (TCPC). It is a PD PHY level controller which handles VBUS and VCONN power connections, CC logic and USB PD message delivery through a simple register interface. HUSB311 implements the portion of protocol layer in the USB PD specification. It sends and receives messages constructed in the TCPM and places them on the CC connections. HUSB311 implements the following portions of the USB PD protocol layer:

- CRCReceiverTimer(PRL_Tx_wait_for_Phy_Response_state)
- RetryCounter(PRL_Tx_Check_RetryCounter State)
- Message ID is not checked in HUSB311 when a non-GoodCRC message is received. Retried messages that are received are passed to the TCPM via $I^2C$
- A message transmission is considered successful after receiving a GoodCRC response with the matching MessageID and SOP type

Two ways allow for asynchronous messages are received (see 0x50 definition).

Two way to handle BIST mode (see 0x19 definition).

## COMMUNICATION BUS

HUSB311 communicates with TCPM via $I^2C$ bus. Two slave addresses are supported for HUSB311, 0x4E and 0x3E. It incorporates the $I^2C$ spec combined portion of SMBUS. There is an open drain active low output pin INT to indicate a change of state.

Some register of HUSB311 is 16-bit. It is important to access this register by writing or reading at the first address. See more details in the Register Map.

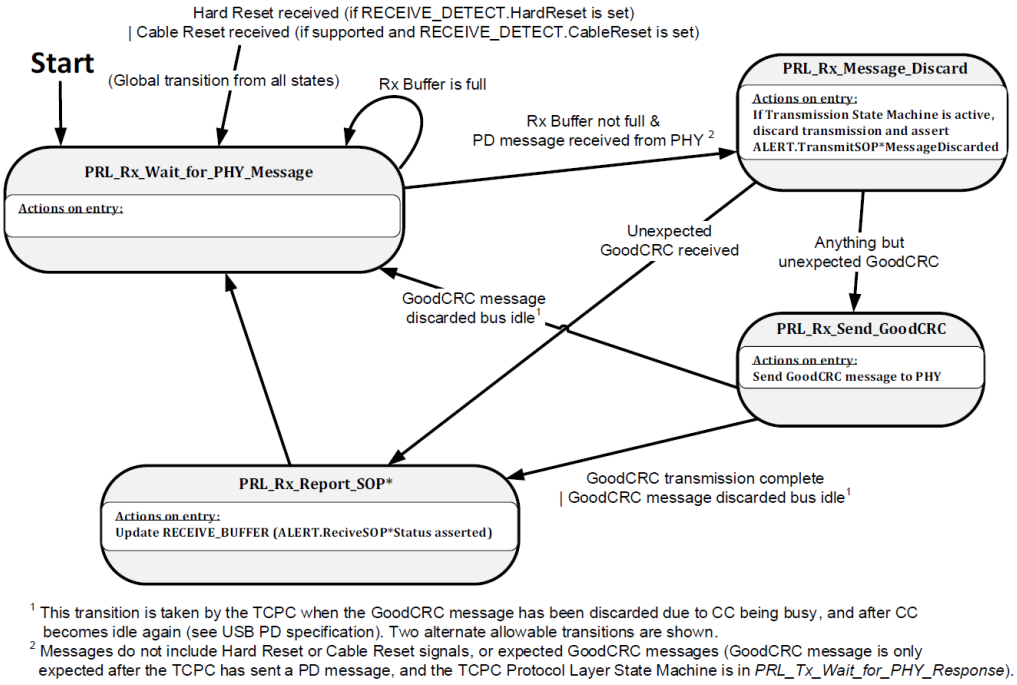
Once TCPM writes to a register or a bit that is reserved, HUSB311 ignores and does nothing.

## RX BUFFER

HUSB311 implements an Rx buffer for PD message reception. The main purpose of Rx buffer is:

1. Rx buffer is able to handle two set of 32 bytes date (1 byte Count number + 1 byte Frame type + 2 bytes Message Header+ 28 bytes data)
2. When there are already two sets of data stored in Rx buffer and the rest set of registers is 0, HUSB311 is not able to respond any following PD message (NOT include the CableReset, HardReset) unless TCPM reads Rx buffer and clear the RX_BUF by set Alert.RX_SOP_MSG_STATUS and Alert.RXBUF_OVFLOW

HUSB311 performs RX_BUFF as following state diagram. To start this state diagram, it depends on the RECEIVE_DETECT register settings (0x2F). If a not enabled type of message is received, the state will not change anything. Please note that if an unexpected GoodCRC is received during the transition, this unexpected GoodCRC should be treated as a command PD message.




[1] This transition is taken by the TCPC when the GoodCRC message has been discarded due to CC being busy, and after CC becomes idle again (see USB PD specification). Two alternate allowable transitions are shown.
[2] Messages do not include Hard Reset or Cable Reset signals, or expected GoodCRC messages (GoodCRC message is only expected after the TCPC has sent a PD message, and the TCPC Protocol Layer State Machine is in *PRL_Tx_Wait_for_PHY_Response*).

*Figure 5. Rx_BUFF State Machine Diagram*

After the GoodCRC according to the received PD message is sent in PRL_Rx_Send_GoodCRC, HUSB311 is going to PRL_Rx_Report_SOP* state and assert INT_N pin for attention.

TCPM handles the Alert interruption after INT_N is asserted. The Rx Buff is accessed by TCPM to transmit the data. TCPM should clean the RX_BUFF by writing Alert[2]=1. Once HUSB311 receives the write command to set Alert[2]=1.

## DEAD BATTERY MODE

Low battery power could cause conditions in which communication over USB Type-C can no longer be maintained. When this situation occurs, it is critical to transition to attached.SNK state so that power from VBUS can be used to charge the battery back to an operational level. This condition is known as Dead Battery Mode.

The HUSB311 supports dead-battery mode by presenting Rd to both CC pins when VDD is no longer active.

In the dead-battery mode access to HUSB311 registers is not available. Upon exiting dead-battery mode, the HUSB311 enters mode dictated by the value of ROLE_CONTROL register (Register 0x1A).

# REGISTERS

HUSB311 has several registers to configure the functions. The registers are accessed by the I²C address of 0x4E or 0x3E. The detailed function is defined as below:

**Table 7. Register Map**

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| 0x00 | VENDOR_ID | 7:0 | VID[7:0] | 0x99 | R | A unique 16-bit unsigned integer Assigned by the USB-IF to the Vendor |
| 0x01 | | 7:0 | VID[15:8] | 0x2E | R | |
| 0x02 | PRODUCT_ID | 7:0 | PID[7:0] | 0x11 | R | A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the HUSB311 |
| 0x03 | | 7:0 | PID[15:8] | 0x03 | R | |
| 0x04 | DEVICE_ID | 7:0 | DID[7:0] | 0x00 | R | A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the HUSB311 |
| 0x05 | | 7:0 | DID[15:8] | 0x00 | R | |
| 0x06 | USBTYPEC_REV | 7:0 | USBTYPEC_REV | 0x11 | R | Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001) |
| 0x07 | | 7:0 | Reserved | 0 | R | |
| 0x08 | USBPD_REV_VER | 7:0 | USBPD_VER | 0x11 | R | 0001 0000 – Version 1.0<br>0001 0001 – Version 1.1 Etc |
| 0x09 | | 7:0 | USBPD_REV | 0x20 | R | 0010 0000 – Revision 2.0 |
| 0x0A | PD_INTERFACE_REV | 7:0 | PDIF_VER | 0x10 | R | 0001 0000 – Version 1.0<br>0001 0001 – Version 1.1 etc. |
| 0x0B | | 7:0 | PDIF_REV | 0x10 | R | 0010 0000 – Revision 1.0 |
| 0x10 | ALERTL | 7 | ALARM_VBUS_VOLTAGE_H | 0 | R | Not support |
| | | 6 | TX_SUCCESS | 0 | RW | 0b: Cleared<br>1b: Reset or SOP* message transmission successful |
| | | 5 | TX_DISCARD | 0 | RW | 0b: Cleared<br>1b: Reset or SOP* message transmission not sent due to incoming receive message |
| | | 4 | TX_FAIL | 0 | RW | 0b: Cleared<br>1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission |
| | | 3 | RX_HARD_RESET | 0 | RW | 0b: Cleared<br>1b: Received Hard Reset message |
| | | 2 | RX_SOP_MSG_STATUS | 0 | RW | 0b: Cleared<br>1b: RECEIVE_BUFFER register changed |
| | | 1 | POWER_STATUS | 0 | RW | 0b: Cleared<br>1b: Port status changed |
| | | 0 | CC_STATUS | 0 | RW | 0b : Cleared<br>1b : CC_STATUS is changed |
| 0x11 | ALERTH | 7 | Reserved | 0 | R | Not support |
| | | 6 | Reserved | 0 | R | Not support |
| | | 5 | Reserved | 0 | R | Not support |
| | | 4 | Reserved | 0 | R | Not support |
| | | 3 | Reserved | 0 | R | Not support |
| | | 2 | RXBUF_OVFLOW | 0 | RW | 0b: HUSB311 Rx buffer is functioning properly<br>1b: HUSB311 Rx buffer has overflowed |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | 1 | FAULT | 0 | RW | 0b: No Fault<br>1b: A Fault has occurred |
| | | 0 | Reserved | 0 | R | Not support |
| 0x12 | ALERT_MASKL | 7 | M_ALARM_VBUS_VOLTAGE_H | 1 | R | Not support |
| | | 6 | M_TX_SUCCESS | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 5 | M_TX_DISCARD | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 4 | M_TX_FAIL | 1 | RW | 0b: Interrupt masked<br>1b : Interrupt unmasked |
| | | 3 | M_RX_HARD_RESET | 1 | RW | 0b : Interrupt masked<br>1b : Interrupt unmasked |
| | | 2 | M_RX_SOP_MSG_STATUS | 1 | RW | 0b : Interrupt masked<br>1b : Interrupt unmasked |
| | | 1 | M_POWER_STATUS | 1 | RW | 0b : Interrupt masked<br>1b : Interrupt unmasked |
| | | 0 | M_CC_STATUS | 1 | RW | 0b : Interrupt masked<br>1b : Interrupt unmasked |
| 0x13 | ALERT_MASKH | 7 | Reserved | 0 | R | Not support |
| | | 6 | Reserved | 0 | R | Not support |
| | | 5 | Reserved | 0 | R | Not support |
| | | 4 | Reserved | 0 | R | Not support |
| | | 3 | Reserved | 1 | R | Not support |
| | | 2 | M_RXBUF_OVFLOW | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 1 | M_FAULT | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 0 | M_ALARM_VBUS_VOLTAGE_L | 1 | R | Not support |
| 0x14 | POWER_STATUS_MASK | 7 | Reserved | 0 | R | Not support |
| | | 6 | M_TCPC_INITIAL | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 5 | M_SRC_NonDefault | 1 | R | Not support |
| | | 4 | M_SRC_VBUS | 1 | R | Not support |
| | | 3 | M_VBUS_PRESENT_DETC | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 2 | M_VBUS_PRESENT | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 1 | M_VCONN_PRESENT | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 0 | M_SINK_VBUS | 1 | R | Not support |
| 0x15 | FAULT_STATUS_MASK | 7 | M_VCON_OV | 0 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 6 | M_FORCE_OFF_VBUS | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked<br>This field has no meaning for HUSB311 |
| | | 5 | M_AUTO_DISC_FAIL | 1 | RW | 0b: Interrupt masked |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | | | | | 1b: Interrupt unmasked<br>This field has no meaning for HUSB311 |
| | | 4 | M_FORCE_DISC_FAIL | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked<br>This field has no meaning for HUSB311 |
| | | 3 | M_VBUS_OC | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked<br>This field has no meaning for HUSB311 |
| | | 2 | M_VBUS_OV | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked<br>This field has no meaning for HUSB311 |
| | | 1 | M_VCON_OC | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| | | 0 | M_I²C_ERROR | 1 | RW | 0b: Interrupt masked<br>1b: Interrupt unmasked |
| 0x18 | CONFIG_STANDARD_OUTPUT | 7 | H_IMPEDENCE | 0 | R | Not support |
| | | 6 | DBG_ACC_CONNECT_O | 0 | R | Not support |
| | | 5 | AUDIO_ACC_CONNECT | 0 | R | Not support |
| | | 4 | ACTIVE_CABLE_CONNECT | 0 | R | Not support |
| | | 3:2 | MUX_CTRL | 0 | R | Not support |
| | | 1 | CONNECT_PRESENT | 0 | R | Not support |
| | | 0 | CONNECT_ORIENT | 0 | R | Not support |
| 0x19 | TCPC_CONTROL | 7 | Reserved | 0 | R | |
| | | 6 | EN_LK4CNCT_ALERT | 0 | RW | 0b: Disable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes<br>1b: Enable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes |
| | | 5:4 | Reserved | 0 | R | |
| | | 3:2 | I²C_CK_STRETCH | 0 | R | Not support |
| | | 1 | BIST_TEST_MODE | 0 | RW | 0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert<br>1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. HUSB311 may temporarily store incoming messages in the Rx Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert |
| | | 0 | PLUG_ORIENT | 0 | RW | 0b: When VCONN is enabled (0x1C[0]=1), apply it to the CC2 pin. Monitor the CC1 pin for BMC communications<br>1b: When VCONN is enabled (0x1C[0]=1), apply it to the CC1 pin. Monitor the CC2 pin for BMC communications |
| 0x1A | ROLE_CONTROL | 7 | Reserved | 0 | R | |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | 6 | DRP | 0 | RW | 0b: No DRP. Bits B3..0 determine Rp/Rd settings<br>1b: DRP |
| | | 5:4 | RP_VALUE | 0 | RW | 00b: Rp default<br>01b: Rp 1.5 A<br>10b: Rp 3.0 A<br>11b: Reserved |
| | | 3:2 | CC2 | 10 | RW | 00b : Reserved<br>01b: Rp (Use Rp definition in B5..4)<br>10b : Rd<br>11b: Open (Disconnect or don't care) |
| | | 1:0 | CC1 | 10 | RW | 00b : Reserved<br>01b: Rp (Use Rp definition in B5..4)<br>10b: Rd<br>11b: Open (Disconnect or don't care) |
| 0x1B | FAULT_CONTROL | 7 | DIS_VCON_OV | 0 | RW | 0b: VCONN OV Fault detection circuit enabled when EN_VCONN=1 (Reg0x1C[0]=1)<br>1b: VCONN OV Fault detection circuit disabled |
| | | 6:5 | Reserved | 0 | R | Not support |
| | | 4 | DIS_FORCE_OFF_VBUS | 0 | R | Not support |
| | | 3 | DIS_VBUS_DISC_FAULT_TIMER | 0 | R | Not support |
| | | 2 | DIS_VBUS_OC | 0 | R | Not support |
| | | 1 | DIS_VBUS_OV | 0 | R | Not support |
| | | 0 | DIS_VCON_OC | 0 | RW | 0b: Fault detection circuit enabled when EN_VCONN=1 (Reg0x1C[0]=1)<br>1b: Fault detection circuit disabled |
| 0x1C | POWER_CONTROL | 7 | Reserved | 0 | R | |
| | | 6 | VBUS_VOL_MONITOR | 0 | R | Not support |
| | | 5 | DIS_VOL_ALARM | 0 | R | Not support |
| | | 4 | AUTO_DISC_DISCNCT | 0 | R | Not support |
| | | 3 | BLEED_DISC | 0 | R | Not support |
| | | 2 | FORCE_DISC | 0 | R | Not support |
| | | 1 | VCONN_POWER_SPT | 0 | RW | 0b: HUSB311 delivers at least 1W on VCONN.<br>1b: HUSB311 delivers at least the power indicated in DEVICE_CAPABILITIES.VCONN_POWER |
| | | 0 | EN_VCONN | 0 | RW | This bit control the path from VCONN pin to the repopulated CC pin (unattached CC).<br>0b: Disable VCONN Path(default)<br>1b: Enable VCONN Source to unattached CC |
| 0x1D | CC_STATUS | 7:6 | Reserved | 0 | R | |
| | | 5 | Look4Connection | 0 | R | 0b: the HUSB311 is NOT actively looking for a connection. A transition from 1 to 0 indicates a potential connection has been found |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | | | | | 1b: the HUSB311 is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition) |
| | | 4 | Connect_RESULT | 1 | R | 0b: the HUSB311 is currently presenting Rp<br>1b: the HUSB311 is currently presenting Rd |
| | | 3:2 | CC2_STATUS | 0 | R | If (ROLE_CONTROL.CC2 = Rp) or (Connect_RESULT = 0)<br>00b: SRC.Open (Open, Rp)<br>01b: SRC.Ra (below maximum vRa)<br>10b: SRC.Rd (within the vRd range)<br>11b: reserved<br>If (ROLE_CONTROL.CC2 = Rd) or (Connect_RESULT = 1)<br>00b: SNK.Open (Below maximum vRa)<br>01b: SNK.Default (Above minimum vRd-Connect)<br>10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5 A<br>11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0 A<br>If ROLE_CONTROL.CC2 = 00b, this field is set to 00b<br>If ROLE_CONTROL.CC2 = Open, this field is set to 00b and this change doesn't cause an Alert.CCStatus<br>This field always returns 00b if (CC_STATUS[5] = 1), that means the CCStatus is not updated to these bits or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT =0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2 |
| | | 1:0 | CC1_STATUS | 0 | R | If (ROLE_CONTROL.CC1 = Rp) or (Connect_RESULT = 0)<br>00b: SRC.Open (Open, Rp)<br>01b: SRC.Ra (below maximum vRa)<br>10b: SRC.Rd (within the vRd range)<br>11b: reserved<br>If (ROLE_CONTROL.CC1 = Rd) or Connect_RESULT= 1)<br>00b: SNK.Open (Below maximum vRa)<br>01b: SNK.Default (Above minimum vRd-Connect)<br>10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5 A<br>11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0 A<br>If ROLE_CONTROL.CC1 = 00b, this field is set to 00b<br>If ROLE_CONTROL.CC1 = Open, this field is set to 00b and this change doesn't cause an Alert.CCStatus<br>This field always returns 00b if (CC_STATUS[5] = 1), that means the CCStatus is not updated to these bits or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT = |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | | | | | 1). Otherwise, the returned value depends upon ROLE_CONTROL.CC1 |
| 0x1E | POWER_STATUS | 7 | DBG_ACC_CONNECT | 0 | R | Not support |
| | | 6 | TCPC_INITIAL | 0 | R | 0b: The HUSB311 has completed initialization and all registers are valid<br>1b: The HUSB311 is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh |
| | | 5 | SRC_NonDefault | 0 | R | Not support |
| | | 4 | SRC_VBUS | 0 | R | Not support |
| | | 3 | VBUS_PRESENT_DETC | 1 | R | This bit reflects the status of 0x90[1]<br>0b: VBUS Present Detection Disabled (Reg0x90[1]=0b)<br>1b: VBUS Present Detection Enabled (Reg0x90[1]=1b) |
| | | 2 | VBUS_PRESENT | 0 | R | This bit reflects the status of VBUS. It is an edge-trigged comparator. Only a valid rising or falling edge of VBUS can change this bit. The VBUS Detection is enabled by 0x90[1].<br>0b: VBUS Disconnected (VBUS<VBUS_PRS)<br>1b: VBUS Connected (VBUS>VBUS_PRS) |
| | | 1 | VCONN_PRESENT | 0 | R | 0b: VCONN is not present (VCONN<VCN_PRS)<br>1b: This bit is asserted when VCONN present CC1 or CC2 (VCONN>VCN_PRS)<br>When POWER_CONTROL[0]=0b, this bit is set as 0 |
| | | 0 | SINK_VBUS | 0 | R | Not support |
| 0x1F | FAULT_STATUS | 7 | VCON_OV | 0 | RW | 0b: Not in an over-voltage protection state<br>1b: Over-voltage fault latched. |
| | | 6 | FORCE_OFF_VBUS | 0 | R | Not support |
| | | 5 | AUTO_DISC_FAIL | 0 | R | Not support |
| | | 4 | FORCE_DISC_FAIL | 0 | R | Not support |
| | | 3 | VBUS_OC | 0 | R | Not support |
| | | 2 | VBUS_OV | 0 | R | Not support |
| | | 1 | VCON_OC | 0 | RW | This bit is set if the current exceeds the VCON_OC.<br>0b: No Fault detected<br>1b: Over-current VCONN fault latched |
| | | 0 | $I^2C$_ERROR | 0 | RW | 0b: No Error<br>1b: $I^2C$ error has occurred |
| 0x20 | | 7:0 | Reserved | 0 | R | Not support |
| 0x21 | | 7:0 | Reserved | 0 | R | Not support |
| 0x22 | | 7:0 | Reserved | 0 | R | Not support |
| 0x23 | COMMAND | 7:0 | | 0x00 | W | Default Value after POR |
| | | | Look4Connection | 0x99 | W | Start DRP Toggling if ROLE_CONTROL.DRP=1b. If ROLE_CONTROL.CC1/CC2= 01b start with |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | | | | | Rp, if ROLE_CONTROL.CC1/CC2=10b start with Rd |
| | | | RxOneMore | 0xAA | W | Configure the HUSB311 to automatically clear the RECEIVE_DETECT register after sending the next GoodCRC |
| | | | ResetTransmitBuffer | 0xDD | W | The HUSB311 resets the pointer of the Tx_BUFFER register to offset 1 and the contents of Tx_BUFFER becomes invalid when this COMMAND is issued by the TCPM |
| | | | ResetReceiverBuffer | 0xEE | W | After receiving this COMMAND, HUSB311 resets the pointer of RECEIVE_BUFFER to 1 (0x32). This COMMAND doesn't clear the RX_BUFFER |
| 0x24 | DEVICE_CAPABILITIES_1L | 7:5 | ROLES_SUPPORT | 110 | R | 000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP)<br>001b: Source only<br>010b: Sink only<br>011b: Sink with accessory support (optional)<br>100b: DRP only<br>101b: Adapter or Cable (Ra) only<br>110b: Source, Sink, DRP, Adapter/Cable all supported<br>111b: Not valid |
| | | 4 | ALL_SOP_SUPPORT | 1 | R | 1b: All SOP* messages are supported |
| | | 3 | SOURCE_VCONN | 1 | R | 0b: HUSB311 is not capable of switching VCONN<br>1b: HUSB311 is capable of switching VCONN |
| | | 2 | CPB_SINK_VBUS | 0 | R | Not Supported |
| | | 1 | SOURCE_HV_VBUS | 0 | R | Not Supported |
| | | 0 | SOURCE_VBUS | 0 | R | Not Supported |
| 0x25 | DEVICE_CAPABILITIES_1H | 7 | Reserved | 0 | R | Not Supported |
| | | 6 | CPB_VBUS_OC | 0 | R | Not Supported |
| | | 5 | CPB_VBUS_OV | 0 | R | Not Supported |
| | | 4 | CPB_BLEED_DISC | 0 | R | Not Supported |
| | | 3 | CPB_FORCE_DISC | 0 | R | Not Supported |
| | | 2 | VBUS_MEASURE_ALARM | 0 | R | Not Supported |
| | | 1:0 | SOURCE_RP_SUPPORT | 10 | R | 00b: Rp default only<br>01b: Rp 1.5 A and default<br>10b: Rp 3.0 A, 1.5 A, and default<br>11b: Reserved<br>Rp values which may be configured by the TCPM via the ROLE_CONTROL register |
| 0x26 | DEVICE_CAPABILITIES_2L | 7 | SINK_DISCONNECT_DET | 0 | R | 0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VBUS_PRESENT=0b to indicate a Sink disconnect) |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | 6 | STOP_DISC_THD | 0 | R | 0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) |
| | | 5:4 | VBUS_VOL_ALARM_LSB | 11 | R | 11: reserved |
| | | 3:1 | VCONN_POWER | 010 | R | 000b: 1.0 W<br>001b: 1.5 W<br>010b: 2.0 W<br>011b: 3 W<br>100b: 4 W<br>101b: 5 W<br>110b: 6 W<br>111b: External |
| | | 0 | VCONN_OCF | 1 | R | 0b: HUSB311 is not capable of detecting a VCONN over-current fault<br>1b: HUSB311 is capable of detecting a VCONN over-current fault |
| 0x27 | DEVICE_CAPABILITIES_2H | 7:0 | Reserved | 0 | R | Not support |
| 0x28 | STANDARD_INPUT_CAPABILITIES | 7:3 | Reserved | 0 | R | Not support |
| | | 2 | VBUS_EXT_OVF | 0 | R | Not support |
| | | 1 | VBUS_EXT_OCF | 0 | R | Not support |
| | | 0 | FORCE_OFF_VBUS_IN | 0 | R | Not support |
| 0x29 | STANDARD_OUTPUT_CAPABILITIES | 7 | Reserved | 0 | R | Not support |
| | | 6 | CPB_DBG_ACC_IND | 0 | R | Not support |
| | | 5 | CPB_VBUS_PRESENT_MNT | 0 | R | Not support |
| | | 4 | CPB_AUDIO_ADT_ACC_IND | 0 | R | Not support |
| | | 3 | CPB_ACTIVE_CABLE_IND | 0 | R | Not support |
| | | 2 | CPB_MUX_CFG_CTRL | 0 | R | Not support |
| | | 1 | CPB_CONNECT_PRESENT | 0 | R | Not support |
| | | 0 | CPB_CONNECT_ORIENT | 0 | R | Not support |
| 0x2E | MESSAGE_HEADER_INFO | 7:5 | Reserved | 0 | R | Not support |
| | | 4 | CABLE_PLUG | 0 | RW | 0b: Message originated from Source, Sink, or DRP<br>1b: Message originated from a Cable Plug |
| | | 3 | DATA_ROLE | 0 | RW | 0b: UFP<br>1b: DFP |
| | | 2:1 | USBPD_SPECREV | 01 | RW | 00b: Revision 1.0<br>01b: Revision 2.0<br>10b: Revision 3.0<br>11b: Reserved |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| | | 0 | POWER_ROLE | 0 | RW | 0b: Sink<br>1b: Source |
| 0x2F | RECEIVE_DETECT | 7 | Reserved | 0 | R | Not support |
| | | 6 | EN_CABLE_RST | 0 | RW | 0b : HUSB311 does not detect Cable Reset signaling (default)<br>1b : HUSB311 detects Cable Reset signaling |
| | | 5 | EN_HARD_RST | 0 | RW | 0b: HUSB311 does not detect Hard Reset signaling (default)<br>1b : HUSB311 detects Hard Reset signaling |
| | | 4 | EN_SOP2DB | 0 | RW | 0b: HUSB311 does not detect SOP_DBG'' message (default)<br>1b : HUSB311 detects SOP_DBG'' message |
| | | 3 | EN_SOP1DB | 0 | RW | 0b : HUSB311 does not detect SOP_DBG' message (default)<br>1b : HUSB311 detects SOP_DBG' message |
| | | 2 | EN_SOP2 | 0 | RW | 0b : HUSB311 does not detect SOP'' message (default)<br>1b : HUSB311 detects SOP'' message |
| | | 1 | EN_SOP1 | 0 | RW | 0b : HUSB311 does not detect SOP' message (default)<br>1b : HUSB311 detects SOP' message |
| | | 0 | EN_SOP | 0 | RW | 0b : HUSB311 does not detect SOP message (default)<br>1b : HUSB311 detects SOP message |
| 0x30 | RX_BYTE_COUNT | 7:0 | RX_BYTE_COUNT | 0 | R | This register indicates the number of bytes in the RX_BUF_BYTEx registers plus one which means the register counts from Reg0x31 to the register stored the last data byte. It is cleared as 0 when Alert.RX_SOP_MSG_STATUS is cleared. The value in this register should be less than or equal to 31.<br>When a CableReset is received, this register value is 0x01 |
| 0x31 | RX_BUF_FRAME_TYPE | 7:3 | Reserved | 0 | R | |
| | | 2:0 | RX_FRAME_TYPE | 0 | R | Type of received frame<br>000b : Received SOP<br>001b : Received SOP'<br>010b : Received SOP''<br>011b : Received SOP_DBG'<br>100b : Received SOP_DBG''<br>110b : Received Cable Reset<br>111b: Reserved |
| 0x32 | RX_BUF_BYTE0 | 7:0 | RX_HEAD_0 | 0 | R | Byte 0 (bits 7..0) of message header |
| 0x33 | RX_BUF_BYTE1 | 7:0 | RX_HEAD_1 | 0 | R | Byte 1 (bits 15..8) of message header |
| 0x34 | RX_BUF_BYTE2 | 7:0 | RX_OBJ1_0 | 0 | R | Byte 0 (bits 7..0) of 1st data object |
| 0x35 | RX_BUF_BYTE3 | 7:0 | RX_OBJ1_1 | 0 | R | Byte 1 (bits 15..8) of 1st data object |
| 0x36 | RX_BUF_BYTE4 | 7:0 | RX_OBJ1_2 | 0 | R | Byte 2 (bits 23..16) of 1st data object |
| 0x37 | RX_BUF_BYTE5 | 7:0 | RX_OBJ1_3 | 0 | R | Byte 3 (bits 31..24) of 1st data object |
| 0x38 | RX_BUF_BYTE6 | 7:0 | RX_OBJ2_0 | 0 | R | Byte 0 (bits 7..0) of 2nd data object |
| 0x39 | RX_BUF_BYTE7 | 7:0 | RX_OBJ2_1 | 0 | R | Byte 1 (bits 15..8) of 2nd data object |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| 0x3A | RX_BUF_BYTE8 | 7:0 | RX_OBJ2_2 | 0 | R | Byte 2 (bits 23..16) of 2nd data object |
| 0x3B | RX_BUF_BYTE9 | 7:0 | RX_OBJ2_3 | 0 | R | Byte 3 (bits 31..24) of 2nd data object |
| 0x3C | RX_BUF_BYTE10 | 7:0 | RX_OBJ3_0 | 0 | R | Byte 0 (bits 7..0) of 3rd data object |
| 0x3D | RX_BUF_BYTE11 | 7:0 | RX_OBJ3_1 | 0 | R | Byte 1 (bits 15..8) of 3rd data object |
| 0x3E | RX_BUF_BYTE12 | 7:0 | RX_OBJ3_2 | 0 | R | Byte 2 (bits 23..16) of 3rd data object |
| 0x3F | RX_BUF_BYTE13 | 7:0 | RX_OBJ3_3 | 0 | R | Byte 3 (bits 31..24) of 3st data object |
| 0x40 | RX_BUF_BYTE14 | 7:0 | RX_OBJ4_0 | 0 | R | Byte 0 (bits 7..0) of 4th data object |
| 0x41 | RX_BUF_BYTE15 | 7:0 | RX_OBJ4_1 | 0 | R | Byte 1 (bits 15..8) of 4th data object |
| 0x42 | RX_BUF_BYTE16 | 7:0 | RX_OBJ4_2 | 0 | R | Byte 2 (bits 23..16) of 4th data object |
| 0x43 | RX_BUF_BYTE17 | 7:0 | RX_OBJ4_3 | 0 | R | Byte 3 (bits 31..24) of 4th data object |
| 0x44 | RX_BUF_BYTE18 | 7:0 | RX_OBJ5_0 | 0 | R | Byte 0 (bits 7..0) of 5th data object |
| 0x45 | RX_BUF_BYTE19 | 7:0 | RX_OBJ5_1 | 0 | R | Byte 1 (bits 15..8) of 5th data object |
| 0x46 | RX_BUF_BYTE20 | 7:0 | RX_OBJ5_2 | 0 | R | Byte 2 (bits 23..16) of 5th data object |
| 0x47 | RX_BUF_BYTE21 | 7:0 | RX_OBJ5_3 | 0 | R | Byte 3 (bits 31..24) of 5th data object |
| 0x48 | RX_BUF_BYTE22 | 7:0 | RX_OBJ6_0 | 0 | R | Byte 0 (bits 7..0) of 6th data object |
| 0x49 | RX_BUF_BYTE23 | 7:0 | RX_OBJ6_1 | 0 | R | Byte 1 (bits 15..8) of 6th data object |
| 0x4A | RX_BUF_BYTE24 | 7:0 | RX_OBJ6_2 | 0 | R | Byte 2 (bits 23..16) of 6th data object |
| 0x4B | RX_BUF_BYTE25 | 7:0 | RX_OBJ6_3 | 0 | R | Byte 3 (bits 31..24) of 6st data object |
| 0x4C | RX_BUF_BYTE26 | 7:0 | RX_OBJ7_0 | 0 | R | Byte 0 (bits 7..0) of 7th data object |
| 0x4D | RX_BUF_BYTE27 | 7:0 | RX_OBJ7_1 | 0 | R | Byte 1 (bits 15..8) of 7th data object |
| 0x4E | RX_BUF_BYTE28 | 7:0 | RX_OBJ7_2 | 0 | R | Byte 2 (bits 23..16) of 7th data object |
| 0x4F | RX_BUF_BYTE29 | 7:0 | RX_OBJ7_3 | 0 | R | Byte 3 (bits 31..24) of 7th data object |
| 0x50 | TX_BUF_FRAME_TYPE | 7:6 | Reserved | 0 | R | Not support |
| | | 5:4 | TX_RETRY_CNT | 0 | RW | 00b: No message retry is required<br>01b: Automatically retry message transmission once<br>10b: Automatically retry message transmission twice<br>11b: Automatically retry message transmission three times |
| | | 3 | Reserved | 0 | R | Not support |
| | | 2:0 | TX_FRAME_TYPE | 0 | RW | 000b: Transmit SOP<br>001b: Transmit SOP'<br>010b: Transmit SOP"<br>011b: Transmit SOP_DBG'<br>100b: Transmit SOP_DBG"<br>101b: Transmit Hard Reset<br>110b: Transmit Cable Reset<br>111b: Transmit BIST Carrier Mode 2 (HUSB311 shall exit the BIST mode no later than tBISTContMode max). |
| 0x51 | TX_BYTE_COUNT | 7:0 | TX_BYTE_COUNT | 0 | RW | The number of bytes the TCPM will write |
| 0x52 | TX_BUF_BYTE0 | 7:0 | TX_HEAD_0 | 0 | RW | Byte 0 (bits 7..0) of message header |
| 0x53 | TX_BUF_BYTE1 | 7:0 | TX_HEAD_1 | 0 | RW | Byte 1 (bits 15..8) of message header |
| 0x54 | TX_BUF_BYTE2 | 7:0 | TX_OBJ1_0 | 0 | RW | Byte 0 (bits 7..0) of 1st data object |
| 0x55 | TX_BUF_BYTE3 | 7:0 | TX_OBJ1_1 | 0 | RW | Byte 1 (bits 15..8) of 1st data object |
| 0x56 | TX_BUF_BYTE4 | 7:0 | TX_OBJ1_2 | 0 | RW | Byte 2 (bits 23..16) of 1st data object |
| 0x57 | TX_BUF_BYTE5 | 7:0 | TX_OBJ1_3 | 0 | RW | Byte 3 (bits 31..24) of 1st data object |
| 0x58 | TX_BUF_BYTE6 | 7:0 | TX_OBJ2_0 | 0 | RW | Byte 0 (bits 7..0) of 2nd data object |

| Add | Register Name | Bit | Filed | Default | Type | Description |
|---|---|---|---|---|---|---|
| 0x59 | TX_BUF_BYTE7 | 7:0 | TX_OBJ2_1 | 0 | RW | Byte 1 (bits 15..8) of 2nd data object |
| 0x5A | TX_BUF_BYTE8 | 7:0 | TX_OBJ2_2 | 0 | RW | Byte 2 (bits 23..16) of 2nd data object |
| 0x5B | TX_BUF_BYTE9 | 7:0 | TX_OBJ2_3 | 0 | RW | Byte 3 (bits 31..24) of 2nd data object |
| 0x5C | TX_BUF_BYTE10 | 7:0 | TX_OBJ3_0 | 0 | RW | Byte 0 (bits 7..0) of 3rd data object |
| 0x5D | TX_BUF_BYTE11 | 7:0 | TX_OBJ3_1 | 0 | RW | Byte 1 (bits 15..8) of 3rd data object |
| 0x5E | TX_BUF_BYTE12 | 7:0 | TX_OBJ3_2 | 0 | RW | Byte 2 (bits 23..16) of 3rd data object |
| 0x5F | TX_BUF_BYTE13 | 7:0 | TX_OBJ3_3 | 0 | RW | Byte 3 (bits 31..24) of 3rd data object |
| 0x60 | TX_BUF_BYTE14 | 7:0 | TX_OBJ4_0 | 0 | RW | Byte 0 (bits 7..0) of 4th data object |
| 0x61 | TX_BUF_BYTE15 | 7:0 | TX_OBJ4_1 | 0 | RW | Byte 1 (bits 15..8) of 4th data object |
| 0x62 | TX_BUF_BYTE16 | 7:0 | TX_OBJ4_2 | 0 | RW | Byte 2 (bits 23..16) of 4th data object |
| 0x63 | TX_BUF_BYTE17 | 7:0 | TX_OBJ4_3 | 0 | RW | Byte 3 (bits 31..24) of 4th data object |
| 0x64 | TX_BUF_BYTE18 | 7:0 | TX_OBJ5_0 | 0 | RW | Byte 0 (bits 7..0) of 5th data object |
| 0x65 | TX_BUF_BYTE19 | 7:0 | TX_OBJ5_1 | 0 | RW | Byte 1 (bits 15..8) of 5th data object |
| 0x66 | TX_BUF_BYTE20 | 7:0 | TX_OBJ5_2 | 0 | RW | Byte 2 (bits 23..16) of 5th data object |
| 0x67 | TX_BUF_BYTE21 | 7:0 | TX_OBJ5_3 | 0 | RW | Byte 3 (bits 31..24) of 5th data object |
| 0x68 | TX_BUF_BYTE22 | 7:0 | TX_OBJ6_0 | 0 | RW | Byte 0 (bits 7..0) of 6th data object |
| 0x69 | TX_BUF_BYTE23 | 7:0 | TX_OBJ6_1 | 0 | RW | Byte 1 (bits 15..8) of 6th data object |
| 0x6A | TX_BUF_BYTE24 | 7:0 | TX_OBJ6_2 | 0 | RW | Byte 2 (bits 23..16) of 6th data object |
| 0x6B | TX_BUF_BYTE25 | 7:0 | TX_OBJ6_3 | 0 | RW | Byte 3 (bits 31..24) of 6th data object |
| 0x6C | TX_BUF_BYTE26 | 7:0 | TX_OBJ7_0 | 0 | RW | Byte 0 (bits 7..0) of 7th data object |
| 0x6D | TX_BUF_BYTE27 | 7:0 | TX_OBJ7_1 | 0 | RW | Byte 1 (bits 15..8) of 7th data object |
| 0x6E | TX_BUF_BYTE28 | 7:0 | TX_OBJ7_2 | 0 | RW | Byte 2 (bits 23..16) of 7th data object |
| 0x6F | TX_BUF_BYTE29 | 7:0 | TX_OBJ7_3 | 0 | RW | Byte 3 (bits 31..24) of 7th data object |

# PACKAGE OUTLINE DIMENSIONS

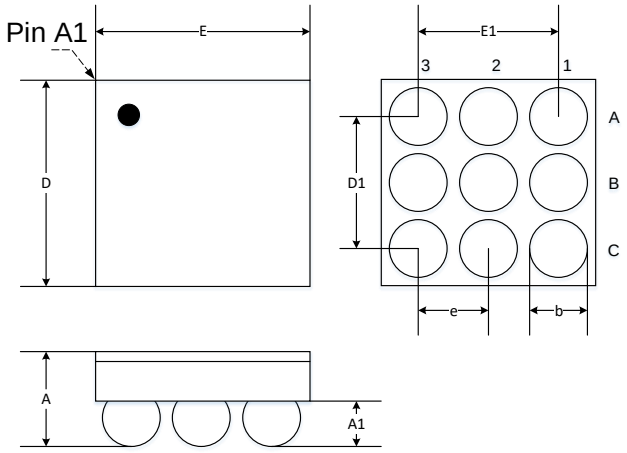
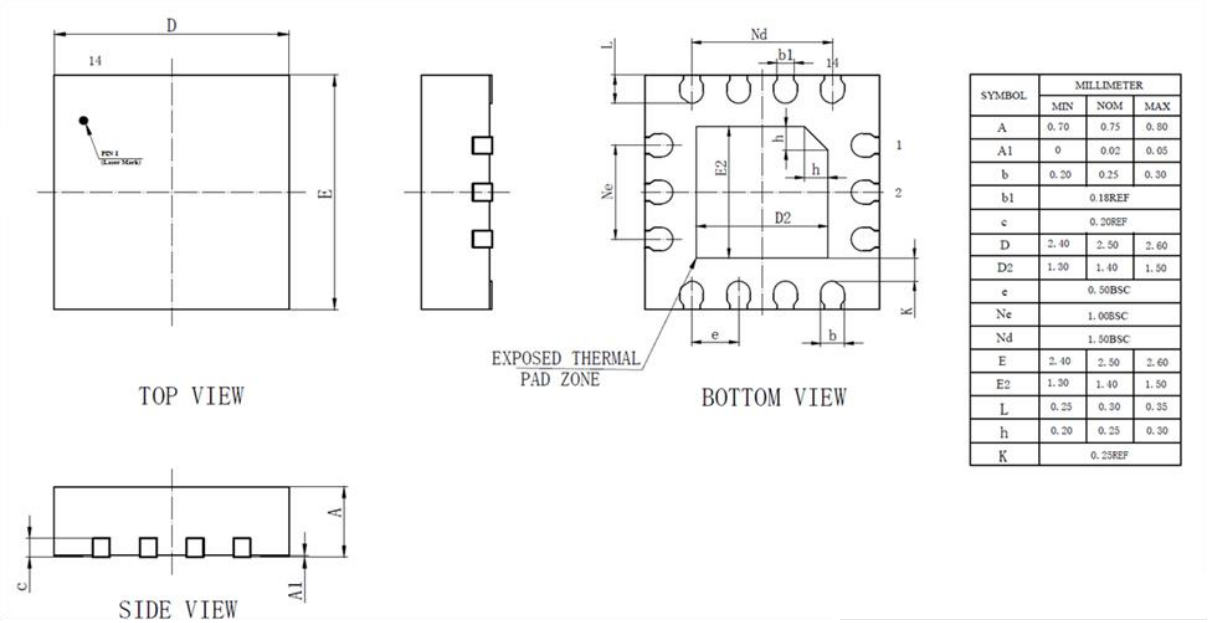



*Figure 6. HUSB311_ACC Dimension*

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max. |
| A | 0.512 | 0.588 | 0.020 | 0.023 |
| A1 | 0.178 | 0.218 | 0.007 | 0.009 |
| b | 0.245 | 0.285 | 0.010 | 0.012 |
| D | 1.330 | 1.380 | 0.052 | 0.054 |
| D1 | 0.800 | | 0.031 | |
| E | 1.380 | 1.430 | 0.054 | 0.056 |
| E1 | 0.800 | | 0.031 | |
| e | 0.400 | | 0.016 | |




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.18REF | | |
| c | 0.20REF | | |
| D | 2.40 | 2.50 | 2.60 |
| D2 | 1.30 | 1.40 | 1.50 |
| e | 0.50BSC | | |
| Ne | 1.00BSC | | |
| Nd | 1.50BSC | | |
| E | 2.40 | 2.50 | 2.60 |
| E2 | 1.30 | 1.40 | 1.50 |
| L | 0.25 | 0.30 | 0.35 |
| h | 0.20 | 0.25 | 0.30 |
| K | 0.25REF | | |

*Figure 7. HUSB311_BLA Dimension*

# PACKAGE TOP MARKING

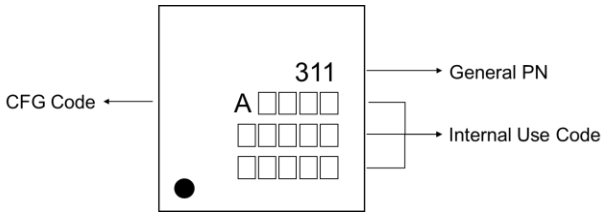



*Figure 8. HUSB311_ACC Package Top Marking*

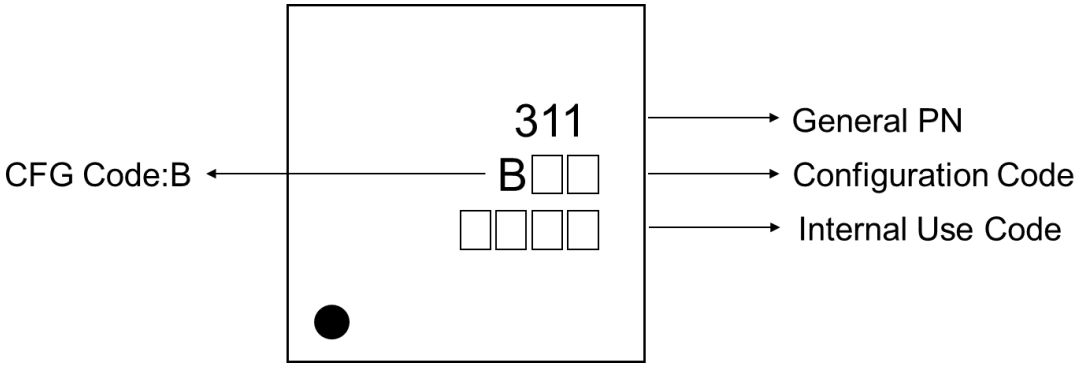



*Figure 9. HUSB311_BLA Package Top Marking*

# ORDERING GUIDE

| Model | Temperature Range | Default Role | Package Option | Shipping Option |
|---|---|---|---|---|
| HUSB311_BLA | -40 °C -125 °C | SINK | QFN-14L | Tape and Reel, 3K |
| HUSB311_ACC | -40 °C -125 °C | SINK | WLCSP-9B | Tape and Reel, 3K |

# IMPORTANT NOTICE

Hynetek Semiconductor Co., Ltd. and its subsidiaries (Hynetek) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to Hynetek’s terms and conditions of sale supplied at the time of order acknowledgment.

Hynetek warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in Hynetek’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent Hynetek deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

Hynetek assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using Hynetek components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Hynetek does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Hynetek components or services are used. Information published by Hynetek regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Hynetek under the patents or other intellectual property of Hynetek.

Reproduction of significant portions of Hynetek information in Hynetek data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Hynetek is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of Hynetek components or services with statements different from or beyond the parameters stated by Hynetek for that component or service voids all express and any implied warranties for the associated Hynetek component or service and is an unfair and deceptive business practice.

Hynetek is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Hynetek components in its applications, notwithstanding any applications-related information or support that may be provided by Hynetek. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify Hynetek and its representatives against any damages arising out of the use of any Hynetek components in safety-critical applications.

In some cases, Hynetek components may be promoted specifically to facilitate safety-related applications. With such components, Hynetek’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No Hynetek components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those Hynetek components which Hynetek has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of Hynetek components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Hynetek has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, Hynetek will not be responsible for any failure to meet ISO/TS16949.

Please refer to below URL for other products and solutions of Hynetek Semiconductor Co., Ltd.