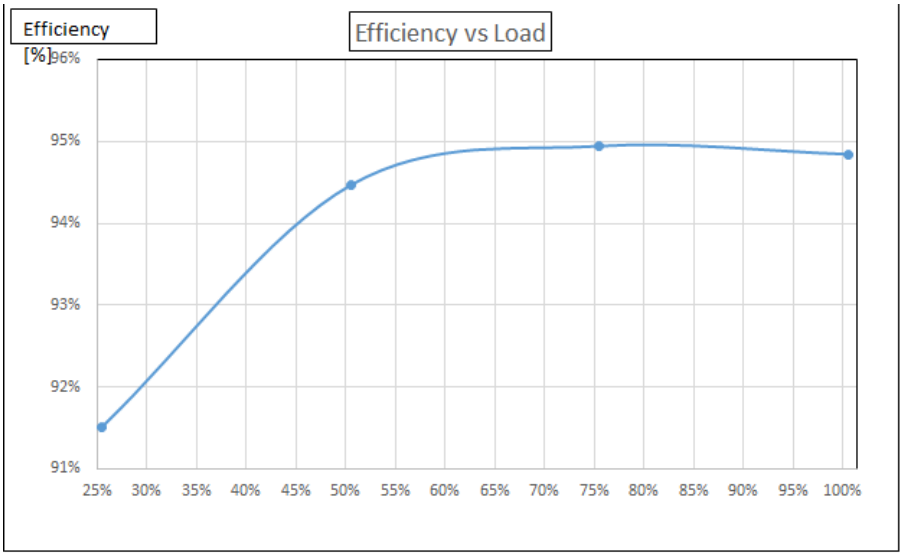
5 EVLMG1-250WLLC performance and efficiency measurement

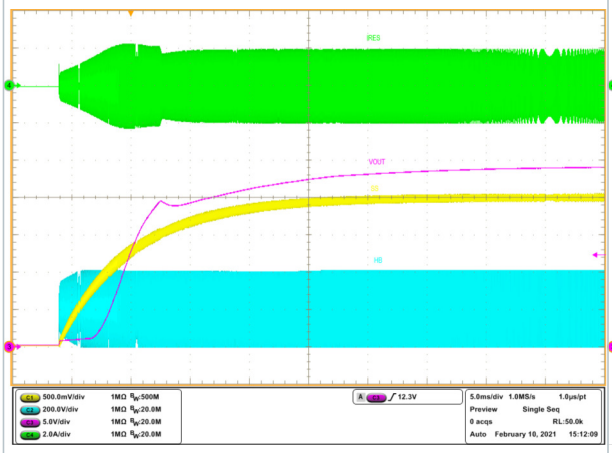
Figure 18. **EVLMG1-250WLLC efficiency**



In the above diagram the Efficiency measured from a 25% to 100% load is reported. At maximum output power the measured efficiency is over 94%.

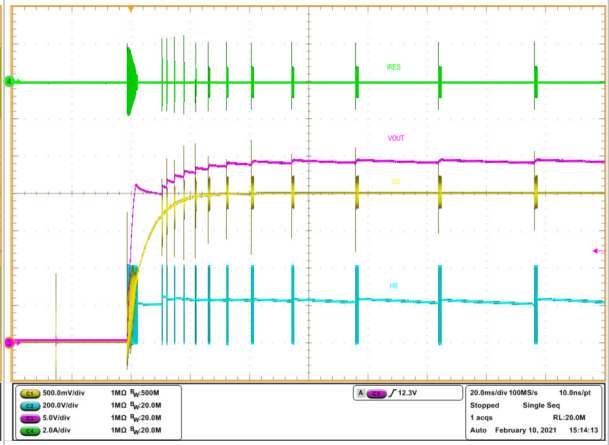
6 EVLMG1-250WLLC waveforms

Figure 19. Startup @ full load



Ch.1: Soft start pin; Ch.2: Half bridge; Ch.3: VOUT;
Ch.4: Resonant current

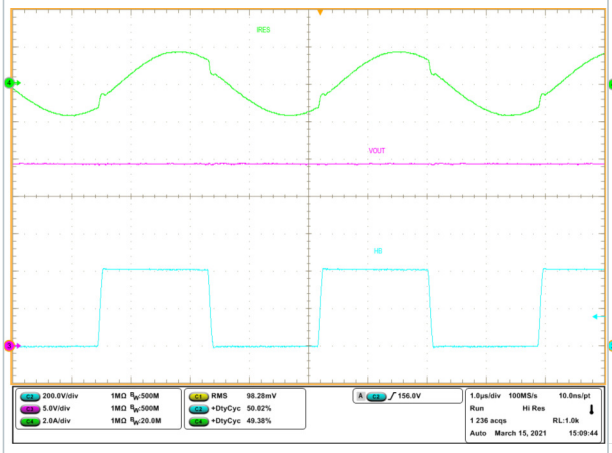
Figure 20. Startup @ no load



Ch.1: Soft start pin; Ch.2: Half bridge; Ch.3: VOUT;
Ch.4: Resonant current

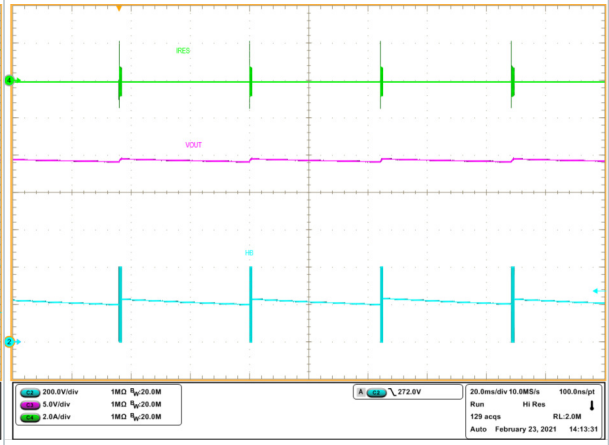
Figure 19 and Figure 20 show the startup operation in both full load and no load conditions.

Figure 21. Steady-state 8A load



Ch.2: Half bridge; Ch.3: VOUT; Ch.4: Resonant current

Figure 22. Steady-state @ no load

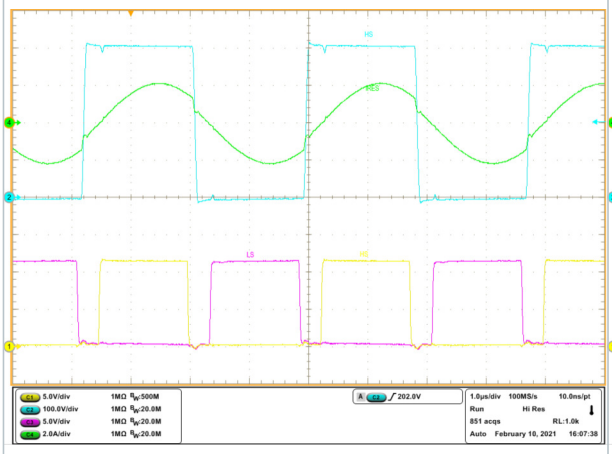


Ch.2: Half Bridge; Ch.3: VOUT; Ch.4: Resonant current

Figure 21 and Figure 22 show the steady-state operations at 8A and no load conditions (burst mode).

Figure 23 and Figure 24 show the steady-state conditions at full and half load: HVG and LVG signals from the L6599A are shown as reference.

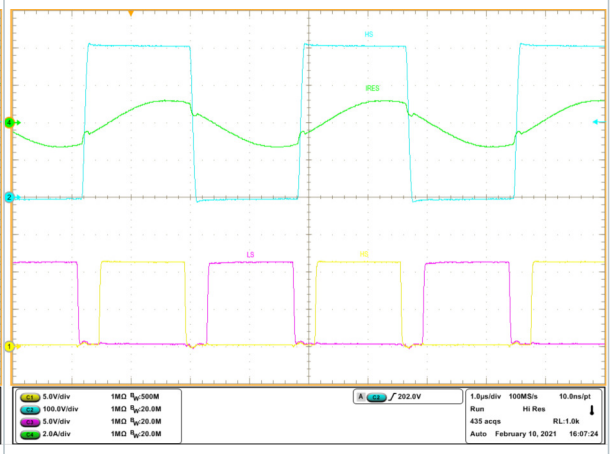
Figure 23. Switching activity steady-state FL



Ch.1: HVG; Ch.2: Half bridge voltage; Ch.3: LVG;

Ch.4: Resonant tank current

Figure 24. Switching activity steady-state HL

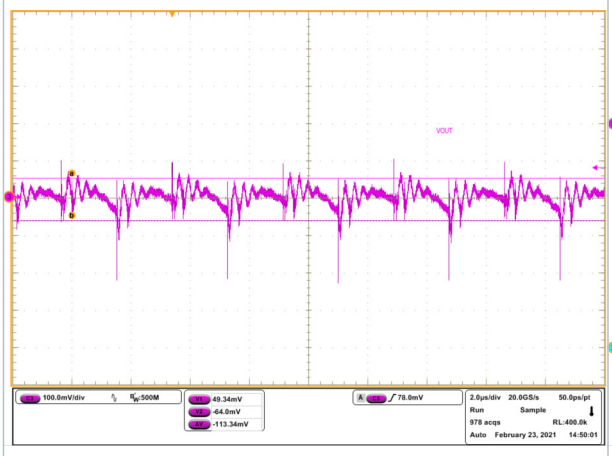


Ch.1: HVG; Ch.2: Half bridge voltage; Ch.3: LVG;

Ch.4: Resonant tank current

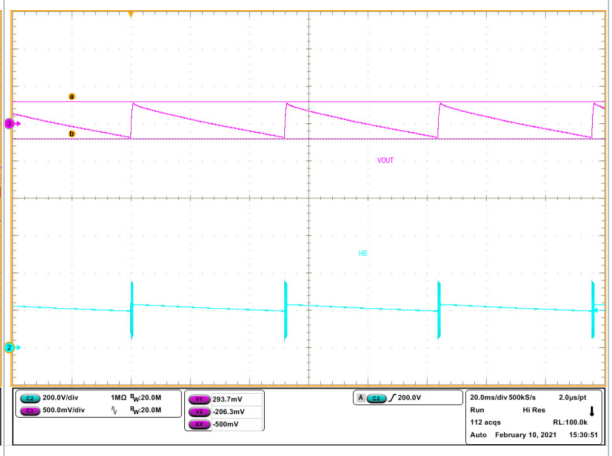
Figure 25 and Figure 26 show the output voltage ripple. The Vpeak to peak ripple are 120 mV at full load and 500 mV at no load during burst mode operation.

Figure 25. Vout ripple full load



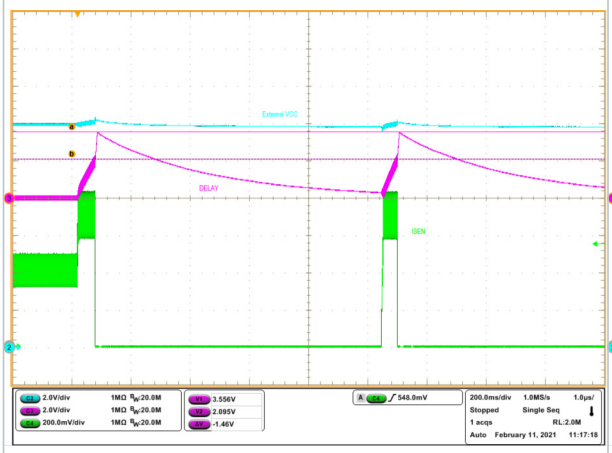
Ch.3: VOUT ripple

Figure 26. Vout ripple no load



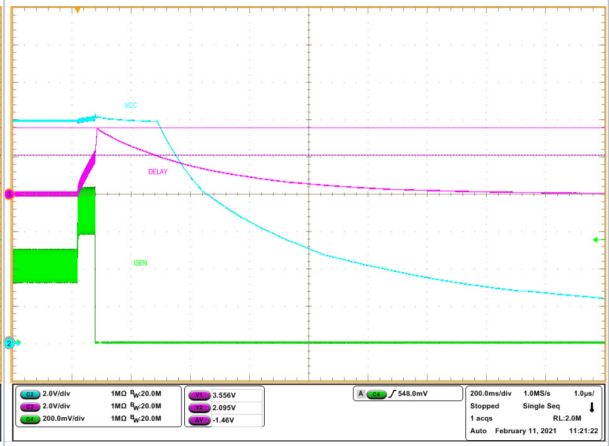
Ch.2: Half bridge; Ch.3: VOUT ripple

Figure 27. Overcurrent protection with ext. VCC



Ch.2: external VCC; Ch.3: Delay pin; Ch.4: ISEN pin

Figure 28. Overcurrent protection without ext. VCC

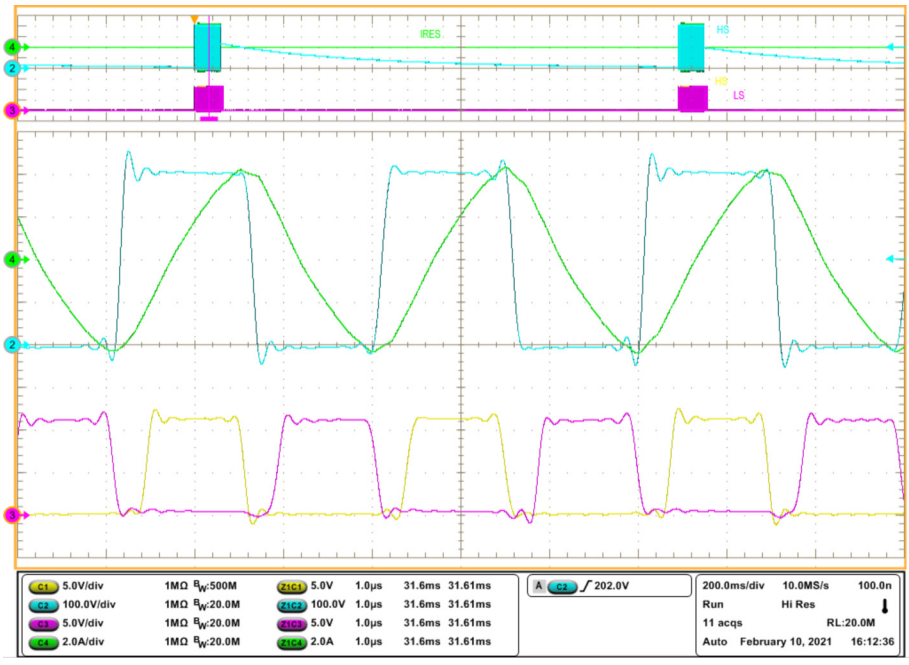


Ch.2: VCC; Ch.3: Delay pin; Ch.4: ISEN pin

The EVLMG1-250WLLC evaluation board is protected by short-circuit or overcurrent which might occur, preventing component overheating or catastrophic failures of the board. Figure 27 and Figure 28 show the safe interruption of switching activity. In Figure 27, since the board is supplied by an external Vcc, it can be observed that the board starts working in hiccup mode until the short is removed. Then it restarts via a soft-start cycle. In Figure 28, since the external Vcc is removed and the board is self supplied, we can see that after the short is applied the converter works for a short time then it stops the operation because the Vcc is lost and the converter cannot restart. To resume operation it is necessary to reconnect the external Vcc allowing the board startup.

Figure 29 shows the significant waveforms of hiccup mode in short-circuit condition.

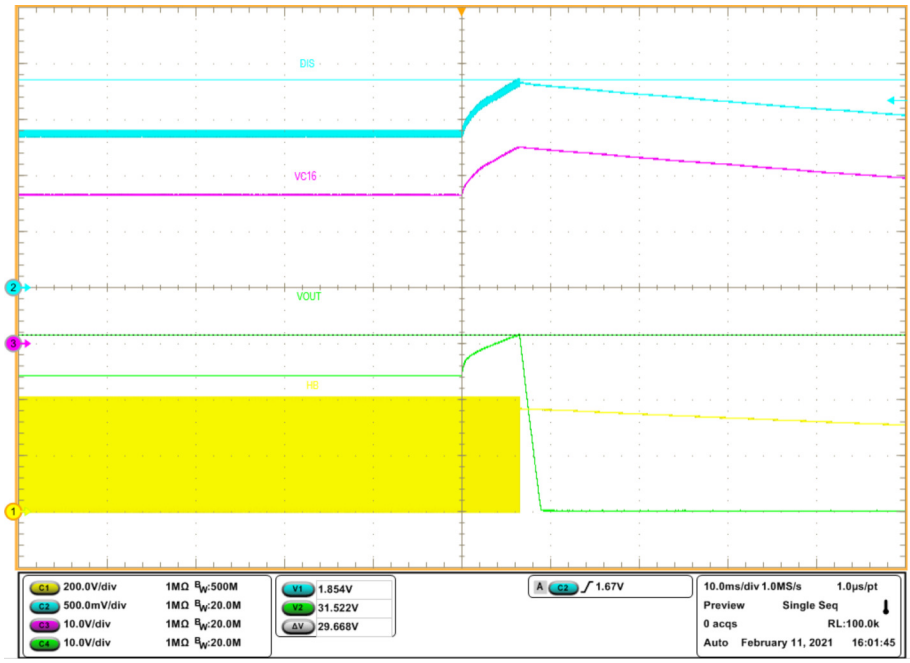
Figure 29. OCP switching activity detail



Ch.1: HVG; Ch.2: Half bridge; Ch.3: LVG; Ch.4: Resonant current

An additional protection of the EVLMG1-250WLLC evaluation board is the open loop failures protection, sensing the auxiliary voltage. As shown in Figure 29, in case of output voltage loop fail, the auxiliary voltage Vaux rises and once the voltage on the DIS pin has reached the 1.85 V threshold, the L6599A stops operation and latches the switching activity. The converter operation is resumed after the Vcc has dropped below the UVLO threshold. The measured Vout is 31.5 V, below the maximum voltage rating of the output capacitors.

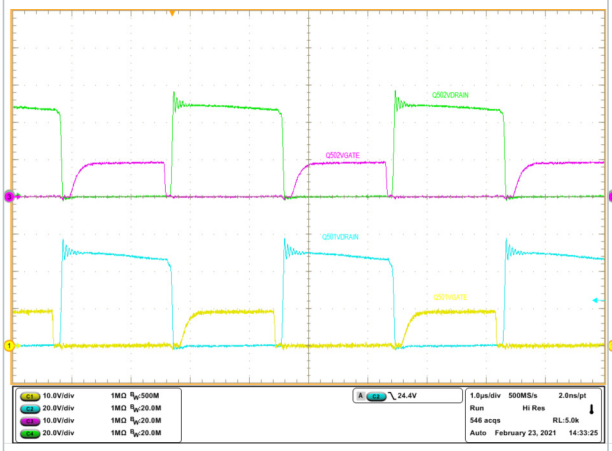
Figure 30. Overvoltage protection



Ch.1: Half bridge; Ch.2: L6599A DIS pin; Ch.3: VC16; Ch.4: VOUT

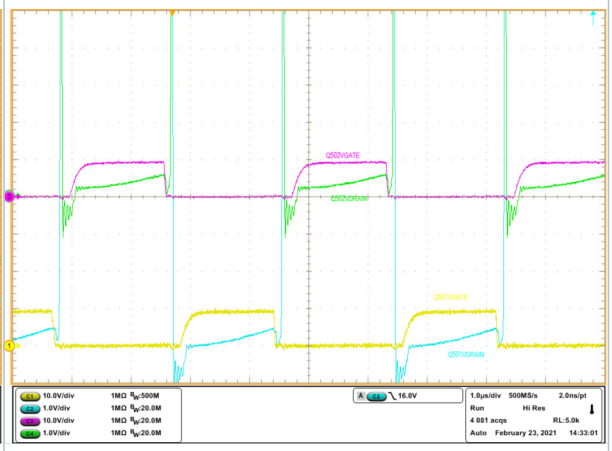
Figure 31 shows the drain and gate voltages of secondary MOSFETs driven by the SRK2001, synchronous rectifier controller. Figure 32 shows the detail of the secondary MOSFET's drain voltage. The voltage drop variation before and after each MOSFET turn-on and turn-off.

Figure 31. SR waveforms



Ch.1: Q501 gate voltage; Ch.2: Q501 drain voltage;
Ch.3: Q502 gate voltage; Ch.4: Q502 drain voltage

Figure 32. SR drain voltage detail



Ch.1: Q501 gate voltage; Ch.2: Q501 drain voltage;
Ch.3: Q502 gate voltage; Ch.4: Q502 drain voltage