Three-Phase PMSM/BLDC Motor Controller with Pre-Driver

General Description

The RT7080 is a highly integrated power module designed for advanced motor drive applications. It consists of a 3-phase motor controller, a gate driver, six MOSFETs, a 5V LDO, a charge pump circuit, a buck converter and 3 current sense resistors designed for PMSM/BLDC motor applications.

The RT7080 is of great benefit to users such as cost effectiveness, easy design, board space saving with features and better quality control.

The RT7080 integrates the ARM 32-bit Cortex-M0 core with peripheral circuits to perform field oriented control (FOC) and sensorless motor control. In additions, system level peripheral functions, such as ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, undervoltage-lockout (UVLO), short circuit protection (SCP) and locked-rotor protection are integrated so as to reduce component count, PCB size and system cost. Furthermore, the RT7080 drives internal N-Channel MOSFETs in three half-bridge configuration with a build-in charge pump circuit up to 28V. The RT7080 is available in WQFN-40L 6x6 packages.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

- **Input Voltage Range : 8V to 28V**
- **Drive Current : 3.5A Peak**
- **Sensor-Less, Sine-Wave Field Oriented Control (FOC)**
- **No External Sense Resistors Required**
- **Integrated Buck Converter and 5V LDO**
- **ARM 32-bit Cortex-M0 CPU, Frequency up to 60MHz**
- **Communication Interface : I^2C and UART**
- **Protections : SCP, OVP, UVP and Locked-Rotor Detection**
- **WQFN-40L 6x6 Pin**

Applications

- Pedestal Fan
- Ventilation Fan
- Robot Vacuum Cleaner
- Water Pump

Ordering Information

RT7080□□-□□□□□

- □□□□□ : Programmed Firmware Code
- □□ : Package Type
  - QW : WQFN-40L 6x6 (W-Type) (Exposed Pad-Option 1)
- □ : Lead Plating System
  - G : Green (Halogen Free and Pb Free)

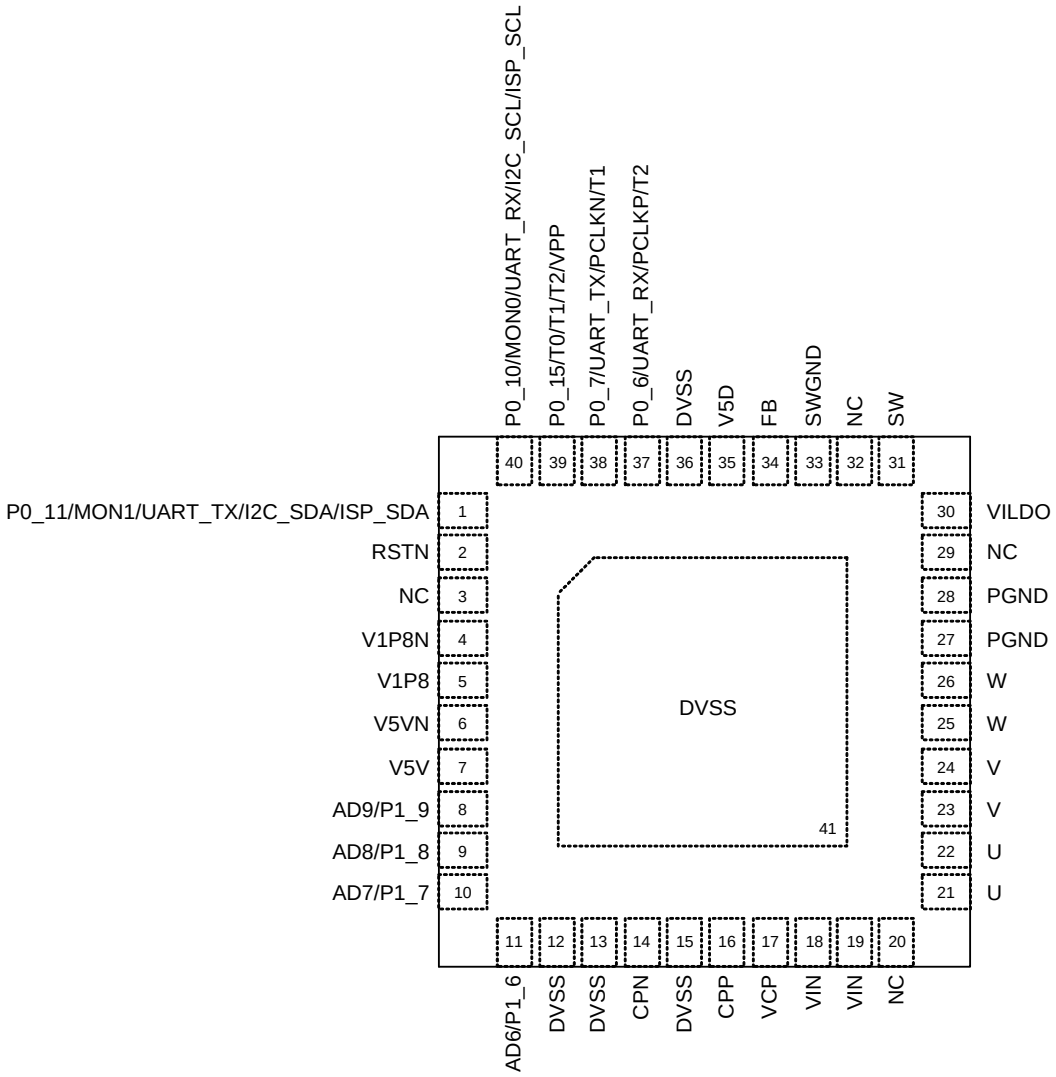
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



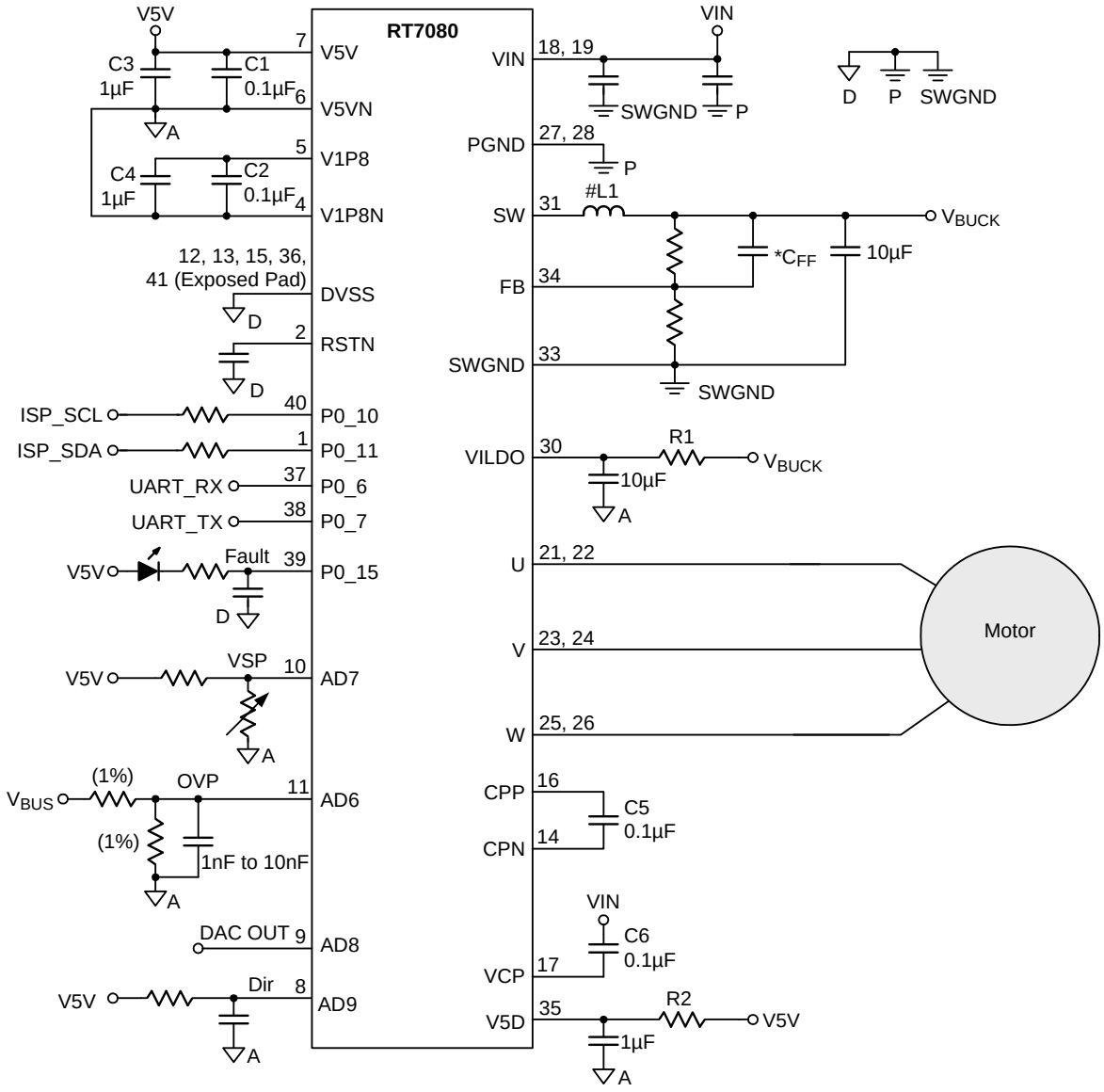
WQFN-40L 6x6

Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	P0_11	DIO	Pin 11 of GPIO port 0.
	MON1	DO	Internal digital signal monitoring output pin.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DIO	I^2C data pin.
	ISP_SDA	DIO	In system programming data input pin.
2	RSTN	DI	Pad reset pin.
3, 20, 29, 32	NC	--	No internal connection.
4	V1P8N	GND	1.8V power pin negative terminal.
12, 13, 15, 36, 41 (Exposed Pad)	DVSS	GND	Digital ground. The thermal pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.
5	V1P8	P	1.8V power pin for internal operation voltage.
6	V5VN	GND	5V power pin negative terminal.
7	V5V	P	5V power pin.
8	AD9	AIO	ADC channel 9 input pin.
	AD9	AIO	Current type DAC input pin. (Sink type)
	P1_9	DIO	Pin 9 of GPIO port 1.
9	AD8	AIO	ADC channel 8 input pin.
	AD8	AIO	Voltage type DAC output pin.
	P1_8	DIO	Pin 8 of GPIO port 1.
10	AD7	AIO	ADC channel 7 input pin.
	P1_7	DIO	Pin 7 of GPIO port 1.
11	AD6	AIO	ADC channel 6 input pin.
	P1_6	DIO	Pin 6 of GPIO port 1.
14	CPN	P	Charge pump pin 1, use a ceramic capacitor between CPN and CPP
16	CPP	P	Charge pump pin 2, use a ceramic capacitor between CPN and CPP
17	VCP	P	Charge pump output pin
18, 19	VIN	VI	Input supply voltage
21, 22	U	VO	Output for U-Phase.
23, 24	V	VO	Output for V-Phase.
25, 26	W	VO	Output for W-Phase.
27, 28	PGND	GND	Power ground for gate driver and MOSFETs.
30	VILDO	P	Internal LDO input pin.
31	SW	VO	Switch node. Connect the switching node to external inductor.
33	SWGND	GND	Switch GND for internal buck converter.

Pin No.	Pin Name	Type	Pin Function
34	FB	AIO	Feedback pin of internal buck converter
35	V5D	P	Connect a resistor between this pin and V5V pin.
37	P0_6	DIO	Pin 6 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	PCLKP	DO	Programmable clock positive output pin.
	T2	DI	T2 external enable or external clock input pin.
38	P0_7	DIO	Pin 7 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	PCLKN	DO	Programmable clock negative output pin.
	P1	DI	T1 external enable or external clock input pin.
39	P0_15	DIO	Pin 15 of GPIO port 0.
	T0	DI	T0 external enable or external clock input pin.
	T1	DI	T1 external enable or external clock input pin.
	T2	DI	T2 external enable or external clock input pin.
	VPP	P	8V input power for MTP fast programming.
40	P0_10	DIO	Pin 10 of GPIO port 0.
	MON0	DO	Internal digital signal monitoring output pin.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DIO	I^2C clock pin.
	ISP_SCL	DI	In system programming clock input pin.

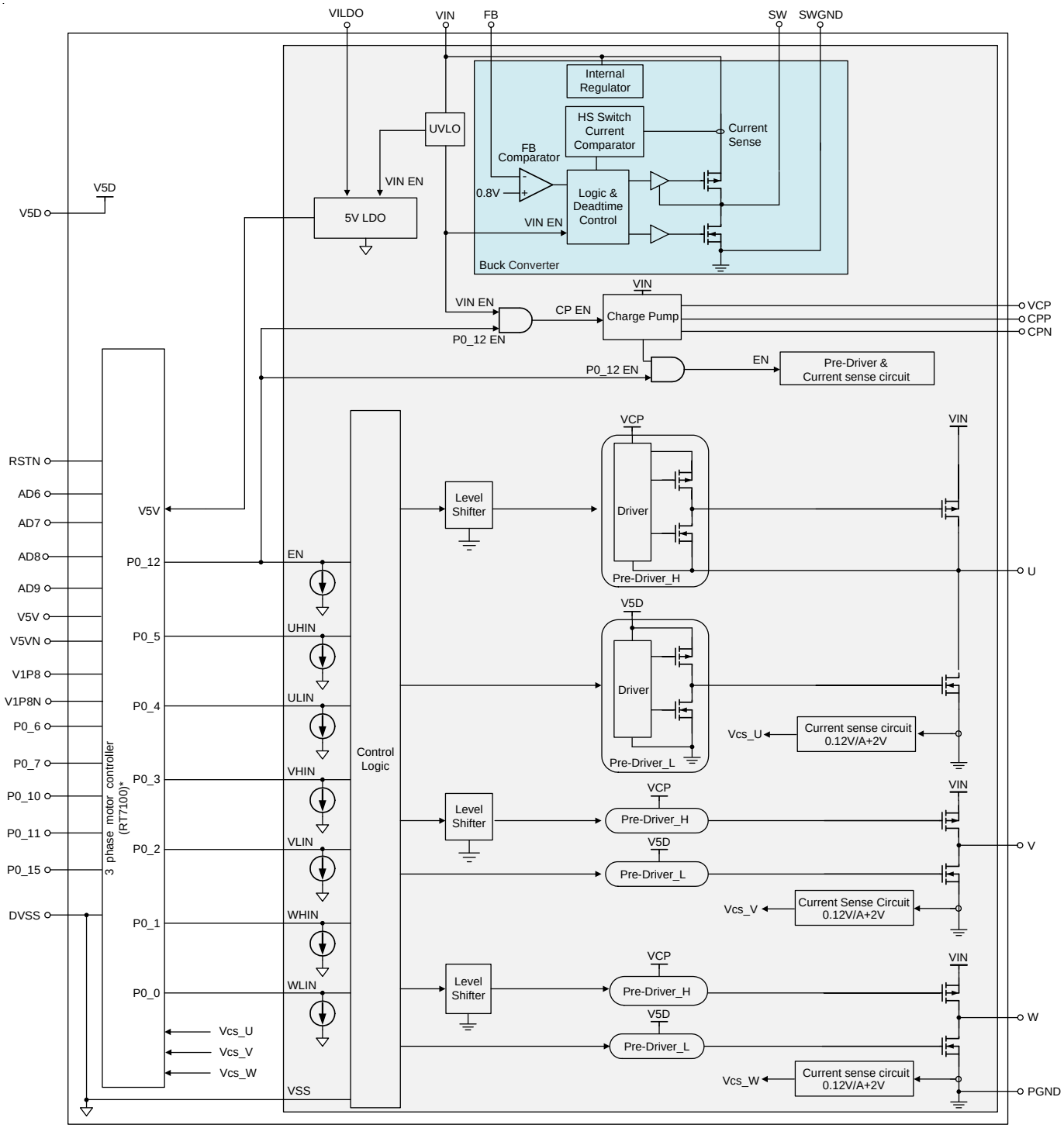
Typical Application Circuit



Note :

1. C1 , C2 , C3, C4 and L1 as close as possible to the IC.
2. C1 , C2 : option.
3. C3 , C4 : 1µF, the 5V ripple must be kept under 80mV peak to peak for full operation temperature range
4. * : Recommended C_{FF} capacitor helps to improve the output ripple voltage. Suggest value is 270pF to 470pF.
5. #: L1 suggest value is 68µH.
6. R1 , R2 : Suggest is 10Ω.

Functional Block Diagram



* : Please refer to AN_RT7100_Introduction_TW for how to use RT7100.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 30V
- U, V, W, VILDO ---------- –1V to 30V
- V5V ---------- 12V
- CPN ---------- –0.3V to 30V
- VCP, CPP ---------- –0.3V to V_{CC} + 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 6x6 ---------- 3.7W
- Package Thermal Resistance (Note 2)
  WQFN-40L 6x6, θ_{JA} ---------- 27°C/W
  WQFN-40L 6x6, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 8V to 28V
- U, V, W ---------- –0.7V to 28V
- Buck Inductor ---------- 68µH
- Buck Output Capacitor ---------- 10µF
- Charge Pump Capacitance (C5, C6) ---------- 0.1µF
- Current Sense Range ---------- 3A
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(V_{VIN} = 24V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		58.8	60	61.2	MHz
Slow Clock for Sleep Mode	f_{LCLK}		77.6	80	82.4	kHz
Power Management Section						
Turn-On Voltage of V5V	V_{V5V_ON}		--	4.15	--	V
V5V On-Off Hysteresis	V_{V5V_HYS}	Turn-off voltage = V_{V5V_ON} - V_{V5V_hys}	--	0.3	--	V
LDO Output for Internal Operation Voltage	V_{V1P8}	Full speed operation w/i external 20mA sink, C_{V1P8} > 1µF	--	1.8	--	V
V5V Current at Operation Mode	I_{V5V_OPER}	Typical sensor-less motor control library	--	18	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V5V Current at Deep Sleep Mode	I_{V5V_DSLP}		--	400	--	μA
ADC Section (0 to 4V, 10-bit, Single End Mode, Gain = 1) (Note 5)						
ADC Input Voltage Range	V_{ADCIN}		0	--	4	V
VDAC Section (0V to 4V, 8-bit for Short and Over-Current) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}		--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}		--	4	--	V
DAC Offset	V_{OFFSET}		--	2	--	LSB
Output Resistance of DAC	R_O	(Note 7)	--	5k	--	Ω
VDAC Section (0V to 3V, 8-bit for General Purposed Comparator) (Note 5)						
Minimum Conversion Voltage	V_{O_MIN}		--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}		--	3	--	V
DAC Offset	V_{OFFSET}		--	2	--	LSB
Output Resistance of DAC	R_O	(Note 7)	--	5k	--	Ω
IDAC Section (0 to 126μA, 6-Bit for Current Sink) (Note 5)						
IDAC Output Bias Voltage Range	Vibias		0.2	--	5	V
Minimum Sink Current	I_{O_MIN}	Vibias = 2.5V	--	0	--	μA
Maximum Sink Current	I_{O_MAX}	Vibias = 2.5V	--	126	--	μA
Average Current Step	I_{LSB}	Test : (Ii_min-Ii_max) / (256-1)	--	2	--	μA
DAC Offset	I_{OFFSET}		--	0	--	μA
Current Limit Comparator Section (Short and Over-Current)						
Comparator Offset	V_{OFFSET}	(Note 6)	–10	0	10	mV
Input Voltage Range of Comparator	V_{IN}	(Note 7)	1	--	4	V
Over-Current Level Range	V_{OC}	(Note 7)	0.5	--	4	V
General Purposed Comparator (Note 6)						
Comparator Offset	V_{OFFSET}		–5	0	5	mV
Input Voltage Range of Comparator	V_{IN}		0	--	3	V
IO of P0_6 to P0_7 Section						
Input High Voltage	V_{IH}		--	--	0.7 x V5V	V
Input low Voltage	V_{IL}		0.3 x V5V	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pull-Down Resistor	R_{DOWN}		--	90	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of P0_10 to P0_11 Section						
Input High Voltage	V_{IH}		--	--	0.7 x V5V	V
Input low Voltage	V_{IL}		0.3 x V5V	--	--	V
Pull-Up Resistor	R_{UP}		--	70	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	15	--	mA
IO of AD6 to AD9 Section and P0_15						
Input High Voltage	V_{IH}		--	--	2.7	V
Input Low Voltage	V_{IL}		0.6	--	--	V
Current Source for External Bias	I_{BIAS}		--	50	--	μA
Low Level Output Current	I_{OL}		--	2	--	mA
RSTN Pin Pull-Up Resistor	R_{UP}		--	10	--	kΩ
Power Supply Section						
VIN Under-Voltage Lockout Threshold (On)	V_{THON_VIN}		--	7.2	--	V
VIN Under-Voltage Lockout Threshold (Off)	V_{THOFF_VIN}		--	6.7	--	V
VIN Standby Current (w/o MCU)	I_{Q_VIN}		--	3	4	mA
VIN Operating Current (w/o MCU)	I_{P_VIN}		--	3.5	--	mA
Buck Regulator Section						
$R_{DS(ON)}$ (High-Side)	$R_{DS(ON)\_H}$		--	3	--	Ω
$R_{DS(ON)}$ (Low-Side)	$R_{DS(ON)\_L}$		--	1.5	--	Ω
FB UVP Voltage for Over Load or SC	V_{FB_UV}	Latch function	--	0.7	--	V
UVP Blanking Time	t_{BLANK_UV}	Output cap.= 10μF	--	3.5	--	ms
FB OVP Voltage	V_{FB_OV}	Latch function	--	1.22	--	V
Feedback Comparator Trip Voltage			0.76	0.8	0.84	V
Feedback Comparator Hysteresis			--	5	--	mV
Soft-Start Period	t_S		--	1	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Side Peak Current Limit	I_{PEAK_H}		--	135	--	mA
5V LDO Section						
VILDO Input Voltage	V_{VILDO}	I_{LOAD} = 0mA to 60mA	6	--	15	V
LDO Short Current	I_{SC}		60	--	130	mA
Integrated MOSFET Section						
R_{DSON} Series Resistance (H + L)		T_A = 25°C; V_{CC} = 24V; $V_{(VCP)}$ = 29V; I_{OUT} = 1A	--	0.3	--	Ω
		T_A = 85°C; V_{CC} = 24V; $V_{(VCP)}$ = 29V; I_{OUT} = 1A	--	0.35	--	
Internal Pre-Driver Section						
Turn-On Propagation Delay	t_{ON}		--	100	--	ns
Turn-Off Propagation Delay	t_{OFF}		--	100	--	ns
Sense Resistor Section						
Current Sense Resistor	R_{CS}		--	120	--	mΩ
Current Sense Amplifier Section						
Bias Voltage		Include TC	1.9	2	2.1	V
Current Sense Range			–3.5	--	3.5	A
Maximum Output Voltage		For SCP	4	--	--	V
Charge Pump Section						
Frequency	f_{CP}		70	100	130	kHz
Charge Voltage (LDO)	V_{CP}		--	7.5	--	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

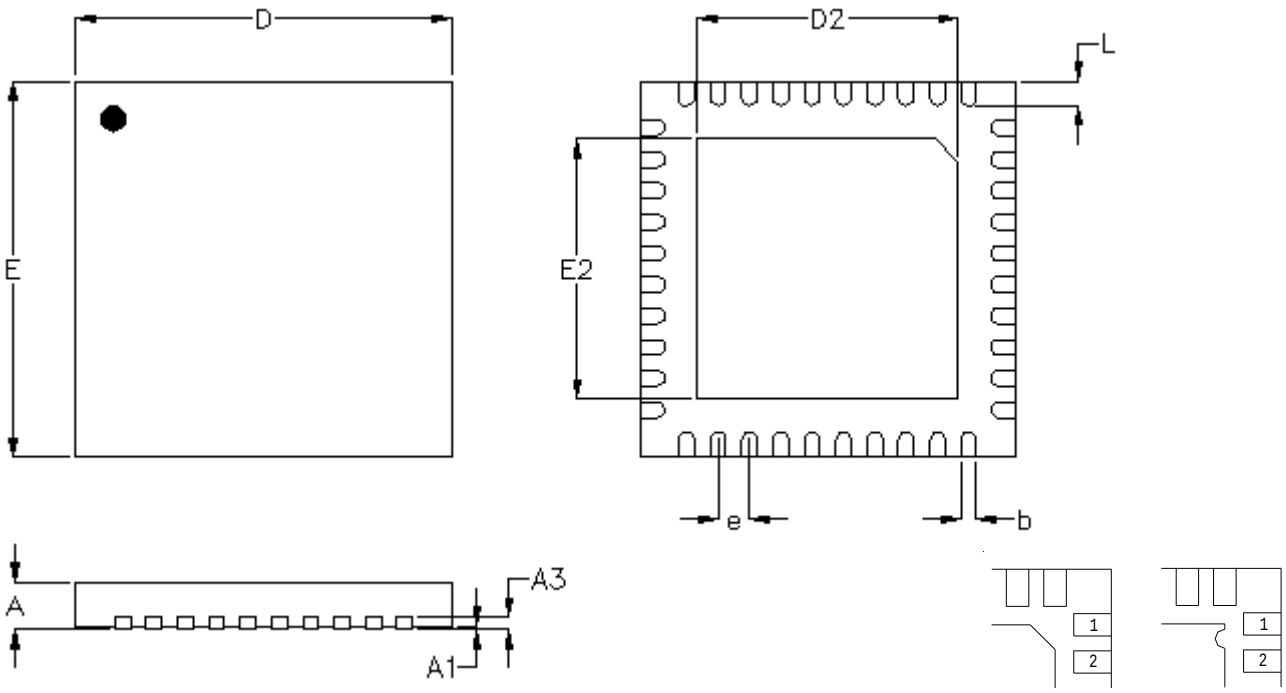
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Characterized, not tested at manufacturing.

Note 6. For comparator only.

Note 7. This parameter is guaranteed by design.

Outline Dimension



DETAIL A

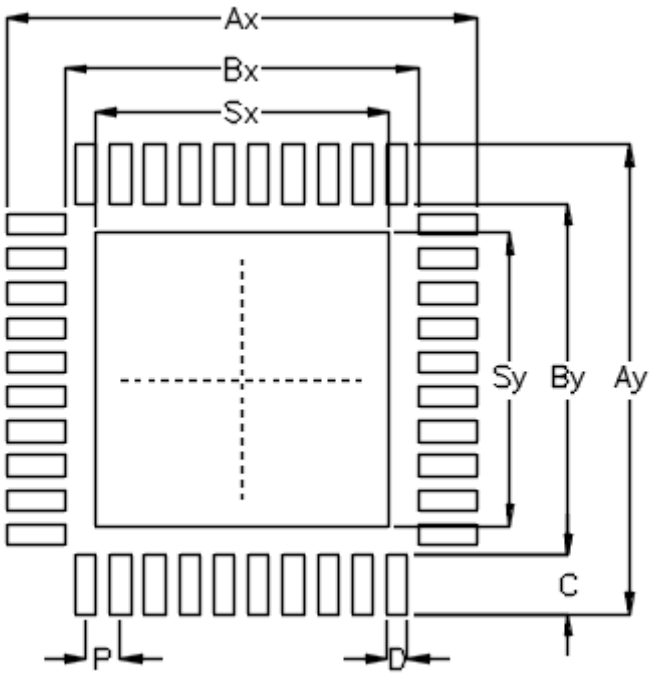
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		5.950	6.050	0.234	0.238
D2	Option1	4.000	4.750	0.157	0.187
	Option2	3.470	3.570	0.137	0.141
E		5.950	6.050	0.234	0.238
E2	Option1	4.000	4.750	0.157	0.187
	Option2	2.570	2.670	0.101	0.105
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 40L QFN 6x6 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN6*6-40	Option1	40	0.50	6.80	6.80	5.10	5.10	0.85	0.30	4.25	4.25	±0.05
	Option2									3.62	2.72	

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Datasheet Revision History

Version	Date	Item	Description
P00	2018/10/19		First Edition