## 3.2 Testing and Results

### 3.2.1 Test Results at Input 120 Vrms, 60 Hz, Output 380-V DC

#### 3.2.1.1 Startup

The startup sequence of the power stage is shown in Figure 58 with input single phase of 120 Vrms VL-N, an output bus regulated at 380 V, and a 1.6-KW load and no load.

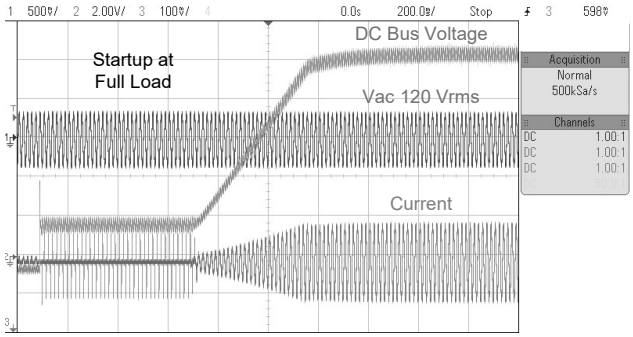


**Figure 58. Startup of PFC Operation at 120-Vac IN, 380-V DC OUT and 1.6-KW Load**

Figure 59 shows the startup under no load.

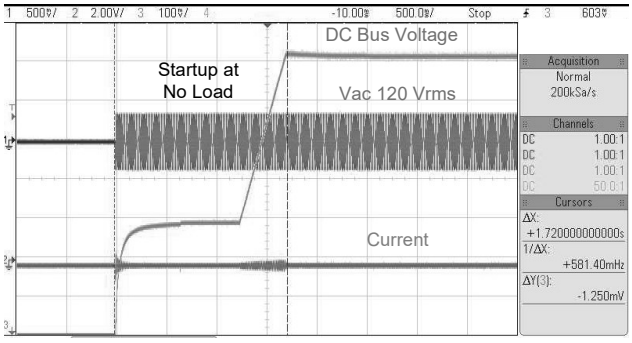


**Figure 59. Startup of PFC at 120-Vac IN, 380-V DC Output, and 0% Load**

#### 3.2.1.2 Steady State Condition

Steady state current waveforms are shown in Figure 60, Figure 61, and Figure 62 at different load conditions. Phase shedding is disabled for these readings.

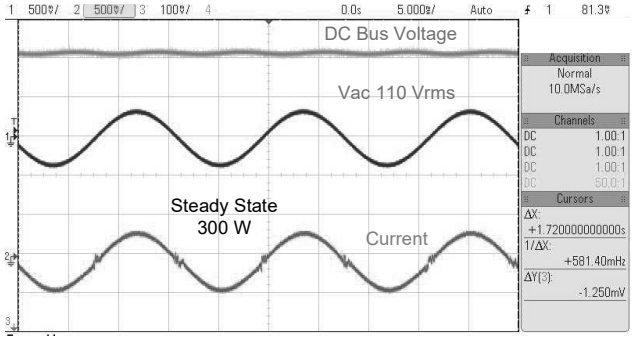


**Figure 60. Steady State 120-Vac IN, 380-V DC OUT 300W, iTHD 5.5%**

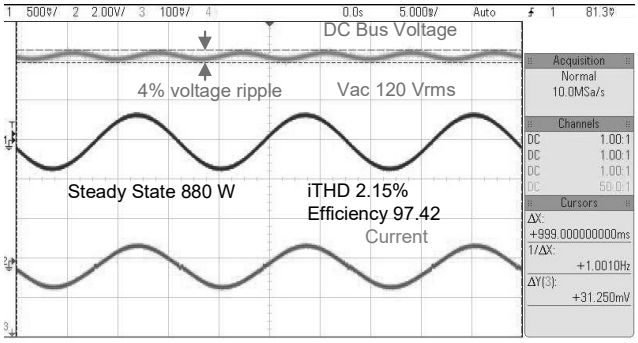


**Figure 61. Steady State 120-Vac IN, 380-V DC OUT 880W, iTHD 2.15%**

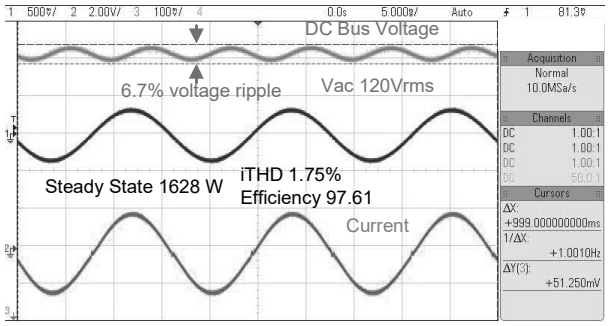


**Figure 62. Steady State 120-Vac IN, 380-V DC OUT, 1.674-KW, iTHD 1.75%**

Table 4 lists the detailed test results of this design under varying load conditions with 120-Vac input and 380-V DC output. For this data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard-switched edge, and the soft switching edge dead time varies between 20 ns and 200 ns.

**Table 4. Detailed Test Results with 120-Vac IN, 380-V DC OUT, and Different Power Levels**

| Vin (V RMS) | Vout (V) | Pin (W) | Iout (A) | Pout (W) | EFFICIENCY % | iTHD% | PF | % RATED LOAD | THETA OFFSET | GI KP |
|---|---|---|---|---|---|---|---|---|---|---|
| 120.05 | 382.02 | 154.27 | 0.375 | 143.47 | 92.98 | 10.54 | 0.9927 | 9.0 | -0.014 | 0.35 |
| 119.86 | 382.01 | 301.30 | 0.750 | 286.36 | 95.14 | 5.50 | 0.9974 | 17.9 | -0.01 | 0.35 |
| 119.49 | 382.01 | 444.40 | 1.120 | 427.76 | 96.30 | 4.16 | 0.9987 | 26.7 | -0.01 | 0.35 |
| 119.42 | 382.03 | 579.10 | 1.469 | 561.40 | 96.94 | 2.89 | 0.9950 | 35.1 | -0.01 | 0.35 |
| 119.16 | 382.02 | 721.30 | 1.837 | 701.80 | 97.30 | 2.42 | 0.9995 | 43.9 | -0.01 | 0.35 |
| 119.02 | 382.05 | 863.00 | 2.202 | 841.50 | 97.52 | 2.15 | 0.9995 | 52.6 | 0 | 0.35 |
| 118.78 | 381.96 | 1007.20 | 2.573 | 983.30 | 97.64 | 1.92 | 0.9995 | 61.5 | 0 | 0.35 |
| 118.63 | 382.08 | 1152.00 | 2.944 | 1125.30 | 97.69 | 1.82 | 0.9995 | 70.3 | 0 | 0.35 |
| 118.40 | 382.08 | 1298.40 | 3.319 | 1268.20 | 97.70 | 1.72 | 0.9994 | 79.3 | 0 | 0.35 |
| 118.25 | 382.08 | 1442.00 | 3.685 | 1408.30 | 97.69 | 1.87 | 0.9991 | 88.0 | 0 | 0.3 |
| 118.03 | 382.08 | 1593.80 | 4.071 | 1555.50 | 97.65 | 1.80 | 0.9991 | 97.2 | 0 | 0.3 |
| 117.98 | 382.05 | 1716.40 | 4.449 | 1674.80 | 97.61 | 1.75 | 0.9991 | 104.7 | 0 | 0.3 |

#### 3.2.1.3 Transient Test With Step Load Change

##### 3.2.1.3.1 0% to 50% Load Step Change

Figure 63 shows the transient response when input is 120 Vrms and a load step of 50% is applied to the power stage

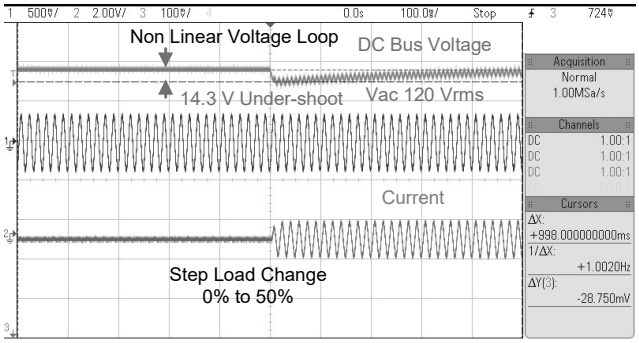


**Figure 63. Transient Response, 120 Vrms, 60 Hz, 0% to 50% Load Step**

##### 3.2.1.3.2 50% to 100% Load Step Change

Figure 64 shows the transient response when input is 120 Vrms and load is stepped up from 50% to 100%

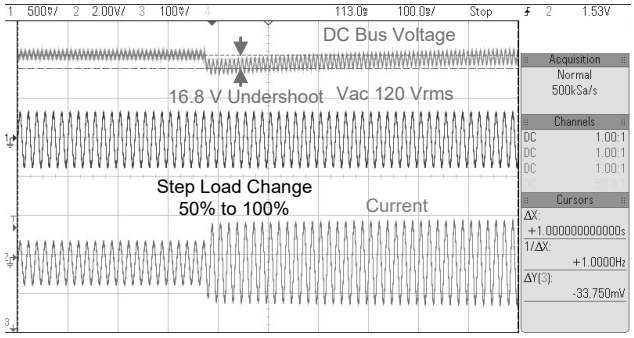


**Figure 64. Transient Response, 120 Vrms, 60 Hz, 50% to 100% Load Step**

##### 3.2.1.3.3 100% to 50% Load Step Change

Figure 65 shows the transient response when the input is 120 Vrms and load is stepped down from 100% to 50%.

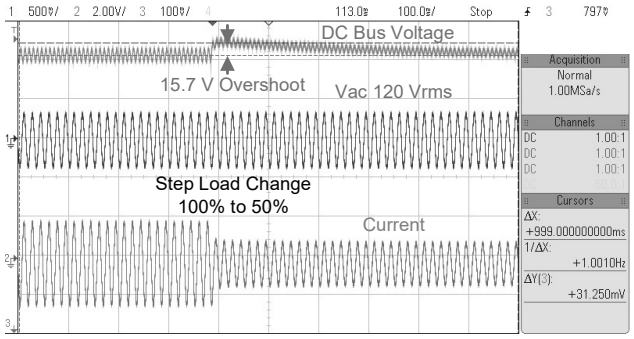


**Figure 65. Transient Response, 120 Vrms, 60 Hz, 100% to 50% Load Step**

#### 3.2.1.3.4 50% to 100% Load Step Change

Figure 66 shows the transient response when input is 120Vrms and load is stepped down from 50% to 0%.

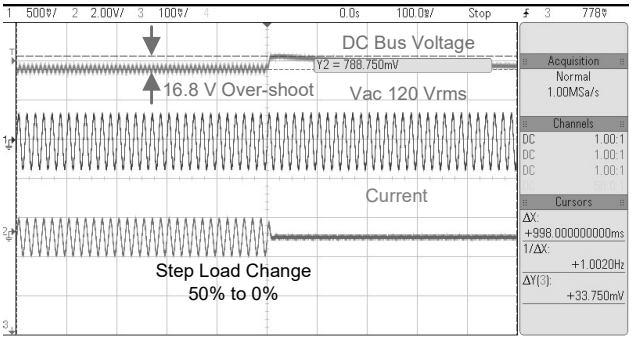


**Figure 66. Transient Response, 120 Vrms, 60 Hz, 50% to 0% Load Step**

### 3.2.2 Test Results at Input 230 Vrms, 50 Hz, Output 380 V DC

#### 3.2.2.1 Startup

Figure 67 shows the startup sequence of the power stage with input single phase 230-Vrms VL-N and output bus regulated at 380V and a 880-W load.

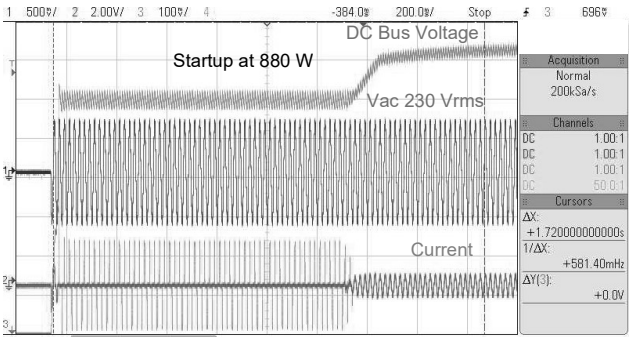


**Figure 67. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at 880-W Load**

Figure 68 shows the startup of PFC at no load at 230 Vrms.

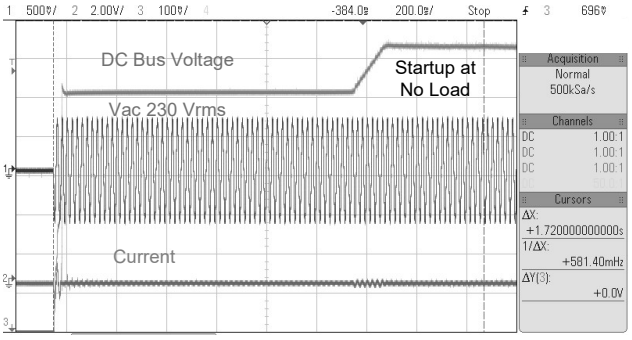


**Figure 68. Startup of PFC Operation at 230-Vac IN, 380-V DC OUT at no Load**

#### 3.2.2.2 Steady State Condition

Figure 69, Figure 70, and Figure 71 show the steady state current waveform at different load conditions. Phase shedding is disabled for these readings.

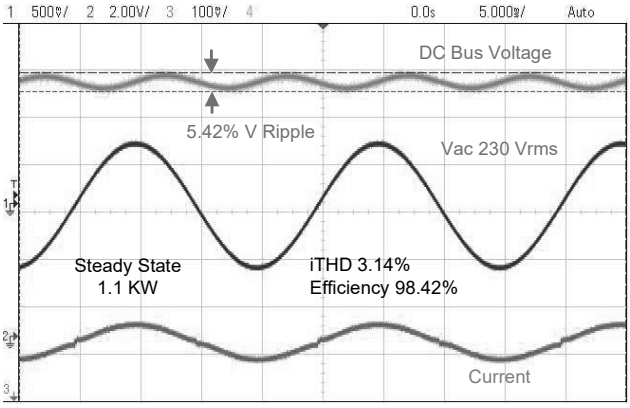


**Figure 69. Steady State 230-Vac IN, 380-V DC OUT, 1.1KW, iTHD 3.14%**

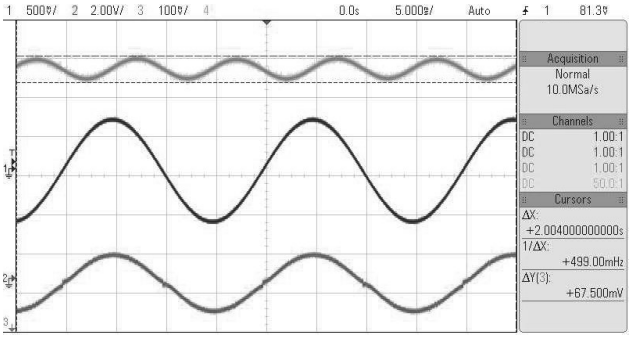

**Figure 70. Steady State 230-Vac IN, 380-V DC OUT, 2.2KW, iTHD 2.62%**

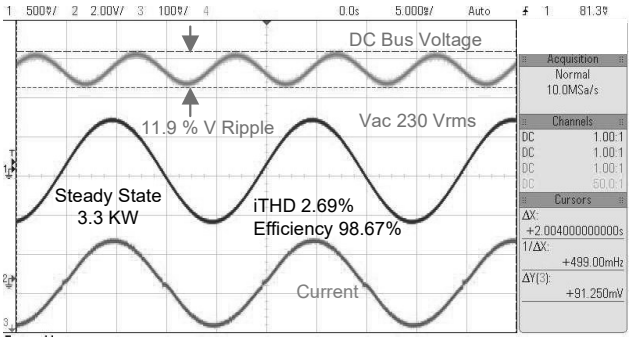


**Figure 71. Steady State 230-Vac IN, 380-V DC OUT, 3.3KW, iTHD 2.69%**

Table 5 lists the detailed test results of this design under varying load conditions with 230-Vac input and 380-V DC output. For the following data, phase shedding is disabled, adaptive dead time is enabled, 100 ns is chosen as the fixed dead time for the hard switched edge, and the soft-switching edge dead time varies between 20 ns to 200 ns.

**Table 5. Detailed Test Results With 230-Vac IN, 380-V DC OUT and Different Power Levels**

| Vin (V RMS) | Vout (V) | Pin (W) | Iout (A) | Pout (W) | EFFICIENCY % | iTHD% | PF | % RATED LOAD | THETA OFFSET | Gi Kp |
|---|---|---|---|---|---|---|---|---|---|---|
| 230.68 | 381.98 | 151.28 | 0.372 | 142.16 | 94.03 | 18.20 | 0.9775 | 4.4 | -0.025 | 0.35 |
| 230.43 | 382.00 | 292.24 | 0.736 | 281.41 | 96.29 | 9.15 | 0.9936 | 8.8 | -0.02 | 0.35 |
| 230.25 | 382.03 | 435.90 | 1.109 | 423.62 | 97.18 | 6.12 | 0.9938 | 13.2 | -0.01 | 0.35 |
| 230.06 | 382.06 | 576.40 | 1.473 | 562.86 | 97.66 | 4.85 | 0.9972 | 17.6 | -0.01 | 0.35 |
| 229.80 | 382.05 | 856.80 | 2.201 | 841.00 | 98.15 | 4.16 | 0.9974 | 26.3 | 0 | 0.35 |
| 229.70 | 382.11 | 1140.10 | 2.935 | 1121.90 | 98.42 | 3.14 | 0.9989 | 35.1 | 0 | 0.35 |
| 229.52 | 382.08 | 1418.80 | 3.659 | 1398.40 | 98.57 | 2.42 | 0.9993 | 43.7 | 0 | 0.3 |
| 229.28 | 382.08 | 1699.20 | 4.386 | 1676.40 | 98.66 | 2.74 | 0.9995 | 52.4 | 0 | 0.3 |
| 229.06 | 382.09 | 1977.70 | 5.106 | 1951.90 | 98.71 | 2.56 | 0.9996 | 61.0 | 0 | 0.3 |
| 229.09 | 382.11 | 2261.50 | 5.840 | 2232.40 | 98.73 | 2.62 | 0.9995 | 69.8 | 0 | 0.25 |
| 228.91 | 382.11 | 2548.30 | 6.580 | 2515.60 | 98.73 | 2.50 | 0.9994 | 78.6 | 0 | 0.25 |
| 228.86 | 382.14 | 2840.60 | 7.332 | 2803.20 | 98.71 | 2.89 | 0.9990 | 87.6 | 0 | 0.2 |
| 228.51 | 382.12 | 3132.80 | 8.083 | 3091.10 | 98.69 | 2.80 | 0.9989 | 96.6 | 0 | 0.2 |
| 228.22 | 382.03 | 3439.10 | 8.873 | 3392.30 | 98.65 | 2.69 | 0.9988 | 106.0 | 0 | 0.2 |

#### 3.2.2.3 Transient Test With Step Load Change

Following sections show the transient test results with step load change.

##### 3.2.2.3.1 33% to 100% Load Step Change

Figure 72 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

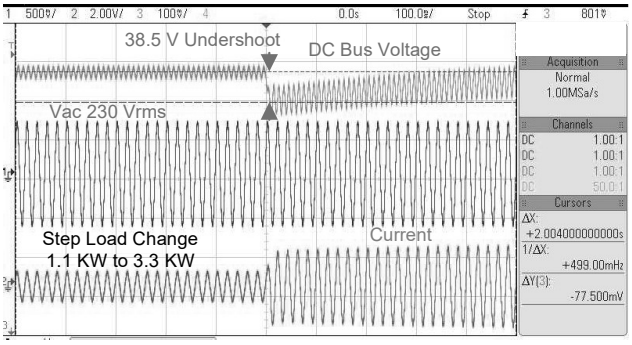


**Figure 72. Transient Response, 230 Vrms 50 Hz, 33% to 100% Load Step**

#### 3.2.2.3.2 100% to 33% Load Step Change

Figure 73 shows the transient response when input is 230 Vrms and load is stepped down from 100% to 33%.

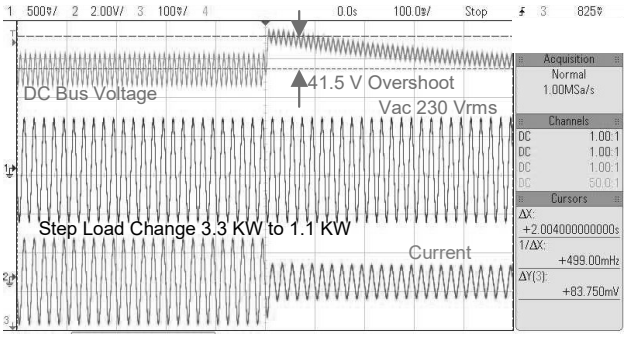


**Figure 73. Transient Response, 230 Vrms 50 Hz, 100% to 33% Load Step**

### 3.2.3 Test Results Graphs

Figure 74 shows the efficiency data plotted under different test conditions for this design.

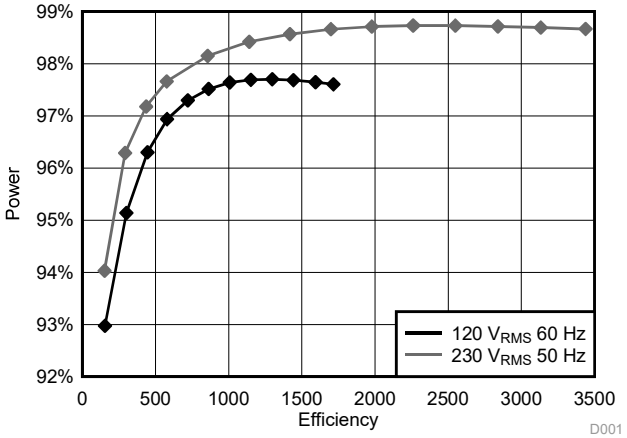


**Figure 74. Efficiency at 230-Vrms Input and 120-Vrms Input**

Figure 75 shows the THD data plotted under these test conditions.

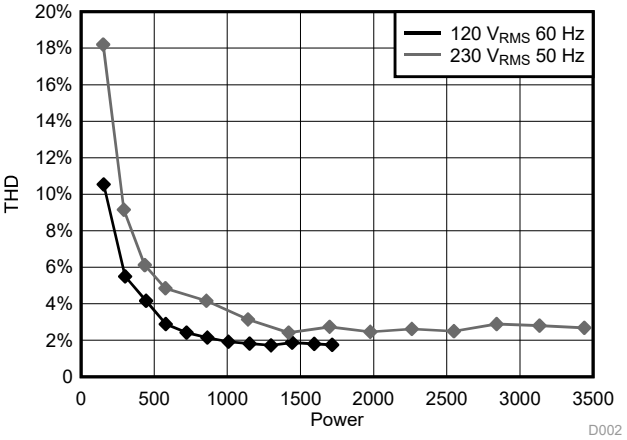


**Figure 75. THD at 230-Vrms Input and 120-Vrms Input**

Figure 76 shows the PF data plotted under these test conditions.

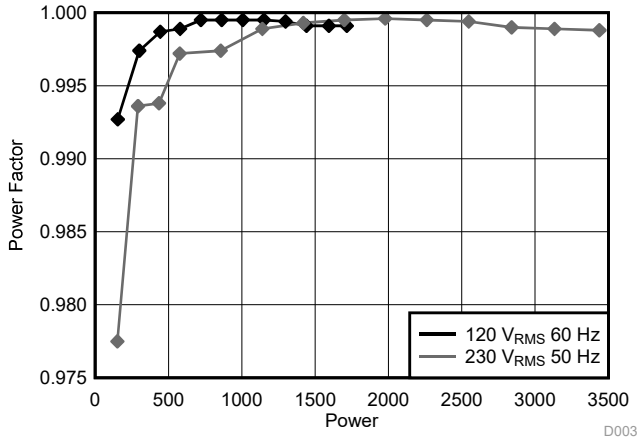


**Figure 76. PF at 230 Vrms and 120Vrms With Varying Load**

# 4 Design Files

## 4.1 Schematics

To download the schematics, see the design files at TIDM-1007 .

## 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-1007 .

## 4.3 PCB Layout Recommendations

### 4.3.1 Layout Prints

To download the layer plots, see the design files at TIDM-1007 .

## 4.4 Altium Project

To download the Altium project files, see the design files at TIDM-1007 .

## 4.5 Gerber Files

To download the Gerber files, see the design files at TIDM-1007 .

## 4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-1007 .

# 5 Software Files

To download the software files, see the design files at TIDM-1007 .

# 6 Related Documentation


1. Texas Instruments, *How to reduced current spike at AC zero crossing for totem-pole PFC Technical Brief*
2. Z. Ye, A. Aguilar, Y. Bolurian and B. Daugherty, *GaN FET-Based High CCM Totem-Pole Bridgeless PFC*, Texas Instruments Power Supply Design Seminar, 2014-15.
3. L. Xue, Z. Shen, D. Boroyevich and P. Mattavelli, *GaN-based High Frequency Totem-Pole Bridgeless PFC Design with Digital Implementation*, IEEE 2015 Applied Power Electronics Conference, 2015, pp. 759-766.
4. H.-S. Youn, J.-B. Lee, J.-I. Black and G.-W. Moon, *A Digital Phase Leading Filter Current Compensation (PLFCC) Technique for CCM Boost PFC Converter to Improve PF in High Ligne Voltage and Light Load Condition*, IEEE Transactions on Power Eelectronics , vol. 31, no. 9, pp. 6596-6606, 2016.
5. D. M. V. d. Sype, K. D. Gusseme, A. P. M. V. d. Bossche and J. A. Melkebeek, *Duty-Ratio Feeforward for Digitally Controlled Boost PFC Converters*, IEEE Transactions on Industrial Electronics, vol. 52, no. 1, pp. 108-115, February 2005.
6. "Rodriguez, P.,Luna, A., Candela, I., Teodorescu, R., and Blaabjerg, F. *Grid Synchronization of Power Converters Using Multiple Second Order Generalized Integrators* , In Proceedings of IEEE industrial Electronics Conference (IECON'08), November 2008, pp 755-760"
7. Texas Instruments, *Software PLL Design Using C2000 MCUs Single Phase Grid Connected Inverter Application Report*
8. Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers Data Manual*
9. Texas Instruments, *LMG3410 600-V 12-A Single Channel GaN Power Stage Data Sheet*

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## 7 About the Author

**MANISH BHARDWAJ** is a Systems Application Engineer with C2000 Microcontrollers System Solutions Group at Texas Instruments, where he is responsible for developing reference design solutions for digital power, motor control, and solar power applications. Before joining TI in 2009, Manish received his Masters of Science in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta in 2008 and his Bachelor of Engineering from Netaji Subhash Institute of Technology, University of Delhi, India in 2007.

## Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from A Revision (March 2018) to B Revision | Page |
|---|---|
| • Added items to Features | 1 |
| • Added F28004x to Section 2.3.1 and updated text | 6 |
| • Changed power supply connection to TP604 from TP612 in Table 3 | 12 |
| • Changed power supply connection to TP606/TP609 from TP609 in Table 3 | 12 |
| • Added Section 3.1.2.3 | 18 |
| • Added Section 3.1.2.5 | 38 |

# Revision A History

**Changes from Original (November 2017) to A Revision** **Page**

- Changed Figure 9: *Current Loop Control Model* ..... 7
- Changed Figure 11: *DC Voltage Loop Control Model* ..... 9
- Changed power supply connection from TP612 to TP604 in Section 3.1.1.1: *Base Board Settings* ..... 11
- Changed Figure 36: *Build Level 3 Control Diagram: Output Voltage Control With Inner Current Loop* ..... 33
- Changed Figure 38: *Build Level 3: Expressions View* ..... 35
- Changed Figure 39: *Build Level 3: Expressions View After AC Voltage is Applied* ..... 36

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