

GN25L98 GPON 2Layer BOB – Board 23

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Revision History

Revision 1
Initial revision 09/24/2015



Introduction

- This report provides test results from measurements conducted on a GN25L98 based GPON DDMI 2 Layer BOSA on Board (BOB) design that will be sampled to customers.
 - ➢ Board 23
 - BOSA EZConn: 1.25G 1310nm DFB/ 2.5G 1490nm APD-TIA(Lab44APD+GN25L53)
 - > Part number: EBS63432-B1203
 - ➢ BOSA S/N EEU082448
 - Each module is supplied as part of a kit that encompasses the 2 Layer BOB, Graphical User Interface, Test cables, etc.
- This sample utilises GN25L98 B00 silicon.
- The version of Graphical User Interface is GN25L98_GPON_DDMI_ GUI_V0_R1_B3.
- Config File:A2_Table_2_Template_rev02_BOB_141216



2 Layer BOB Design

- The 2 Layer BOB design provides demonstration of the Transmitter & Receiver performance with APD based GPON BOSA. The EVB is configured with APC & ERC loops enabled and associated seeding for fast start operation provided by pre-configured Bias and Modulation Look Up Tables.
- Look up table support for both the Transmitter and Receiver parameters are demonstrated.
 - Transmitter Bias and ERC seeding LUT enabled, TRIM_ER LUT enabled
 - Receiver APD Bias control LUT enabled

Note: We determine the bias, ERC,TRIM_ER_LUT seeding value at room temperature and extract slope data from the last few samples to determine other temperature points for loading LUT's.

- APD Circuit Quick Trip is enabled
- Full DDMI reporting is provided.



GN25L98 2 Layer BOB





Board Schematic – Tx & Rx signal paths





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Board Schematic – APD Bias Gen & Interface

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Board Schematic – Digital





BOM File

Comment	Description	Designator	Footprint	LibRef	Quantity			R5, R6, R17, R20, R22,			
EZconn GPON BOSA		BOSAL	BOSA_DDMI_ZTE	BOSA_ZTE	1	OR	Resistor	R58, R59	04028	RES1	11
				Cap Semi, Cap Semi,		470R	Resistor	R9, R12	06038	RES1	2
		C1. C6. C7. C8. C9. C10.		Cap Semi, Cap Semi, CAP1, CAP1, CAP1		1K	Resistor	R13, R14	06038	RES1	2
100nF	Capacitor	C12, C13, C16, C17	06038	CAP1, CAP1, CAP1	10	470R	Resistor	R15, R18, R21	04028	RES1	3
	Polarised Capacitor,	0.00	00000	CAPACITOR POL 1206,		10K	Resistor	R16	04028	RES1	1
107	Capacitor, Capacitor	C2, C5, C21	06038	Cap Sem, CAP1	3	4K7	Resistor	R19, R38	04028	RESI	2
		C32, C36, C37, C39,				3.9K	Resistor	R23, R24, R25, R33	04028	RESI	4
100-5	Consider	C40, C41, C42, C44,	0.4038	C491		39K	Resistor	R26	04028	RESI	1
1000	Capacitor Relationd Capacitor	C45, C46, C47	12064	CAPACITOR POL 1006	40	NC(300K)	Resistor	R28	04028	RESI	1
100r	Polarised Capacitor	C11, C10	12068	CAPACITOR FOL 1205		NC(17M)	Resistor	829	04028	RESI	1
4.7pr/1004	Capacitor	C19	00054	CAPI		200K	Resistor	830	04028	RESI	1
1005	Capacitor	C20	UBUSa	CAPI	1	1008	Resistor	R31 R34 R36 R49	04028	REST	
0.106/1009	Capacitor	C23	USUSA	CAPI	1	2208	Resistor	820	04028	DEC1	
10nF	Capacitor	C25, C27, C33, C35	04028	CAP1	4	150	Resistor	P37 P30 P43	04028	DCC1	
10nF/100V	Capacitor Capacitor Resistor	C30	04028	CAP1	1	108	Resistor	R37, R33, R42	04028	REST	
	Resistor, Resistor,			CAP1, RES1, RES1,		108	Resistor	840	04028	RESI	
	Resistor, Resistor,	C34, R2, R3, R35, R43,		RES1, RES1, RES1, RES1,		300	Resistor	841	04028	RESI	-
NC	Resistor, Resistor	R44, R50, R51	04028	RES1	8	1K	Resistor	845	04028	RESI	1
12pF	Capacitor	C43	04028	CAP1	1	220R	Resistor	R46	04028	RESI	1
DiodePack	SP0503BAHT	D1	SOT143	DiodePack	1	33R	Resistor	R47	04028	RES1	1
BAT46WJ		D2	SOD323F	BAT46WJ	1	NC(1K)	Resistor	R53, R54	06038	RES1	2
1N4148WX		D3	SOD-323	1N4148WX	1	100K	Resistor	R56, R57	04028	RES1	2
HEAD2x5	Header, 5-Pin, Dual row	HD1	HDR2X5	Header 5X2	1	SMA	SMA connector	SK1, SK2, SK3, SK4, SK5, SK6, SK7	SMAEDGE2	SMA2, SMA2, SMA2, SMA2, SMA2, SMA, SMA	7
HEADER2	Header, 2-Pin	HD2, HD3, HD4, HD5, HD8, HD9, HD10	HEAD2	HEADER2	7		Schurter LPH				
	[NoValue], Header, 3-					PUSH SW	(1301.9302)	SW1	LPH	Button Switch	1
HEADER 3	Pin	HD6, HD7	HEAD3	HEADER3, HEADER 3	2	MMS22		SW2	MMS22	MMS22	1
AT24C08C		K1	SOIC8	AT24C08C	1	SW-SPDT	SPDT Subminiature Tog	cSW3, SW4	HEAD3	SW-SPDT	2
NC	Silicon Labs	IC2	Quad20	DDMI 330	1	L					
F342 LQFP-32		IC3	LCC32	F340 LQFP-32	1	l.					
MCP9700		IC5	SC70-5	MCP9700	1						
GN25L98		106	QFN28	GN25L98	1						
US8 Thru TypeB		л	USB	USB Thru TypeB	1						
Socket	Socket	J2, J3, J4, J5, J6	2MMPCB	Socket	5						
BLM18AG221SN1	Inductor	L1, L2, L3, L5, L7	06038	Inductor	5	i i i i i i i i i i i i i i i i i i i					
BLM15AG121SN1	Inductor	14	0402b	Inductor	1						
SRN3010-150M		L6	SRN3010	SRN3010-150M	1	R41/C	43 altered	d to 63R/′	12pF		
3.3NH	Inductor	L8, L9	04028	Inductor	2						
BLM15HG601	Inductor	L10, L11	04028	Inductor	2	2					
P1.0	Red LED	LED1	1206A	LED	1						
P1.1	Red LED	LED2	1206A	LED	1						
LED1	Typical RED GaAs LED	LED3	LEDSM	LED1	1						
TBD	Typical RED GaAs LED	LED4, LED5	LEDSM	LED1	2						
BSS138	N-Channel MOSFET	01, 02, 03	SOT23	MOSFET-N	3						
BC8565 (65V)		04.05	SOT363	BC8565	2	2					
NC(855123)	N-Channel MOSEET	06	SOT23	MOSEET-N	1						
B55123	N-Channel MOSFFT	07.08	SOT23	MOSFET-N	2						
08	Resistor	R1. 87. R10. R11	06038	RESI							
NC	Resistor	R4. R8	06038	RES1	2	8				5	
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Transmitter Test Results



Transmitter Test List & Deliverables

Parameter	Temperature, C					Deliverable
	-10	0	25	70	85	
1/ Average Power	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	Plot Pavg Vs Temp
2/ ER Control	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	Plot ER Vs Temp
3/ Eye margin	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	Eye Diagrams & Mask margin using GbE mask
4/ Burst Timings			\checkmark		\checkmark	Capture Burst timing shots

Note: This evaluation board can work fine in all temperature ranges from - 40C to 85C, to save the test time, just test from -10C to 85C.



1. Transmitter Mean Power Control



Transmitter Mean Power Control

Mean Power Variation - Temp -10C to 85C



• 0.48dB variation over -10C to +85C temperature range



2. Transmitter ER Control



Transmitter Extinction Ratio

ER Variation - Temp -10C to 85C Auto ER enabled.



- 0.31dB variation over -10C to +85C temperature range
- TRIM_ER LUT enabled! (optional feature)



3. Transmitter Mask Margin



Transmitter Mask Margin -10C to 85C

GENNUM PRODUCTS

Mask Margin Temp -10C to 85C



Transmitter Mask Margin



Mask margin 0C





Mask margin -10C 68%

Transmitter Mask Margin



Mask margin 25C 68%

Mask margin 85C 69%



4. Transmitter Burst Timings



Transmitter Burst Timing Requirements

- Tx Burst "ON" time
 - ➤ target 12.8ns maximum
- Tx Burst "Off" time
 - ≻ Target 12.8ns maximum
- Fast Start up settling time
 - within 3 "on" bursts total time 1.92us
- Tx SD output delay time
 - Target < 200ns maximum</p>
- Tx SD width variation
 - Target < 100ns width difference wrt BEN input</p>



Transmitter Burst Timing



 Testing of Burst Mode Timing Delays is measured with 32 bit pre-amble pattern (1-0-1-0 repeated) combined with PRBS data. Timings are measured by determining how many bits are missing from pre-amble (Burst ON) or present (Burst OFF) Settling criteria within 10 to 90% of settled power levels.

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• Please be noticed that the following timing test data base on the previous EVB.



Transmitter - Burst ON performance ,Temp 25C



Burst ON delay 3.53ns Markers indicate relevant timings



Transmitter - Burst OFF performance ,Temp 25C

Spec 12.8ns max



Burst OFF delay 2.88ns

Markers indicate relevant timings



Transmitter - Fast Start Initialization, Temp 25C



Measure Fast Start Initialization – time from start of 3 bursts to time when Optical output has settled within 10% of steady state power level. Fast start using MOD LUT for seeding.

Transmitter - Fast Start Initialization, Temp 85C



Measure Fast Start Initialization – time from start of 3 bursts to time when Optical output has settled within 10% of steady state power level. Fast start using MOD LUT for seeding.

Transmitter - TXSD delay, Temp 25C



Transmitter – TXSD width variation, Temp 25C



TXSD width 338.88ns, BEN input width 320ns, 18.88ns variation.



Receiver Test Results



Receiver Test List & Deliverables

Parameter	Т	empera	ture, C		Deliverable
	-10	25	70	85	
5/ APD Control		\checkmark			Plot APD Bias & EZConn BOSA requirement
6/ Receiver Sensitivity	\checkmark	\checkmark		\checkmark	BER curve. Determine Sensitivity for BER 1e-10.
7/ Crosstalk Penalty	\checkmark	\checkmark		\checkmark	BER Curve with Burst Tx data present. Determine Crosstalk penalty.
8/ LOS Characteristics	\checkmark	\checkmark		\checkmark	Measure Assert/De-Assert & determine Hysteresis
9/ Rx Eye Quality		\checkmark		\checkmark	Capture Eyes at -30dBm, -20dBm & -10dBm



5. APD Bias Control



APD Bias Control – LUT



• Determine the bias seeding value at room temperature and extract slope data from the last few samples to determine other temperature points for loading LUT's.



6. & 7. Receiver Sensitivity & Crosstalk Penalty



Sensitivity – Tx Disabled

Responsivity=0.903A/W





Sensitivity – Crosstalk Penalty, Temp 25C & 85C



8. Signal Detect Characteristics



Signal Detect thresholds – 2dB hysteresis setting





9. Rx Eye Quality



Rx Eye – Single Ended @-30dBm



25C

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Rx Eye – Single Ended @-20dBm



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Rx Eye – Single Ended @-10dBm



25C



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10. Power Consumption



Module Power Consumption, APD controller enabled

Module power consumption- Temp -10C to 85C APC/ERC enabled (CW data)



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• Tx enabled CW data, APD Controller enabled (Popt -30dBm).



Supply Current, mA

11. DDMI Reporting Internal Calibration



DDMI Monitor Accuracy – Internal Cal

Temperature	Temp	Readback TEMP,C	Error, C
remperature	-40	-40.86	-0.86
	-10	-10.73	-0.73
	0	0.91	0.91
	25	24.12	-0.88
	70	69.03	-0.97
	85	83.98	-1.02
Tx Power	TX PowerMeasured, dBm	Readback TX Power dBm	Error,dBm
	3.67	3. 58	-0.09
	2.03	1.99	-0.04
	0.03	0.12	0.09
	-2.06	-1.85	0.21
	-2.99	-2.69	0.3
Vdd	Vdd	Readback Vdd	Error, %
	3	2.9	5 1.3
	3.3	3. 28	8 0.6
	3.6	3. 53	3 1.9

- Temperature calibration has to be performed with Tx and Rx powered up in normal operation mode.
 - Tx ON with Burst data
 - Rx APD controller enabled with Popt -30dBm

Bias Current accuracy difficult to define at module level, but accuracy guaranteed by product characterisation!



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DDMI Monitor Accuracy – Internal Cal

Rx power

	Rx Power Force ,dBm	Readback Rx power, dBm	Error dBm
	-35	-35.23	-0.23
GN25L98	-33	-33.01	-0.01
	-30	-30	0
	-20	-20.04	-0.04
	-15	-15.06	-0.06
	-12	-12.1	-0.1
	-8	-8,05	-0.05
	Rx Power Force ,dBm	Readback Rx power, dBm	Error dBm
	-35	-36.99	-1.99
	-33	-33.98	-0.98
	-30	-30.97	-0.97
	-27	-27.7	-0.7
GNZ5L95	-24	-24. 32	-0.32
	-20	-20.22	-0.22
	-15	-14.91	0.09
	-12	-11.61	0.39
	-9	-8.44	0.56
	-7	-6.24	0.76

Enhanced DDMI reporting capability provides higher margin to ٠ the specification for Rx Power reporting.



12. APD Controller OC/OV Fault



Over Voltage Fault and Auto Restart

The capture shows the restart activity in the presence of a "over voltage" event.



APD Bias ramp to the target value set by APD_DAC at 102us/step

• The OV Threshold is defined in the equation below (refer to slide 9 for R32 and R33):

$$\left(9.87mV + \left(1.261 * \left(\frac{APD_THRESHOLD[7:4]}{255}\right)\right) \right) * \left(\frac{R32 + R33}{R33}\right)$$

APD Controller shut down due to OV Fault triggered (Quick Trip NOT enabled) recovers the APD Controller

- The OV Fault is triggered by deliberately changing the APD_DAC value from 300dec to 100dec with Ramp Target Rate set to 1.6us and APD_OV_RAMP_DIS='0'.
- Restart Timer is set to 105ms.



APD Controller restarted

Over Current Fault and Auto Restart

The capture shows the restart activity in the presence of a "over voltage" event.



Quick Trip

The capture shows the APD output quick discharge capability of the Quick Trip functionality.



OV Fault Triggered, Quick Trip Disabled

OV Fault Triggered, Quick Trip Enabled

The quick trip signal is maintained for 20ms and is then removed



Summary

- The performance of a GN25L98 based GPON 2 Layer BOB design has been presented.
- Automatic Extinction Ratio Control has been demonstrated and will meet the requirement for BOB on applications.
 - Common requirement is ER=13dB over temperature range -40C to 85C.
 - ER variation is typical 0.31dB with TRIM_ER LUT enabled to compensate for ER variation over temperature.
- Transmitter meets Burst Settling time and Fast Start requirements with margin, utilising Bias and Mod LUT's for Fast Start seeding.
- Demonstrated the capability of the lower cost integrated APD controller and associated LUT.
- Receiver Sensitivity and crosstalk performance is competitive.
- Enhanced DDMI reporting capability provides higher margin to the specification for the parameters available, especially for Rx Power.
- GUI is available for download from Semtech FTP site. Contact Semtech Sales for details.





