

AS0140 80ICBGA DEMO3HEAD BOARD

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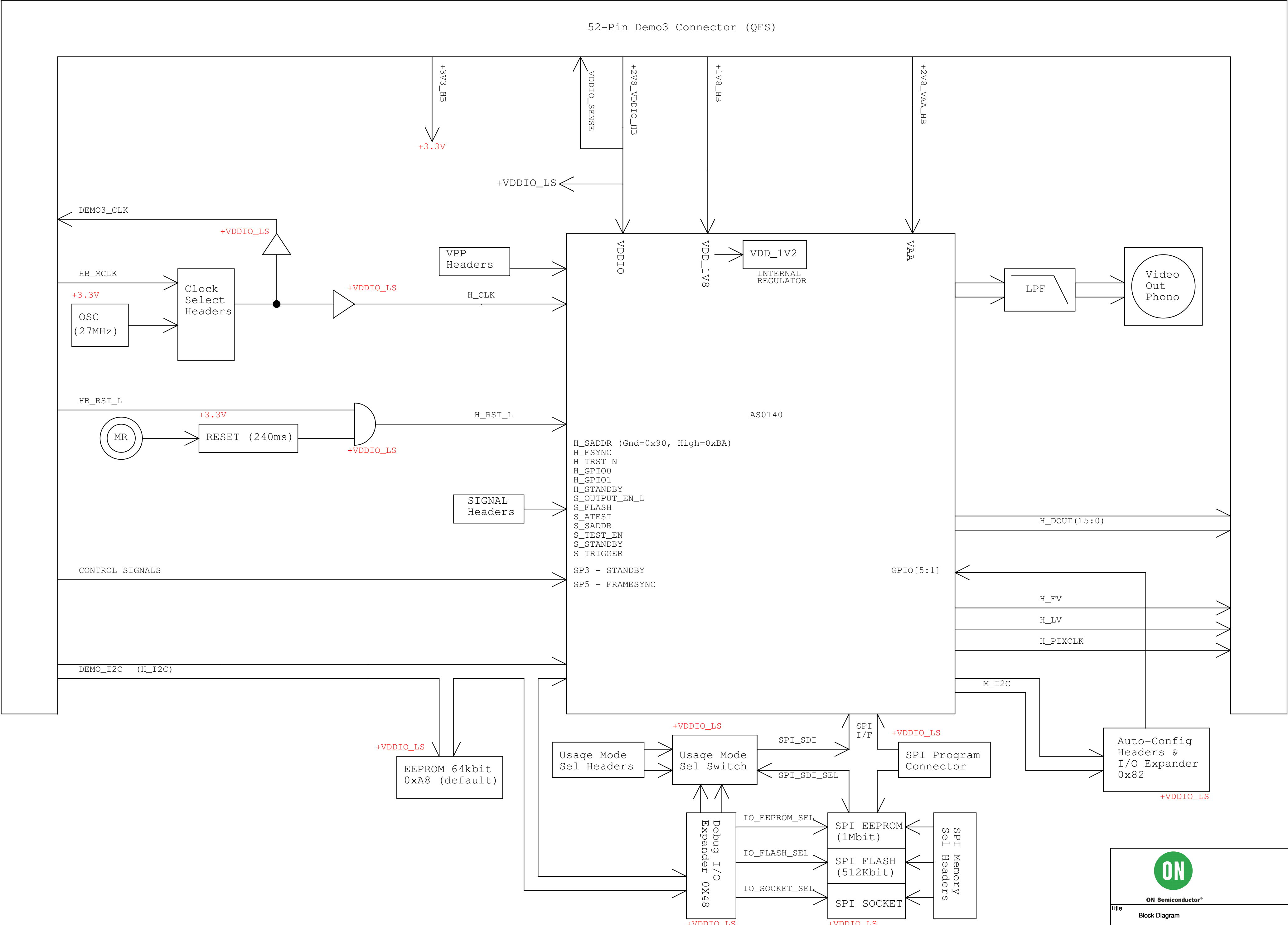
Rev	Who	Date	Description
Rev 0.0	jwrede	10/06/2014	Base Schematic for Custom Design
Rev 0.1	skumar	10/16/2015	- Initial Draft, Copied from "AS0140_130IEBGA_DEMO3HEAD" Replaced orcad symbol with 80ICBGA. Rest of the schematic is exactly similar as AS0140_130IEBGA_DEMO3HEAD
		10/19/2015	- Deleted Extra capacitor from the sensor supply Pin
		10/21/2015	- Removed S_DOUT0 through S_DOUT11,S_FV,S_LV, S_PIXCLK, S_EXTCLK and S_RST_N test points
Rev 1.0	skumar	05/25/2016	- Added Jumper control (P54) for H_STANDBY signal - Replaced PTS635SL25SMTRLFS (C&K Components) to 147873-2 (TE-Connectivity)



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Title		
AS0140_80ICBGA_DEMO3HEAD_Card		
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Block Diagram



PINOUT

	1	2	3	4	5	6	7	8	9	10	11	12
A	S_DOUT11	S_DOUT12	GPIO_5	SPI_SD0	SPI_CS_N	LDO_OP	ICP_SADDR	SPI_SDI	S_DOUT7	DOUT13	S_DOUT9	S_PIXCLK
B	S_DOUT10	S_DOUT8	SCLK	LINE_VALID	PIXCLK	SADDR	DGND	FRAME_SYNC	DGND	RESET_N	S_DOUT15	S_DOUT13
C	GPIO_2	DOUT12									S_DOUT6	SDATA
D	GPIO_3	DOUT6									VDDIO_2V8	DOUT8
E	DOUT11	DOUT0									VDDIO_2V8	DOUT3
F	STANDBY	GPIO_4									M_SCLK	DOUT15
G	DOUT14	GPIO_1									M_SDA	DGND
H	FRAME_VALID	DOUT10									S_TRIGGER	AGND
J	SPI_SCLK	DOUT9									S_DOUT5	AGND
K	S_DOUT4	DGND									OE_N	VAA_2V8
L	S_EXTCLK	S_STANDBY	DOUT5	TEST_EN	FLASH	DAC_NEG	DAC_POS	DOUT2	HCLK_IN	DOUT4	ICP_TRST_N	GPIO_0
M	S_DOUT14	S_LINE_VAILD	DAC_REF	VDD_1V8	VDD_1V8	VDDA_DAC	VDD_1V8	ATEST	DOUT7	DOUT1	S_RESET_N	S_FRAME_VALID

TOP SIDE VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	GPIO_5	SPI_SD0	SPI_CS_N	LDO_OP	ICP_SADDR	SPI_SDI	NC	DOUT13	NC	S_PIXCLK
B	NC	NC	SCLK	LINE_VALID	PIXCLK	SADDR	DGND	FRAME_SYNC	DGND	RESET_N	NC	NC
C	GPIO_2	DOUT12									NC	SDATA
D	GPIO_3	DOUT6									VDDIO_2V8	DOUT8
E	DOUT11	DOUT0									VDDIO_2V8	DOUT3
F	STANDBY	GPIO_4									M_SCLK	DOUT15
G	DOUT14	GPIO_1									M_SDA	DGND
H	FRAME_VALID	DOUT10									TRIGGER	AGND
J	SPI_SCLK	DOUT9									NC	AGND
K	NC	DGND									OE_N	VAA_2V8
L	NC	S_STANDBY	DOUT5	DGND	FLASH	DAC_NEG	DAC_POS	DOUT2	HCLK_IN	DOUT4	ICP_TRST_N	TRIGGER_OUT
M	NC	NC	DAC_REF	VDD_1V8	VDD_1V8	VDDA_DAC	VDD_1V8	NC	DOUT7	DOUT1	NC	NC

CUSTOMER PINOUT TOP SIDE VIEW



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Title

Pinout

Size C

Document Name

Rev

AS0140_80ICBGA_DEMO3HEAD_Card

1.0

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Tuesday, May 24, 2016

Sheet

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of

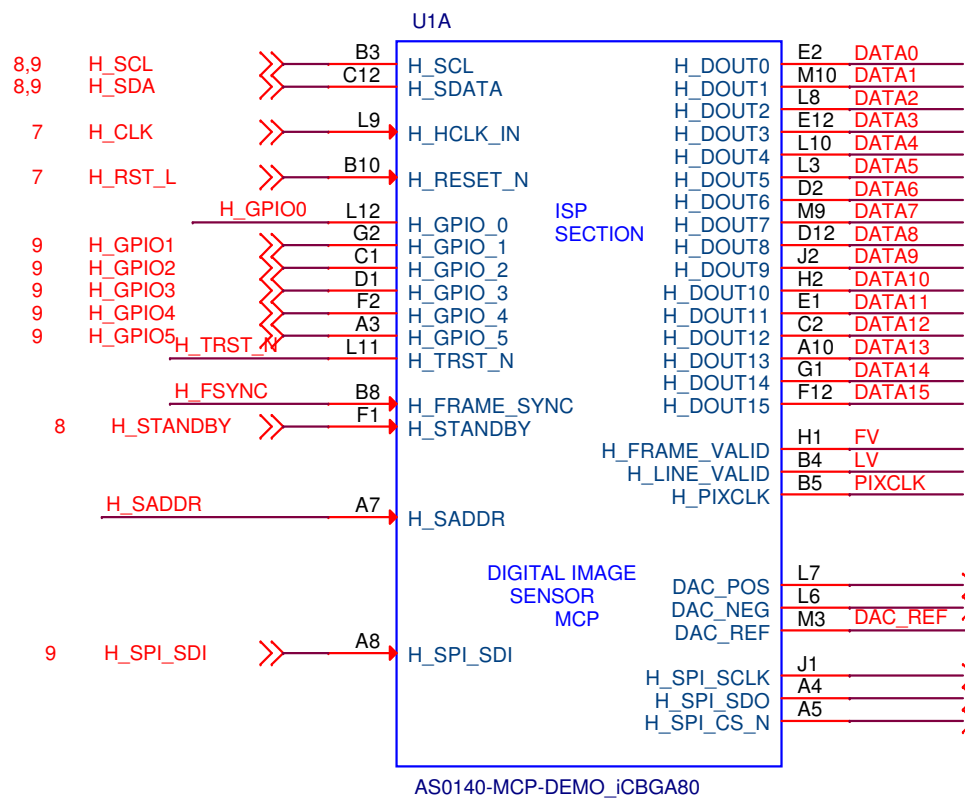
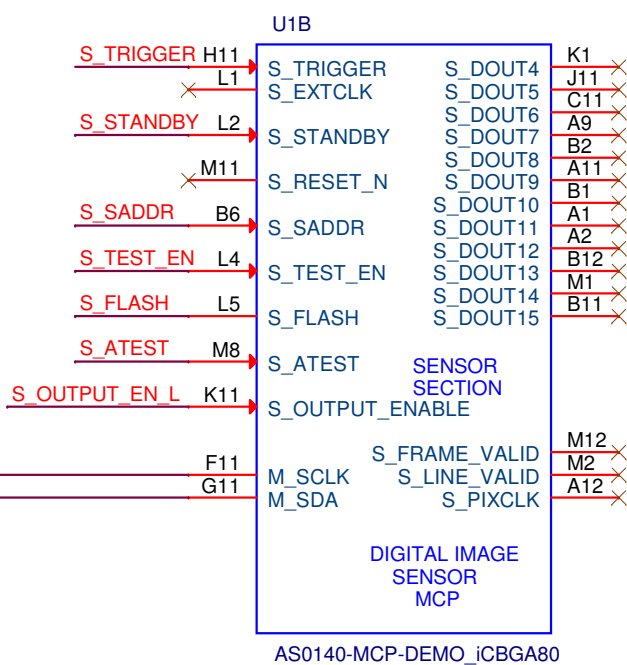
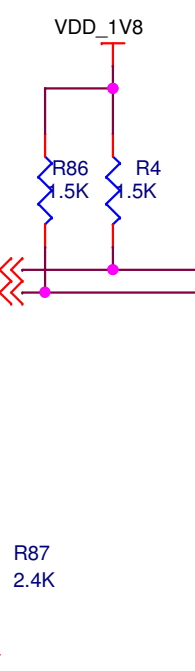
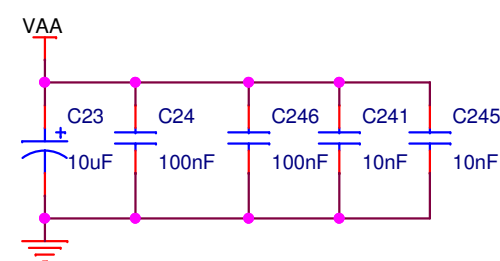
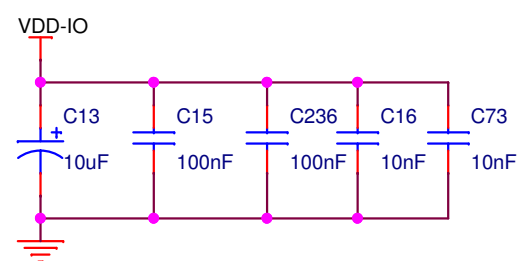
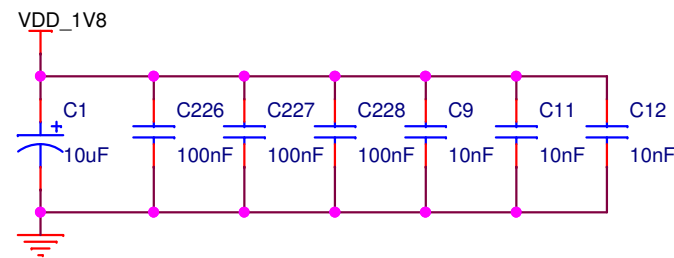
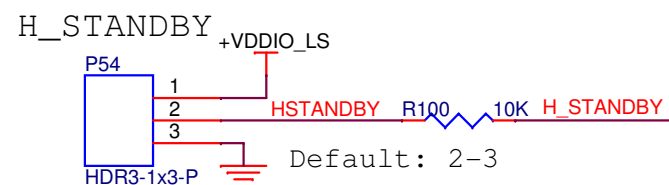
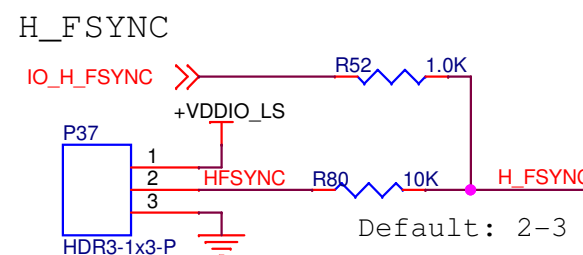
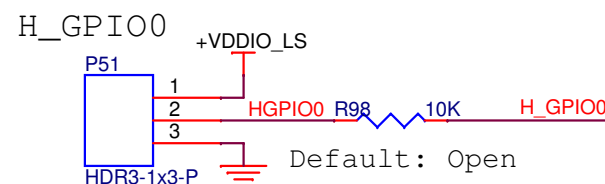
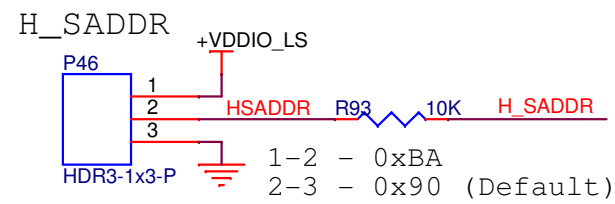
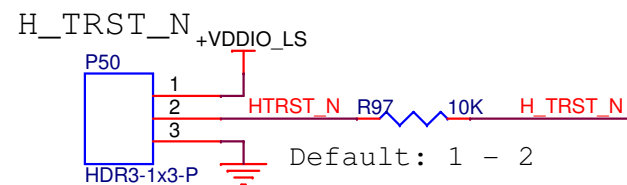
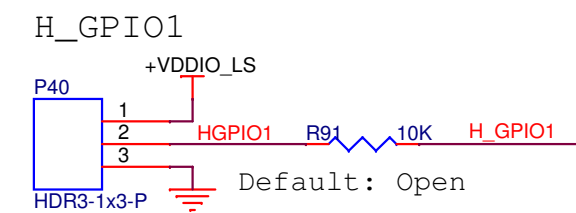
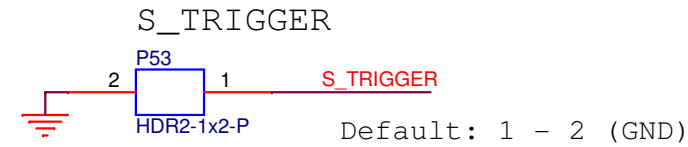
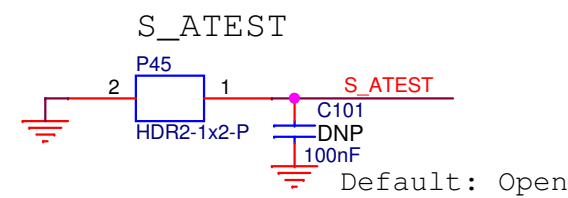
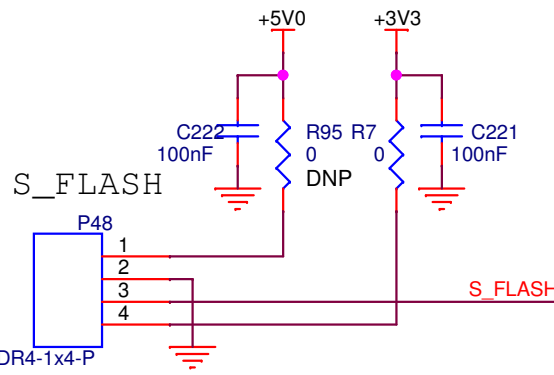
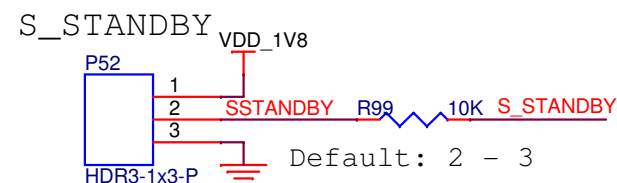
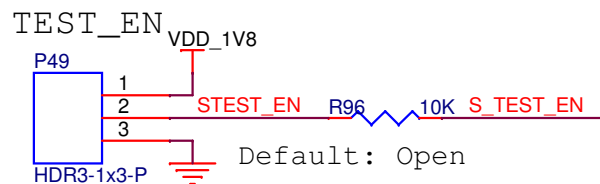
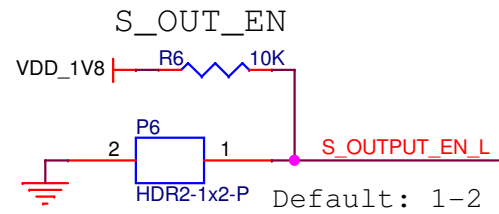
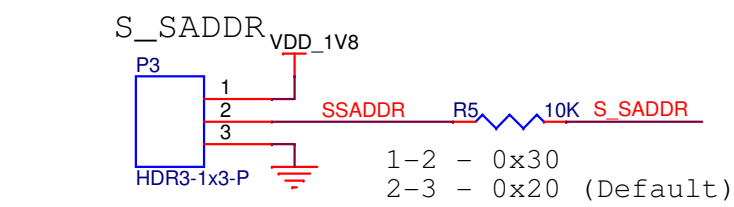
9

Supply Pin details

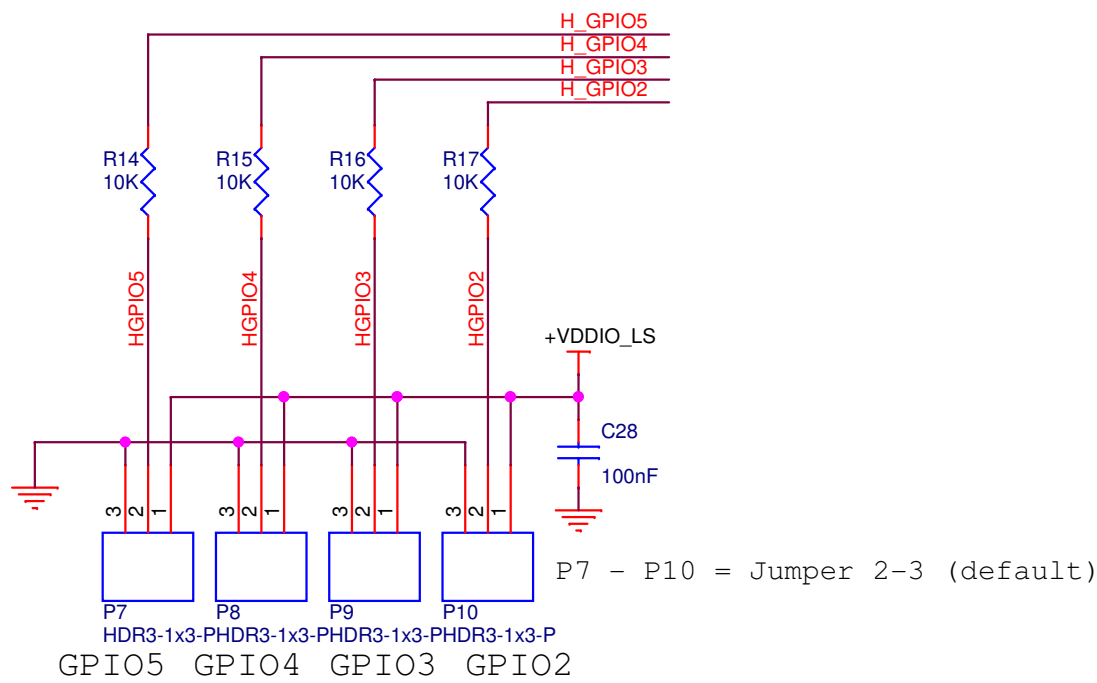
MCP Supply Pin	Voltage	Voltage included
LDO_OP	+1.2V	VDD_H VDDPLL_REF_H VDDPLL_POST_H VDDPLL_A_H FB_SENSE_H VDD_DAC_H LDO_OUTPUT_H
VDD_1V8	+1.8V	VDDIO_SENSOR_H ENLDO_H AVDD_H VDDCORE_S VDDIO_S VDD_PHY_S VDD_SLVS_S
VAA_2V8	+2.8V	VAA_S VAAPIX_S VDDPLL_S
VDDIO_2V8	+2.8V	VDDIO_H VDD_PHY_H VCC_H
VDDA_DAC	+3.3V	VDDA_DAC_H
DGND	0V	VSS_H GNDA_DAC_H EXT_REG_H GND_DAC DGND_S GND_SLVS_S
AGND	0V	AGND_H AGND_S

****_H =>Supply voltage Pin included from ISP AP0100
****_S =>Supply voltage Pin included from Sensor AR0140

Sensor

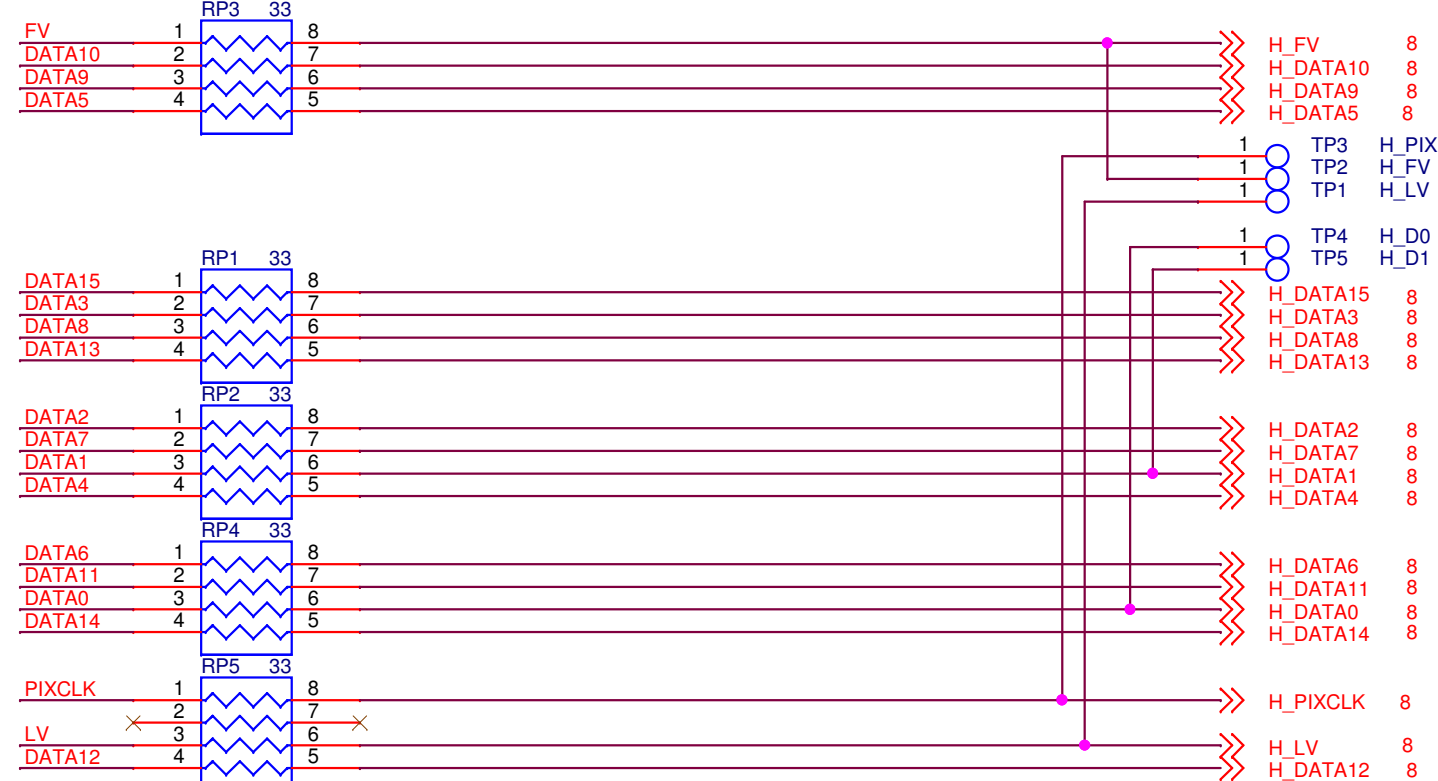


BOOT SELECTION

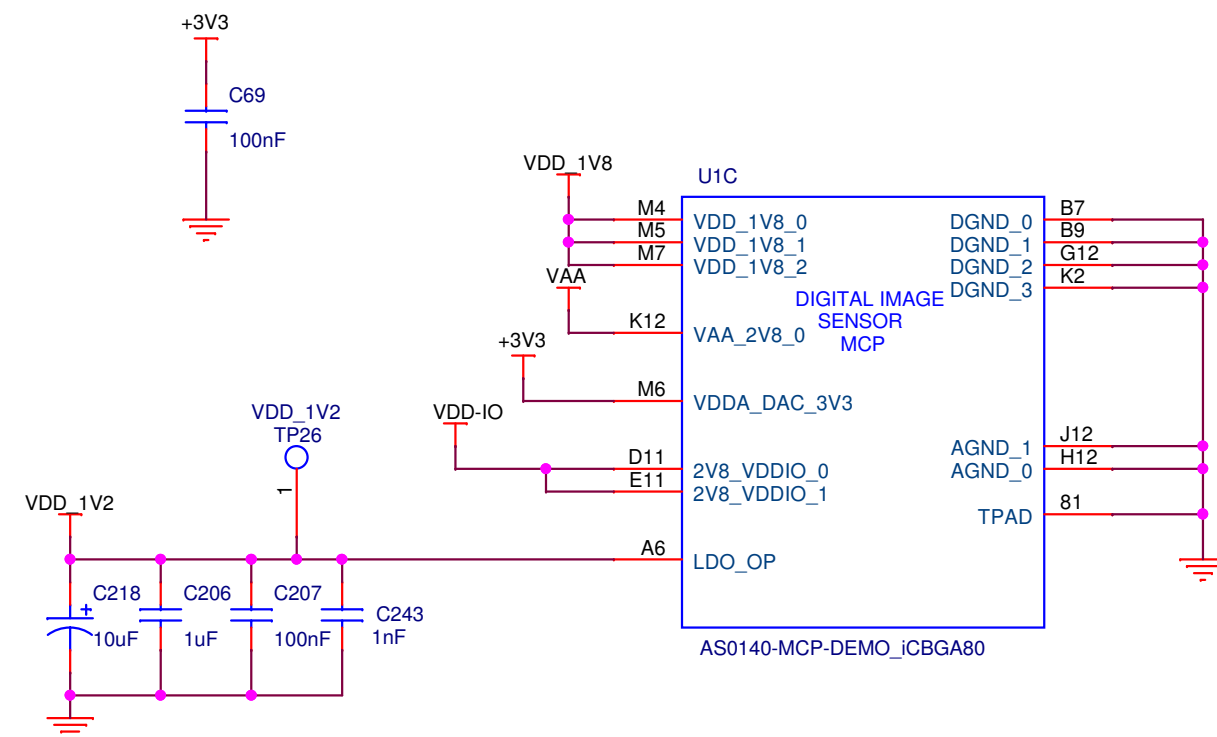
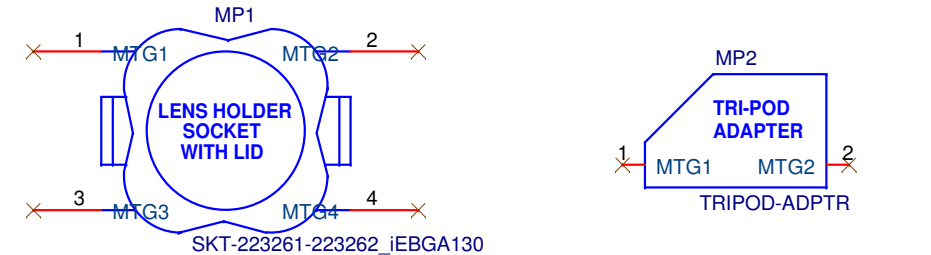


Auto-config Mode Selections

P9 (GPIO3)	=	GND->NTSC	or	HIGH->PAL
P7 (GPIO5)	=	GND->Normal	or	HIGH->Vertical Flip
P8 (GPIO4)	=	GND->Normal	or	HIGH->Horizontal Flip
P10 (GPIO2)	=	GND->No Pedestal	or	HIGH->Pedestal



Socket/Lens Mount



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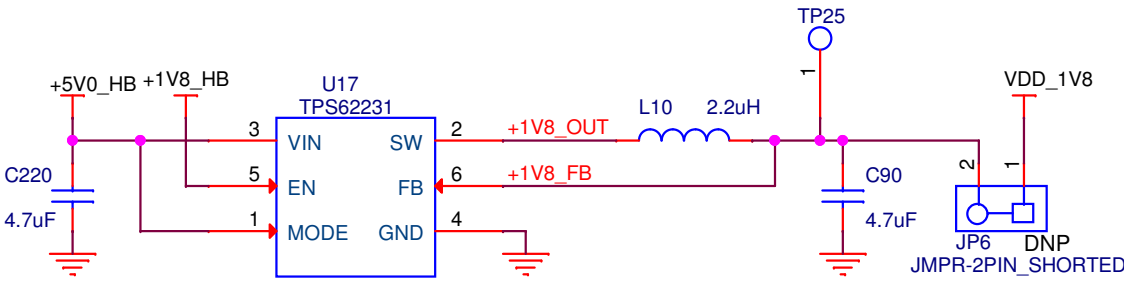
Title Sensor		
Size C	Document Name AS0140_80ICBGA_DEMO3HEAD_Card	Rev 1.0
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Debug Headers: Cut away the shorted trace and mount header for power debugging

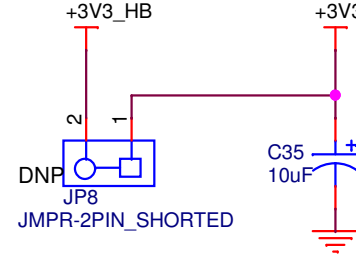
Power

+5V0_HB		+5V0_HB	8
+3V3_HB		+3V3_HB	8
+2V8_VAA_HB		+2V8_VAA_HB	8
+2V8_VDDIO_HB		+2V8_VDDIO_HB	8
+1V8_HB		+1V8_HB	8
+3V3		+3V3	5,7,9
+VDDIO_LS		+VDDIO_LS	5,7,8,9
VDD_1V2		VDD_1V2	5
VDD_1V8		VDD_1V8	5,8
VDD_IO		VDD_IO	5
VAA		VAA	5

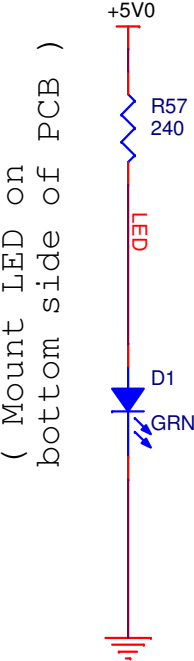
VDD_1V8 1.8V SUPPLY



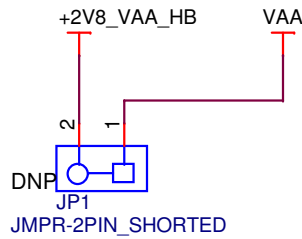
PERIPHERAL 3.3V SUPPLY



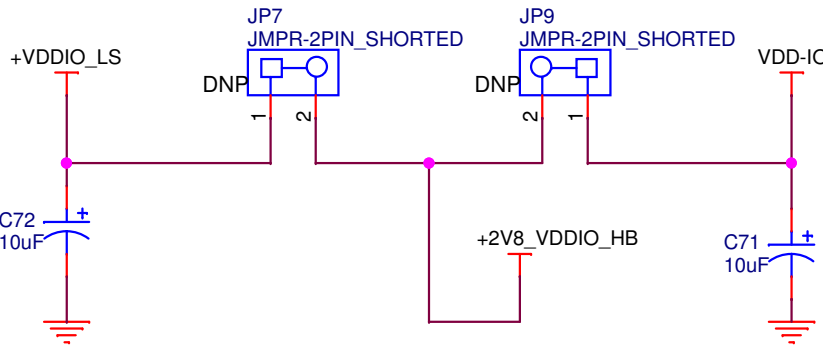
5V LED



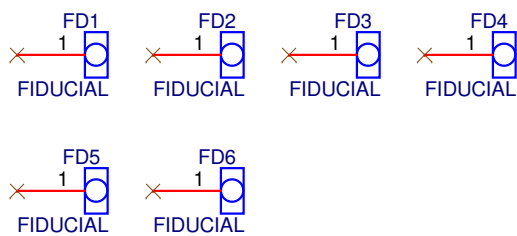
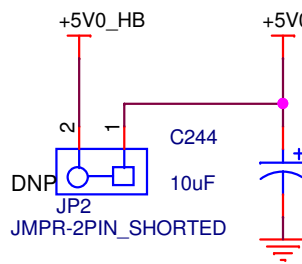
VAA 2.8V SUPPLY



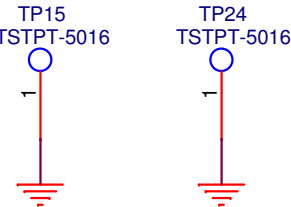
VDDIO & VDDIO_LS 2.8V SUPPLY



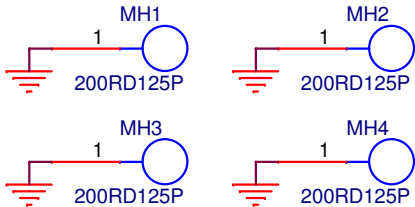
+5V0 SUPPLY



Ground Testpoints



Mounting Holes



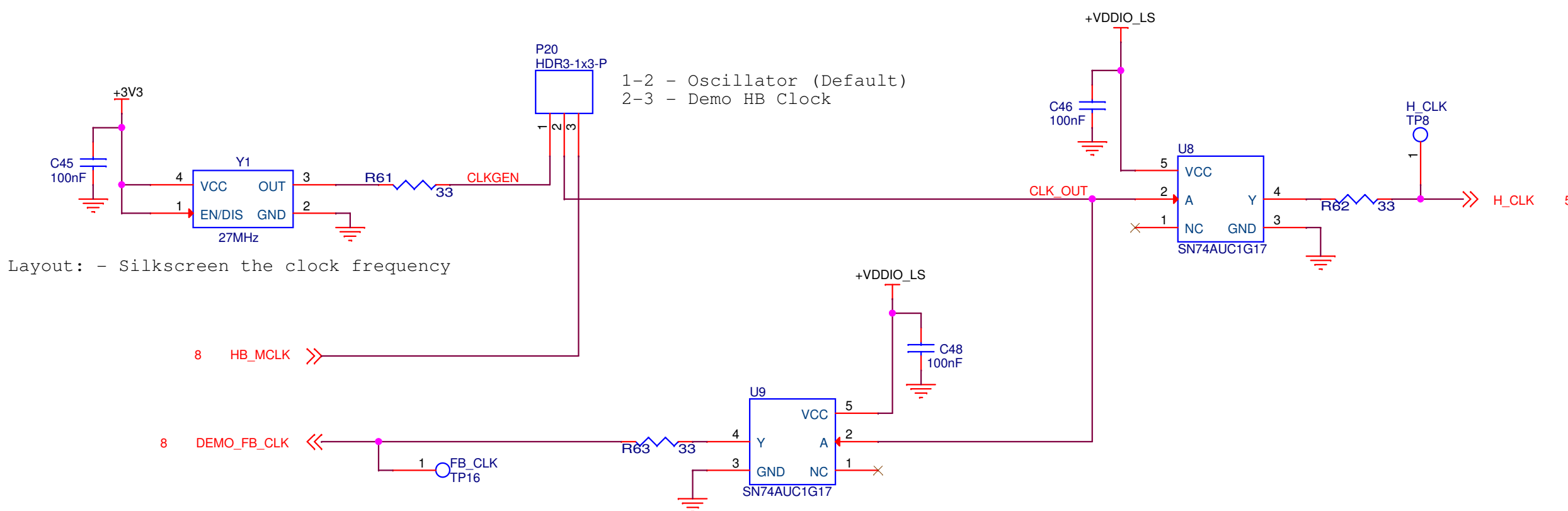
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Title	Power	Rev	1.0
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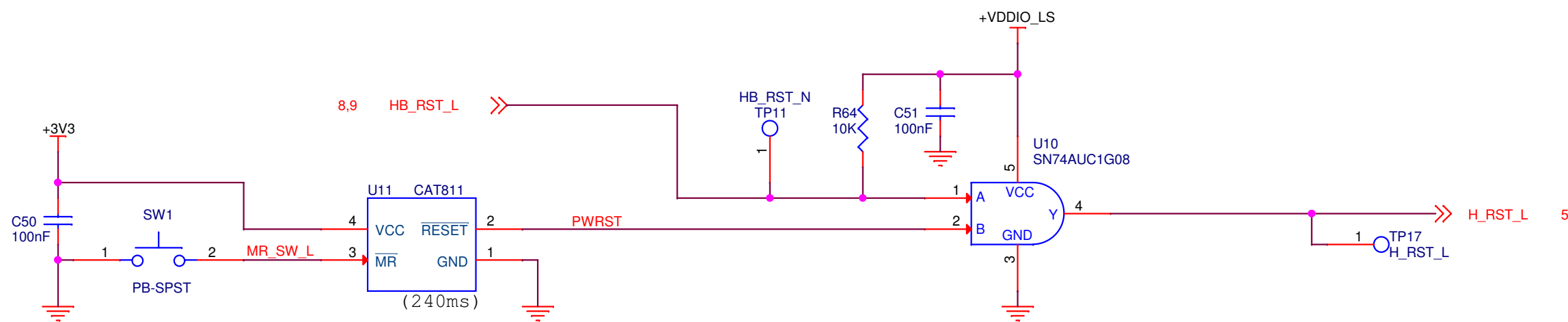
Clock and Reset

+3V3 +VDDIO_LS 5,6,9
+VDDIO_LS +VDDIO_LS 5,6,8,9

CLOCK CIRCUIT



RESET CIRCUIT



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Title
Clock and Reset

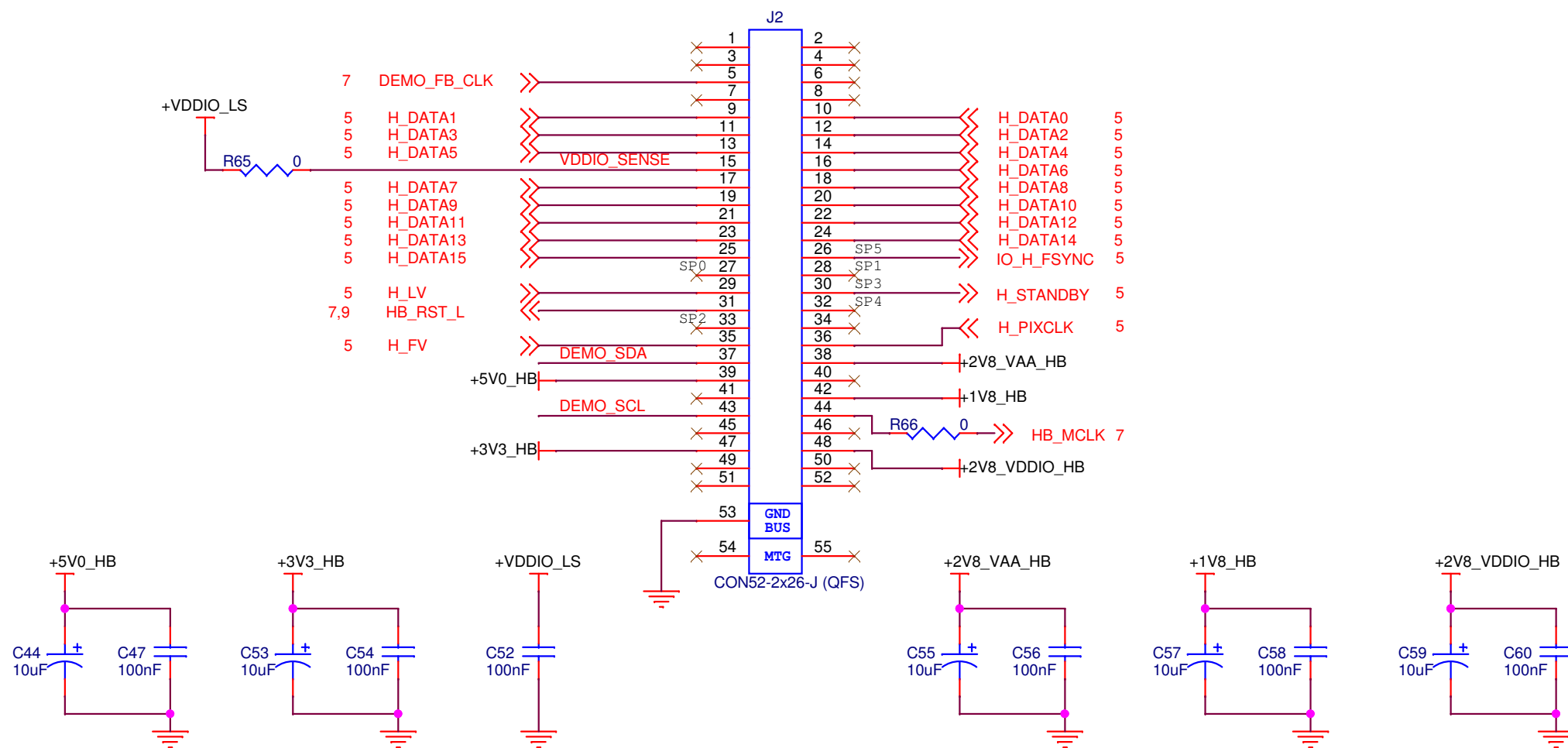
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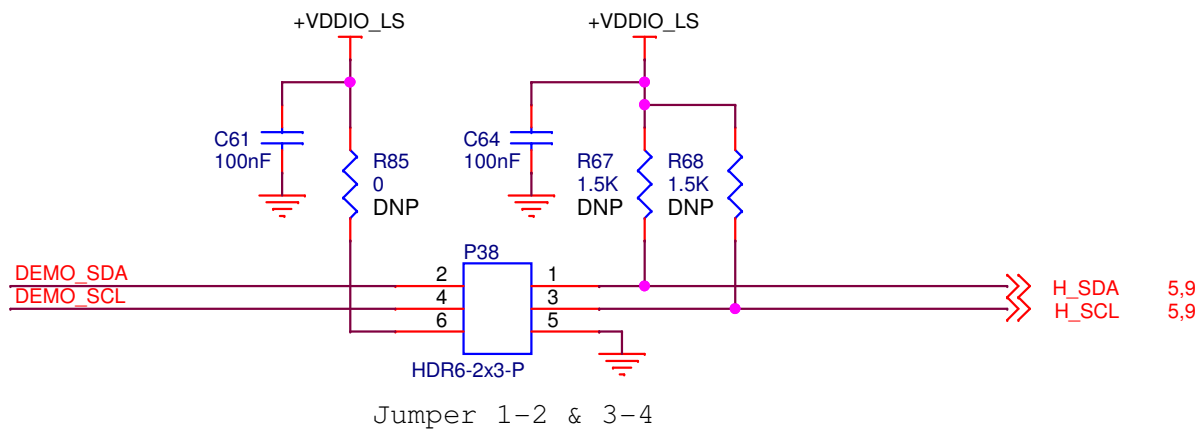
External Interface

+5V0_HB		+5V0_HB	6
+3V3_HB		+3V3_HB	6
+2V8_VAA_HB		+2V8_VAA_HB	6
+2V8_VDDIO_HB		+2V8_VDDIO_HB	6
+1V8_HB		+1V8_HB	6
+3V3		+3V3	5,6,7,9
+VDDIO_LS		+VDDIO_LS	5,6,7,9
VDD_1V8		VDD_1V8	5,6

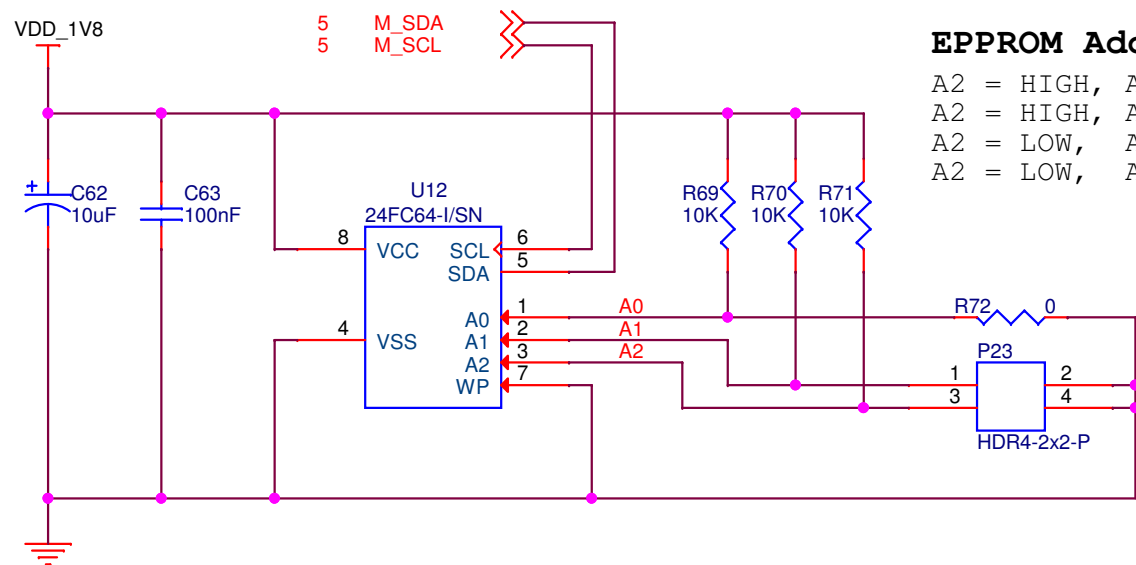
DEMO3 BASEBOARD I/F



I2C DEBUG



LENS CORRECTION EEPROM



EEPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0



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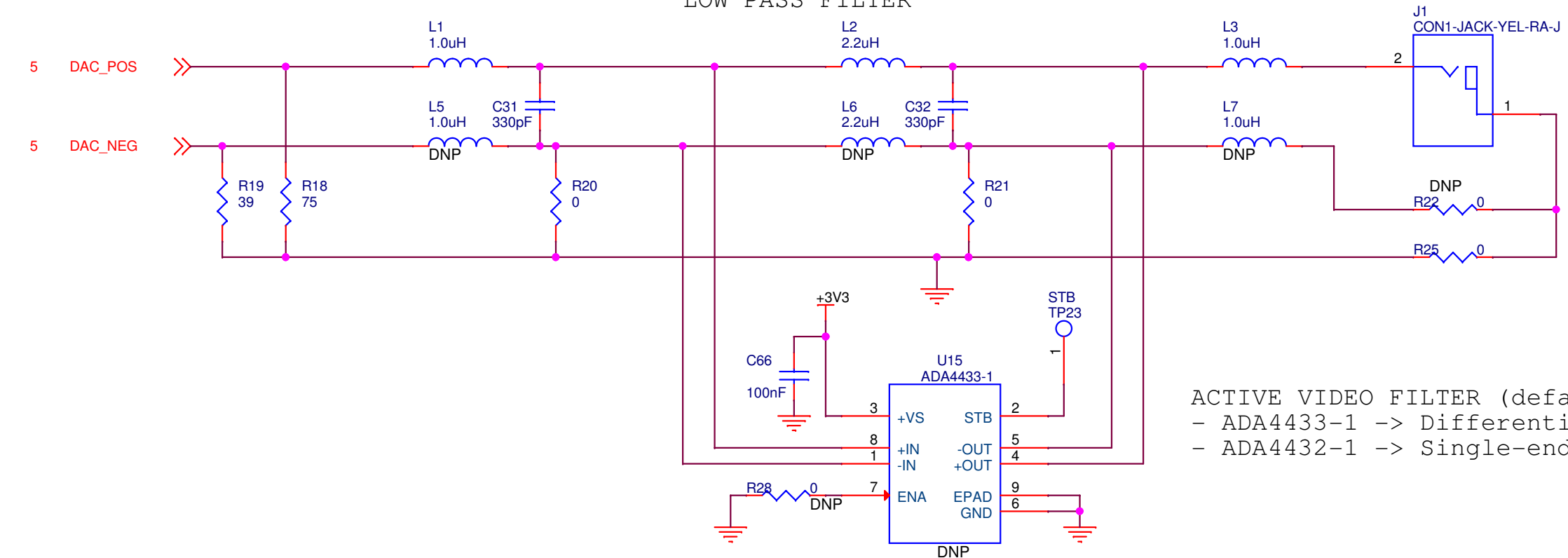
Title External Interface		
Size C	Document Name AS0140_80ICBGA_DEMO3HEAD_Card	Rev 1.0
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Automotive, I/O, Video and SPI

+3V3 +VDDIO_LS +3V3 5,6,7 +VDDIO_LS 5,6,7,8

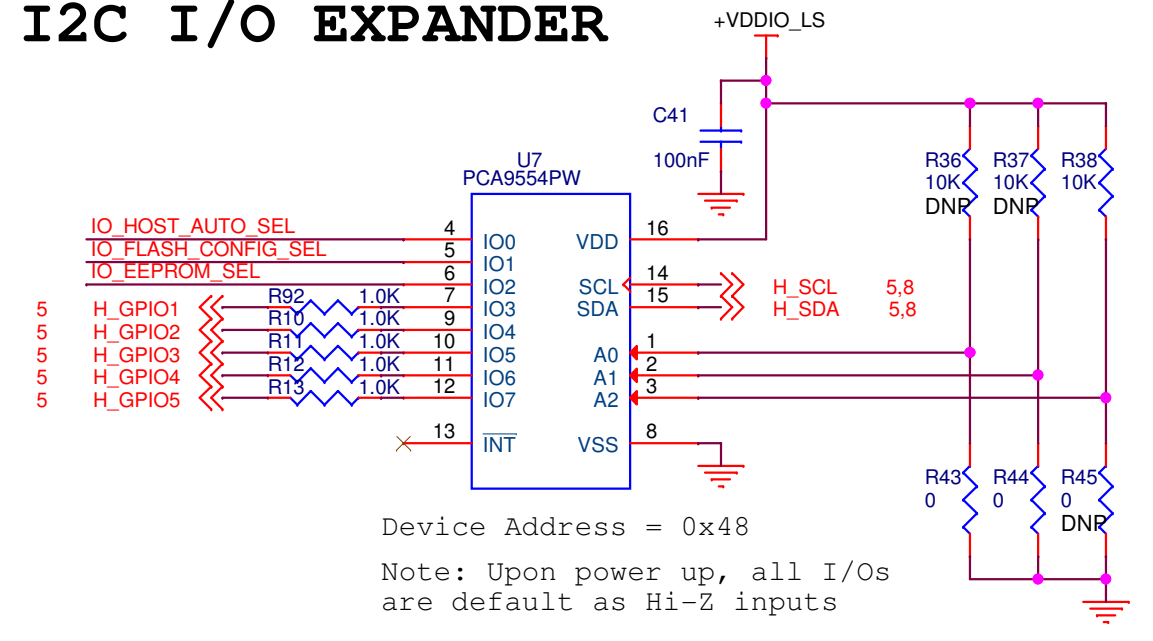
VIDEO OUT

LOW PASS FILTER

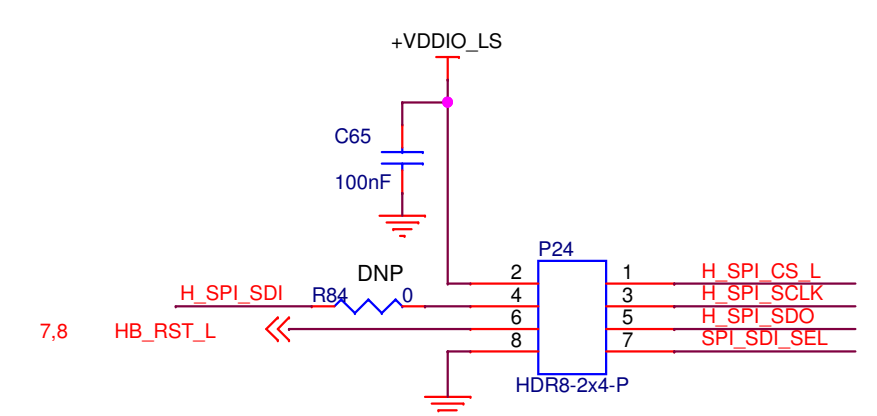


ACTIVE VIDEO FILTER (default - Not Use)
- ADA4433-1 -> Differential Type
- ADA4432-1 -> Single-ended Type

I2C I/O EXPANDER



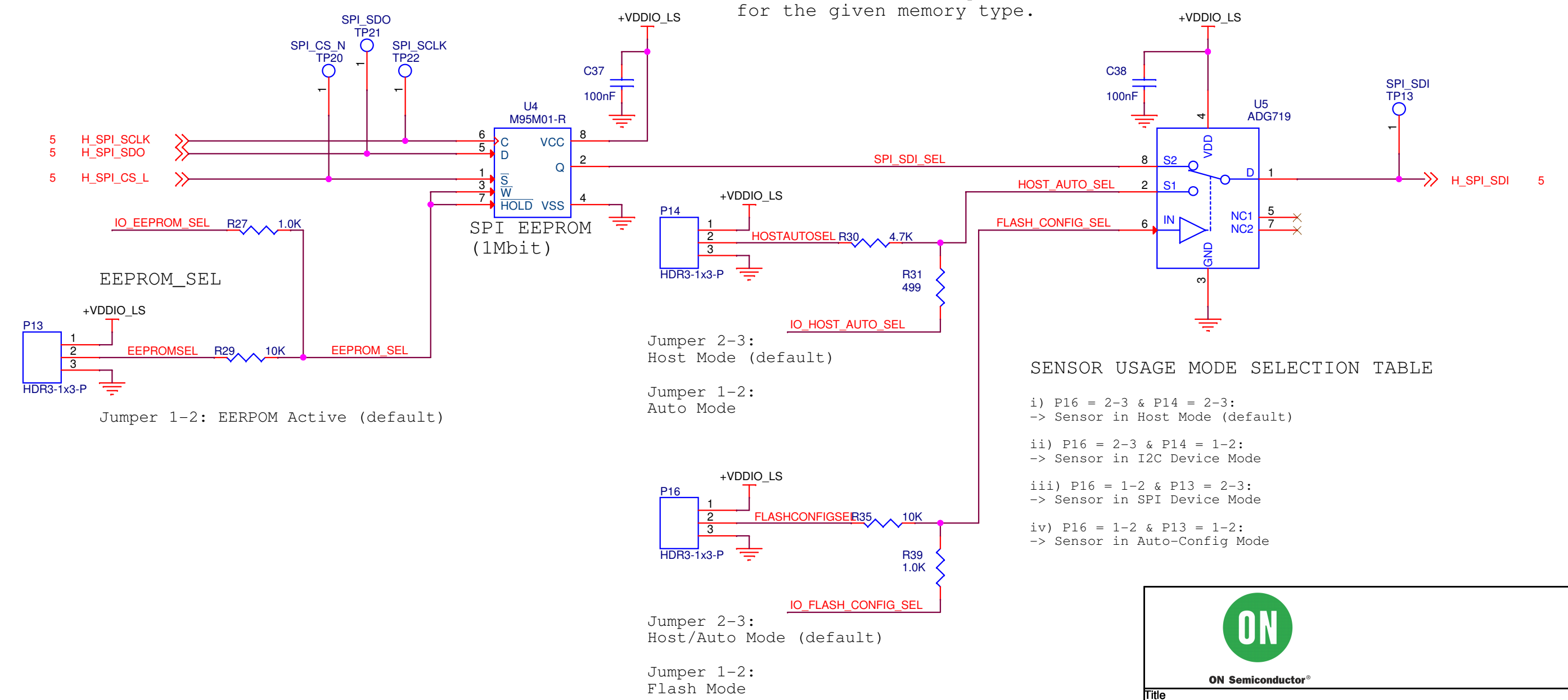
Device Address = 0x48
Note: Upon power up, all I/Os are default as Hi-Z inputs



SPI PROGRAMMING CONNECTOR

SPI MEMORY

To use socketed memory, replace U4 with Samtec FLE-104-01-G-DV. Use Accutec AK08SOIC-ST SOIC adapter for the given memory type.



SENSOR USAGE MODE SELECTION TABLE

- i) P16 = 2-3 & P14 = 2-3:
-> Sensor in Host Mode (default)
- ii) P16 = 2-3 & P14 = 1-2:
-> Sensor in I2C Device Mode
- iii) P16 = 1-2 & P13 = 2-3:
-> Sensor in SPI Device Mode
- iv) P16 = 1-2 & P13 = 1-2:
-> Sensor in Auto-Config Mode



Automotive		
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