# MCIMX8M-EVKB (i.MX8M Customer Board)

# Schematics DevBoard

## Table of Content



## Revision History

| Rev. Code | Date | By | | Description |
|---|---|---|---|---|
| A | 2018-09-06 | Javen | 1 | Revision preliminary version |
| A1 | 2019-03-12 | Javen | 1 | Replace PTN5110DHQ with PTN5110NHQZ for U907<br>Replace PTN36043BX with PTN36043ABX for U901<br>DNP R905,R909,R910,R911<br>DNP 280-76498(BH1401-BH1404)<br>Update U101 with new PN MIMX8MQ6DVAJZAB<br>Update U1602 to IRM-V538M3/TR1 |

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

**Preliminary - Subject to Change without Notice!**

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.


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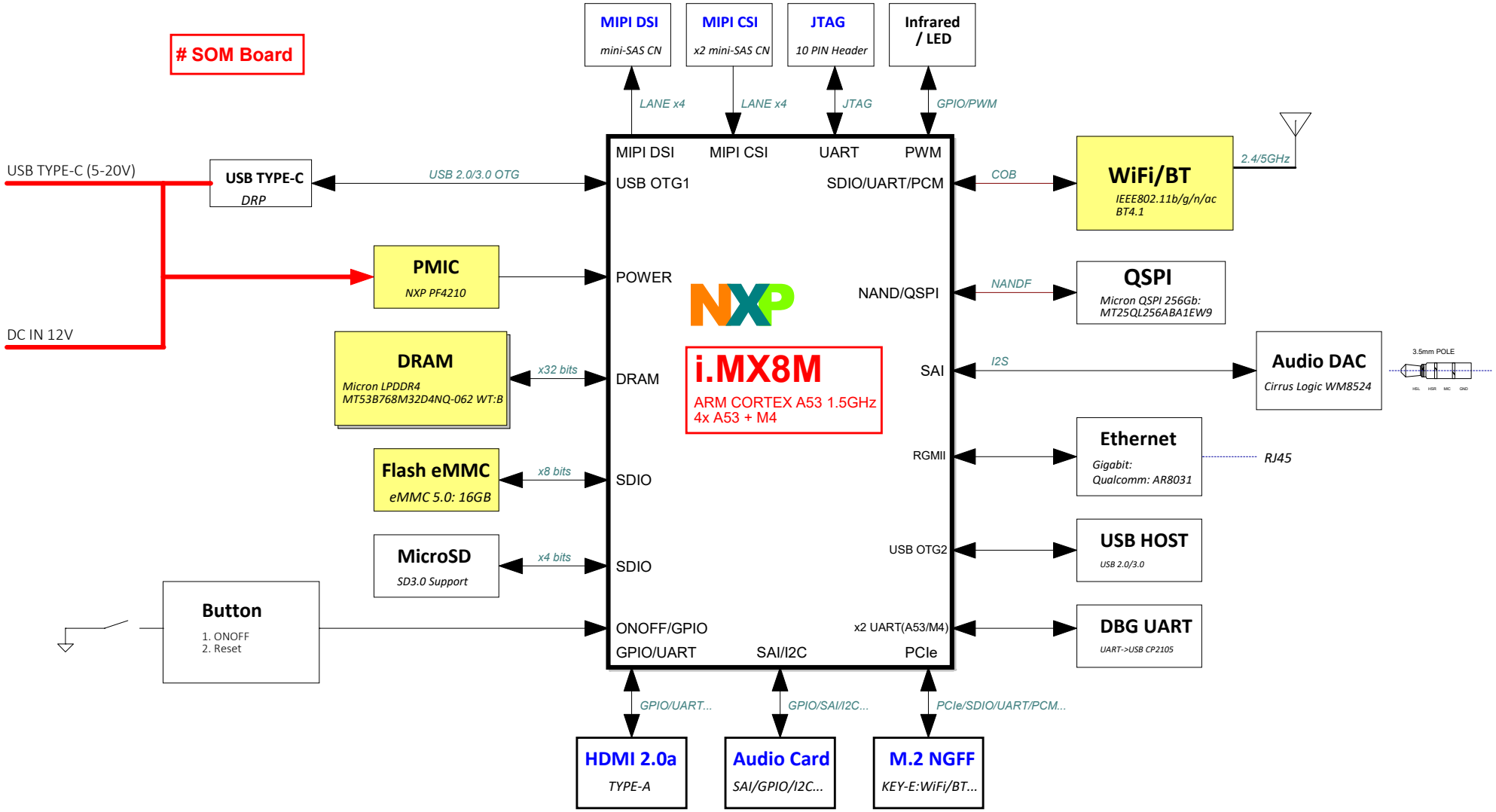
ICAP Classification: CP: IUO: X PUBI:

| | | | |
|---|---|---|---|
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: Title and Rev History | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 1 of 23 | |

# i.MX8M EVK BLOCK DIAGRAM

##### MCIMX8M-EVKB #####

SoC: MIMX8MQ6DVAJZAA



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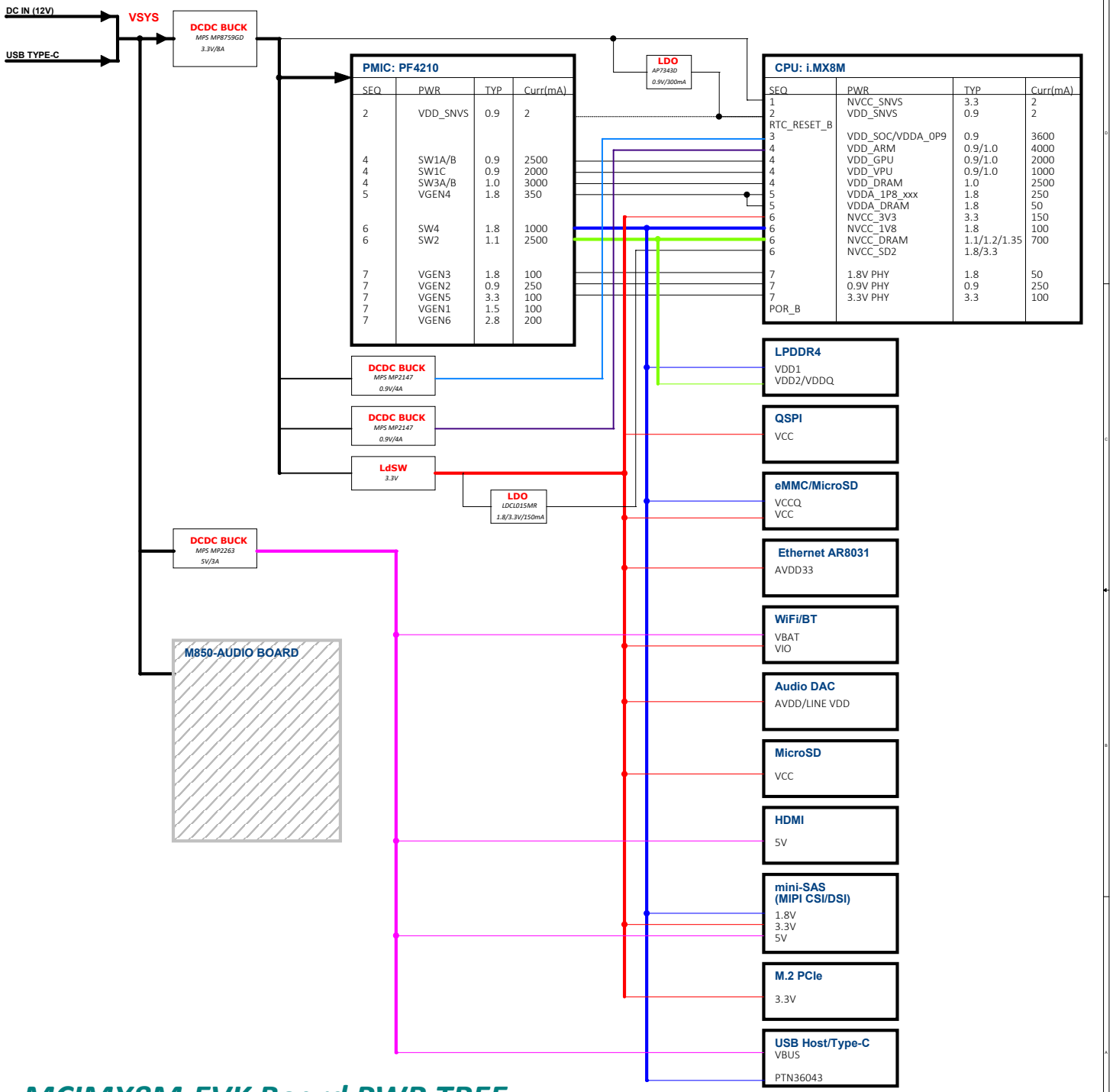
| Drawn by: <JW> | Page Title: Block Diagram | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 2 of 23 |

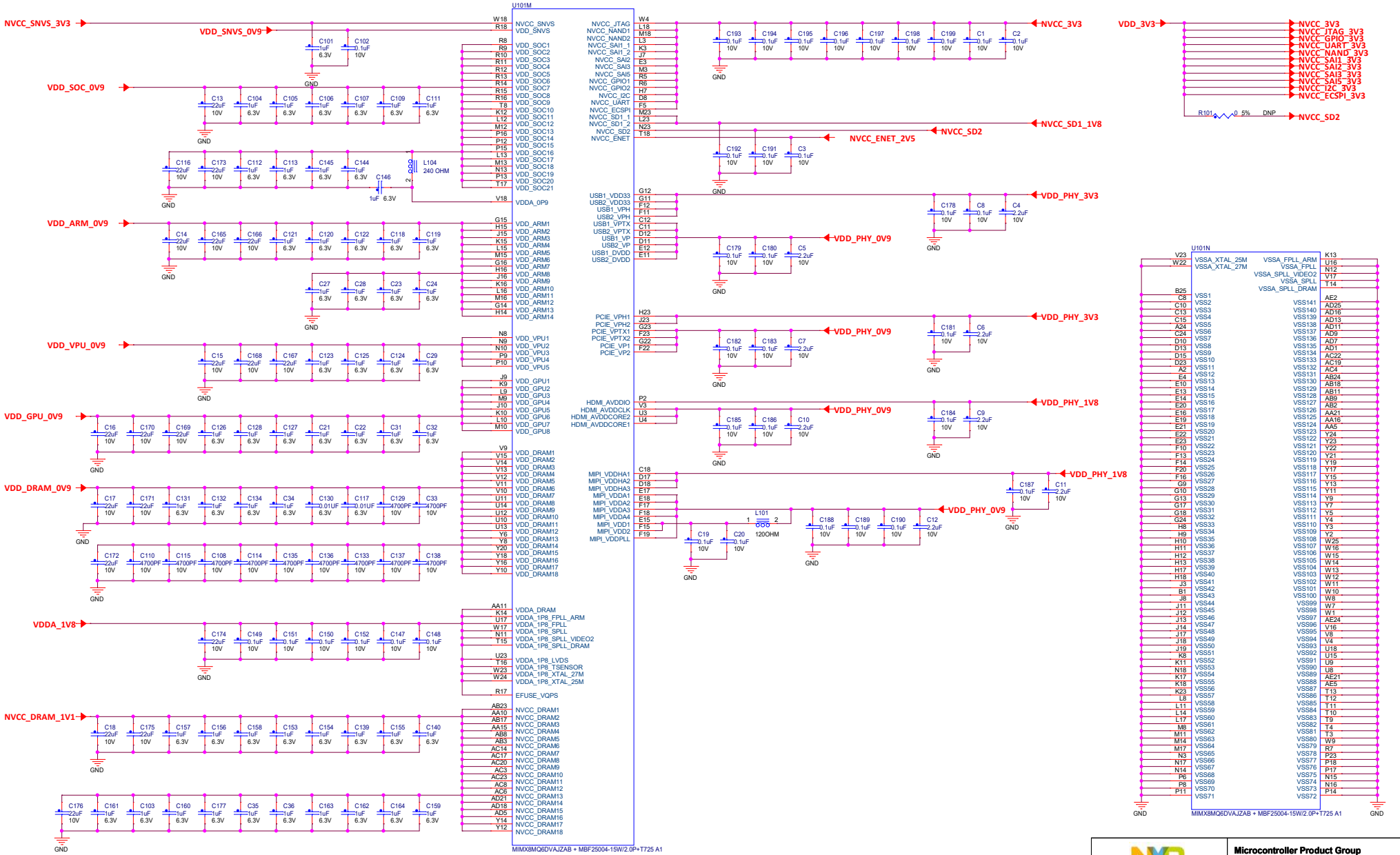



# MCIMX8M-EVK Board PWR TREE



| | | |
|---|---|---|
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | |
| Drawn by: <JW> | Page Title: Power Tree | |
| Approved: <Approver> | Size: Custom; Document Number: SCH-38820 PDF: SPF-38820 | Rev: A1 |
| | Date: Thursday, April 25, 2019 | Sheet 3 of 23 |

# i.MX8M PWR





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| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: CPU PWR | | |
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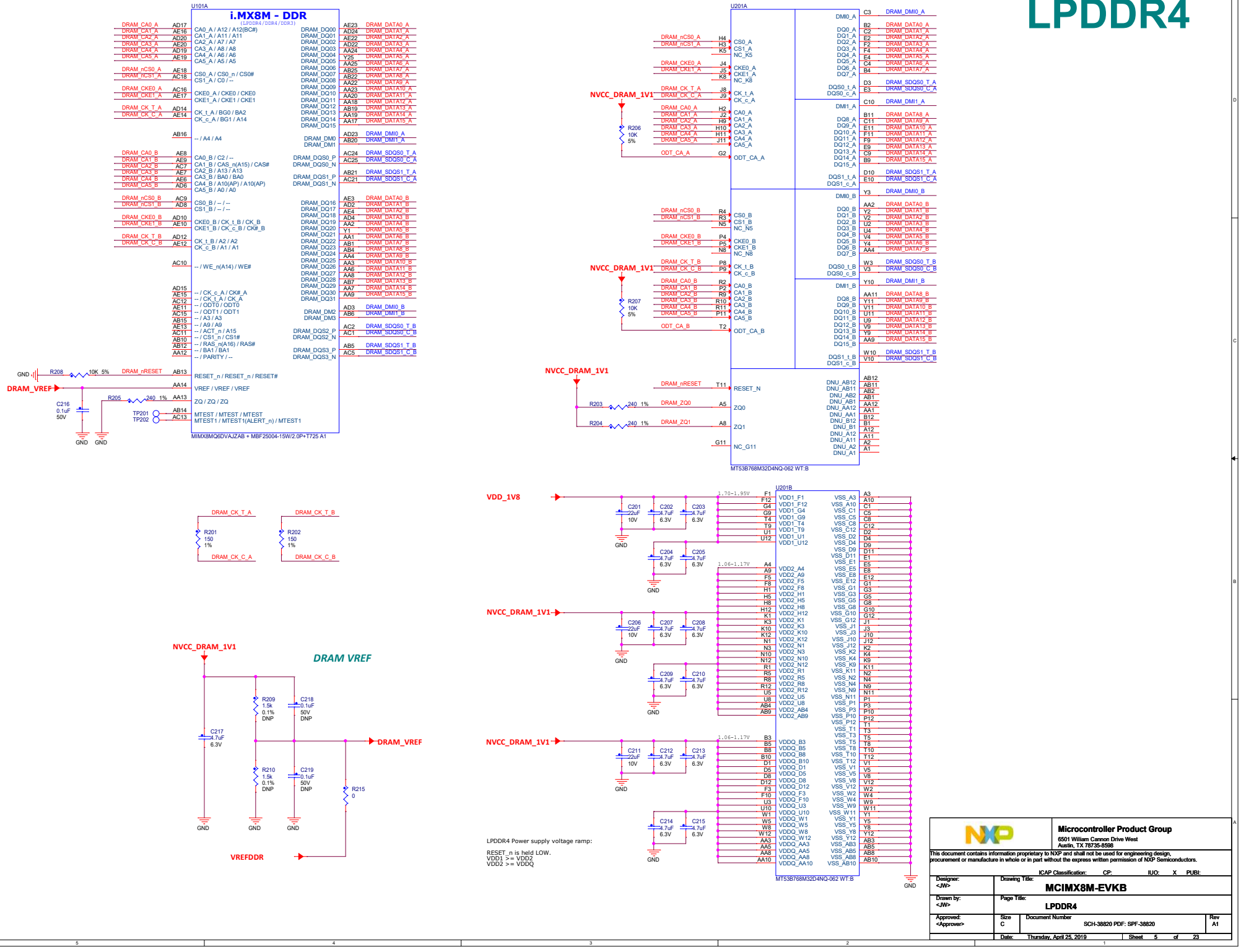
| | Date: Thursday, April 25, 2019 | Sheet 4 of 23 | |

# LPDDR4


U101A
i.MX8M - DDR
(LPDDR4 / DDR4 / DDR3)
MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1
U201A
MT53B768M32D4NQ-062 WT:B
U201B
MT53B768M32D4NQ-062 WT:B
NVCC_DRAM_1V1
VDD_1V8
DRAM_VREF
DRAM VREF
VREFDDR
LPDDR4 Power supply voltage ramp:
RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ
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Drawn by: <JW>
Page Title: LPDDR4
Approved: <Approver>
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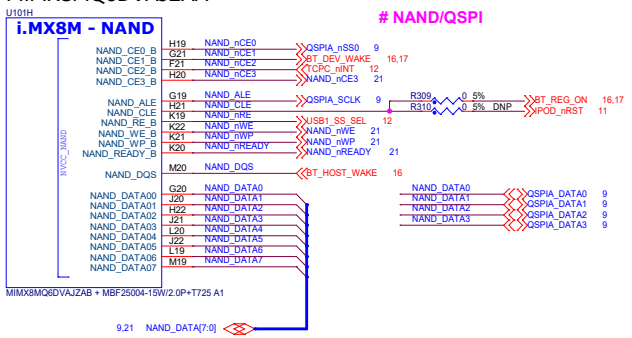
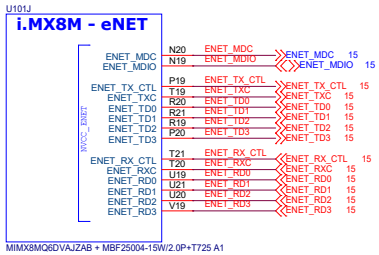
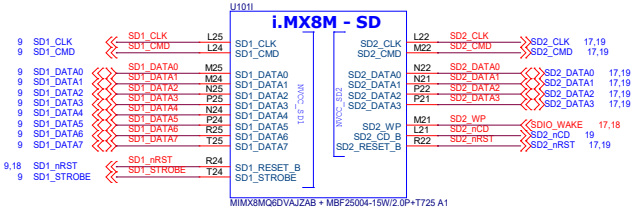
Date: Thursday, April 25, 2019
Sheet 5 of 23

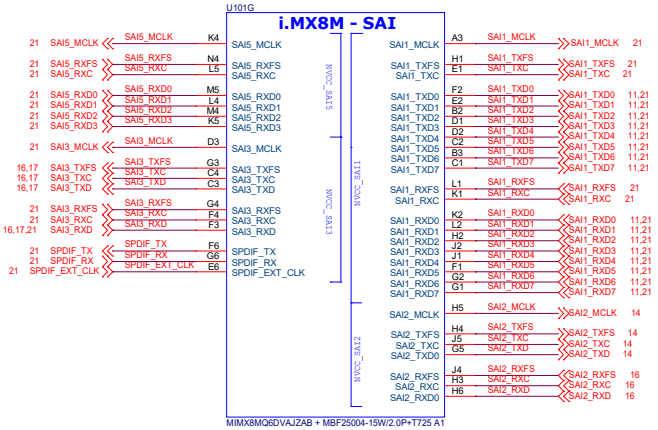
MIMX8MQ6DVAJZAA

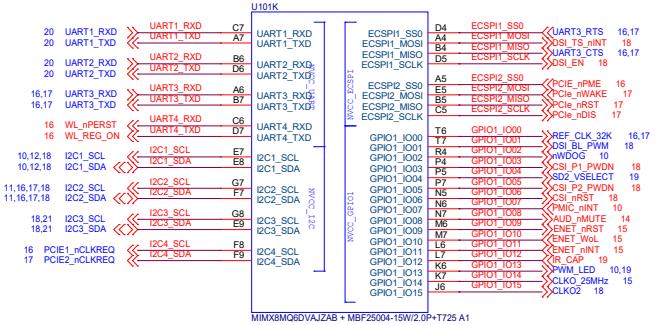
-Internal pullup resistors 27 kOhm;
-Internal pulldown resistor of 90kOhm is always enabled



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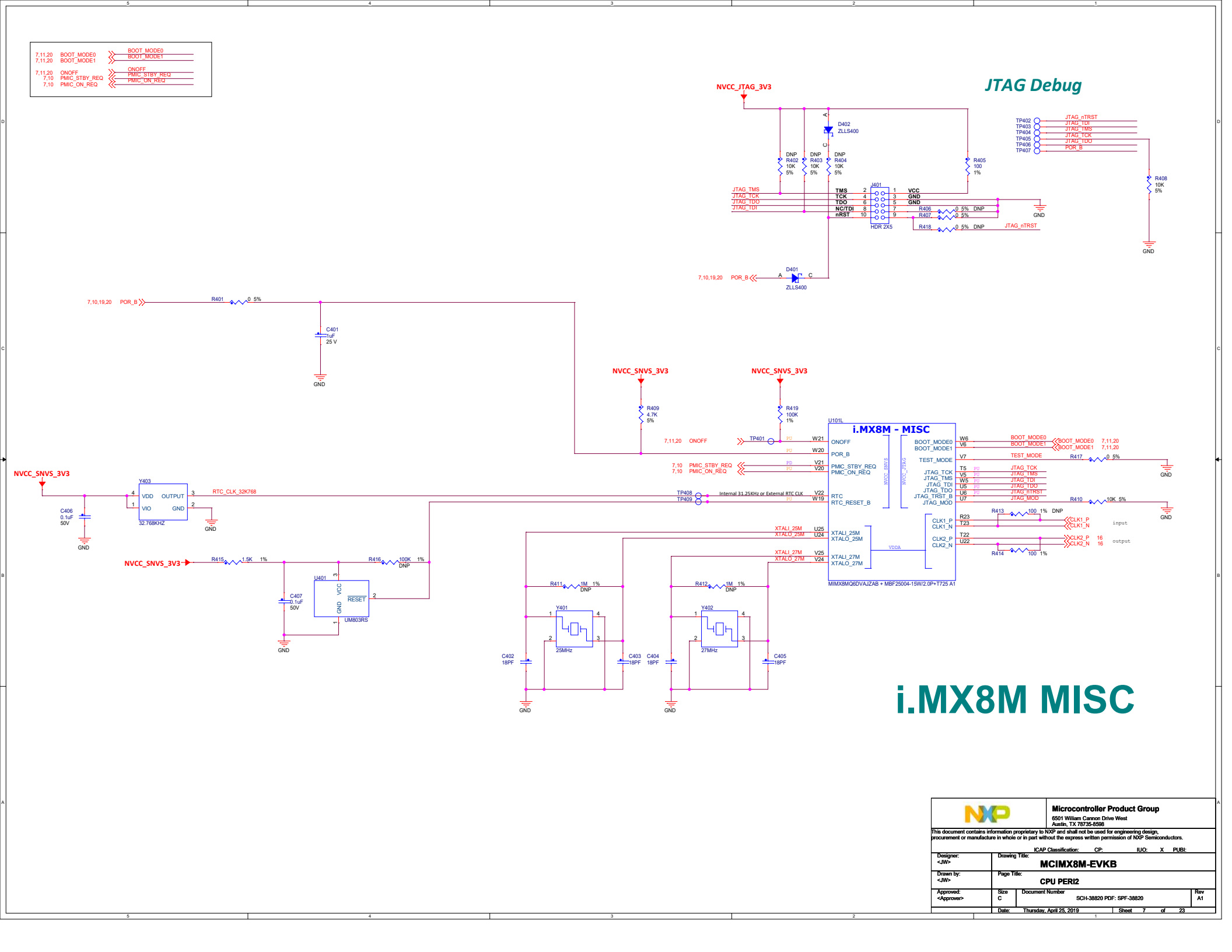
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 6 of 23 | |


JTAG Debug
i.MX8M MISC
i.MX8M - MISC
NVCC_JTAG_3V3
NVCC_SNVS_3V3
D402 ZLLS400
D401 ZLLS400
J401 HDR 2X5
U101L
MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1
Y401 25MHz
Y402 27MHz
Y403 32.768KHZ
U401 UM803RS
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# i.MX8M PHY

VDD_PHY_3V3 → VDD_PHY_3V3
VDD_PHY_1V8 → VDD_PHY_1V8
VDD_PHY_0V9 → VDD_PHY_0V9

USB_RESREF: Attach a 200-Ω 1% 100-ppm/C precision resistor-to-ground on the board.
MIPIDSI REXT: 15K-Ω
PCIE: Z00-Ω±1% ± 100 ppm/°C precision resistor to-ground on the board.
HDMI:a 499Ω (±1% tolerance) resistor to-ground on the board

U101E
## i.MX8M - CSI

| | | | |
|---|---|---|---|
| MIPI_CSI1_CLK_N | A22 | CSI_P1_CKN | CSI_P1_CKN 18 |
| MIPI_CSI1_CLK_P | B22 | CSI_P1_CKP | CSI_P1_CKP 18 |
| MIPI_CSI1_D0_N | A23 | CSI_P1_DN0 | CSI_P1_DN0 18 |
| MIPI_CSI1_D0_P | B23 | CSI_P1_DP0 | CSI_P1_DP0 18 |
| MIPI_CSI1_D1_N | C22 | CSI_P1_DN1 | CSI_P1_DN1 18 |
| MIPI_CSI1_D1_P | D22 | CSI_P1_DP1 | CSI_P1_DP1 18 |
| MIPI_CSI1_D2_N | B24 | CSI_P1_DN2 | CSI_P1_DN2 18 |
| MIPI_CSI1_D2_P | C23 | CSI_P1_DP2 | CSI_P1_DP2 18 |
| MIPI_CSI1_D3_N | C21 | CSI_P1_DN3 | CSI_P1_DN3 18 |
| MIPI_CSI1_D3_P | D21 | CSI_P1_DP3 | CSI_P1_DP3 18 |
| MIPI_CSI2_CLK_N | A19 | CSI_P2_CKN | CSI_P2_CKN 18 |
| MIPI_CSI2_CLK_P | B19 | CSI_P2_CKP | CSI_P2_CKP 18 |
| MIPI_CSI2_D0_N | C20 | CSI_P2_DN0 | CSI_P2_DN0 18 |
| MIPI_CSI2_D0_P | D20 | CSI_P2_DP0 | CSI_P2_DP0 18 |
| MIPI_CSI2_D1_N | A20 | CSI_P2_DN1 | CSI_P2_DN1 18 |
| MIPI_CSI2_D1_P | B20 | CSI_P2_DP1 | CSI_P2_DP1 18 |
| MIPI_CSI2_D2_N | A21 | CSI_P2_DN2 | CSI_P2_DN2 18 |
| MIPI_CSI2_D2_P | B21 | CSI_P2_DP2 | CSI_P2_DP2 18 |
| MIPI_CSI2_D3_N | C19 | CSI_P2_DN3 | CSI_P2_DN3 18 |
| MIPI_CSI2_D3_P | D19 | CSI_P2_DP3 | CSI_P2_DP3 18 |

CSI_P1_VDDHA, CSI_P2_VDDHA

MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1

U101C
## i.MX8M - PCIe

| | | | |
|---|---|---|---|
| PCIE1_TXN_N | J24 | PCIE1_TXM | PCIE1_TXN 16 |
| PCIE1_TXN_P | J25 | PCIE1_TXP | PCIE1_TXP 16 |
| PCIE1_RXN_N | H24 | PCIE1_RXM | PCIE1_RXN 16 |
| PCIE1_RXN_P | H25 | PCIE1_RXP | PCIE1_RXP 16 |
| PCIE1_REF_PAD_CLK_N | K24 | PCIE1_REF_CLKM | PCIE1_REF_CLKN 16 |
| PCIE1_REF_PAD_CLK_P | K25 | PCIE1_REF_CLKP | PCIE1_REF_CLKP 16 |
| PCIE1_RESREF | G25 | R501 200 1% | GND |
| PCIE2_TXN_N | E24 | PCIE2_TXM | PCIE2_TXN 17 |
| PCIE2_TXN_P | E25 | PCIE2_TXP | PCIE2_TXP 17 |
| PCIE2_RXN_N | D24 | PCIE2_RXM | PCIE2_RXN 17 |
| PCIE2_RXN_P | D25 | PCIE2_RXP | PCIE2_RXP 17 |
| PCIE2_REF_PAD_CLK_N | F24 | PCIE2_REF_CLKM | PCIE2_REF_CLKN 17 |
| PCIE2_REF_PAD_CLK_P | F25 | PCIE2_REF_CLKP | PCIE2_REF_CLKP 17 |
| PCIE2_RESREF | C25 | R502 200 1% | GND |

PCIE0_VPH, PCIE1_VPH

MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1

U101F
## i.MX8M - HDMI

| | | | |
|---|---|---|---|
| HDMI_DDC_SCL | R3 | HDMI_DDC_SCL | HDMI_DDC_SCL 13 |
| HDMI_DDC_SDA | P3 | HDMI_DDC_SDA | HDMI_DDC_SDA 13 |
| HDMI_HPD | W2 | HDMI_HPD | HDMI_HPD 13 |
| HDMI_CEC | W3 | HDMI_CEC | HDMI_CEC 13 |
| | | AC coupled differential low swing clock (HCSL levels) | |
| HDMI_REFCLK_N | R1 | HDMI_REFCLKN | |
| HDMI_REFCLK_P | R2 | HDMI_REFCLKP | |
| HDMI_TX_M_LN_0 | T2 | HDMI_TXN0 | HDMI_TXN0 13 |
| HDMI_TX_P_LN_0 | T1 | HDMI_TXP0 | HDMI_TXP0 13 |
| HDMI_TX_M_LN_1 | U1 | HDMI_TXN1 | HDMI_TXN1 13 |
| HDMI_TX_P_LN_1 | U2 | HDMI_TXP1 | HDMI_TXP1 13 |
| HDMI_TX_M_LN_2 | N1 | HDMI_TXN2 | HDMI_TXN2 13 |
| HDMI_TX_P_LN_2 | N2 | HDMI_TXP2 | HDMI_TXP2 13 |
| HDMI_TX_M_LN_3 | M2 | HDMI_TXN3 | HDMI_CLKN 13 |
| HDMI_TX_P_LN_3 | M1 | HDMI_TXP3 | HDMI_CLKP 13 |
| HDMI_AUX_N | V2 | HDMI_AUXN | HDMI_AUXN 13 |
| HDMI_AUX_P | V1 | HDMI_AUXP | HDMI_AUXP 13 |
| HDMI_REXT | P1 | R503 499 1% | GND |

HDMI_AVDD1P0

MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1

U101D
## i.MX8M - DSI

| | | | |
|---|---|---|---|
| MIPI_DSI_CLK_N | C16 | DSI_CKN | DSI_CKN 18 |
| MIPI_DSI_CLK_P | D16 | DSI_CKP | DSI_CKP 18 |
| MIPI_DSI_D0_N | A17 | DSI_DN0 | DSI_DN0 18 |
| MIPI_DSI_D0_P | B17 | DSI_DP0 | DSI_DP0 18 |
| MIPI_DSI_D1_N | A16 | DSI_DN1 | DSI_DN1 18 |
| MIPI_DSI_D1_P | B16 | DSI_DP1 | DSI_DP1 18 |
| MIPI_DSI_D2_N | A18 | DSI_DN2 | DSI_DN2 18 |
| MIPI_DSI_D2_P | B18 | DSI_DP2 | DSI_DP2 18 |
| MIPI_DSI_D3_N | A15 | DSI_DN3 | DSI_DN3 18 |
| MIPI_DSI_D3_P | B15 | DSI_DP3 | DSI_DP3 18 |
| MIPI_DSI_REXT | C17 | R505 15K 1% | GND |

DSI_VDDHA

MIMX8MQ6DVAJZAB + MBF25004-15W/2.0P+T725 A1

U101B
## i.MX8M - USB

| | | | |
|---|---|---|---|
| USB1_VBUS | D14 | USB1_VBUS | USB1_VBUS 12 |
| USB1_DN | B14 | USB1_DN | USB1_DN 12,20 |
| USB1_DP | A14 | USB1_DP | USB1_DP 12,20 |
| USB1_ID | C14 | USB1_ID | USB1_ID |
| USB1_TX_P | A13 | USB1_TXP | USB1_TXP 12 |
| USB1_TX_N | B13 | USB1_TXN | USB1_TXN 12 |
| USB1_RX_P | A12 | USB1_RXP | USB1_RXP 12 |
| USB1_RX_N | B12 | USB1_RXN | USB1_RXN 12 |
| USB1_RESREF | A11 | R504 200 1% | GND |
| USB2_VBUS | D9 | USB2_VBUS | USB2_VBUS 12 |
| USB2_DN | B10 | USB2_DN | USB2_DN 12,17 |
| USB2_DP | A10 | USB2_DP | USB2_DP 12,17 |
| USB2_ID | C9 | USB2_ID | USB2_ID |
| USB2_TX_P | A9 | USB2_TXP | USB2_TXP 12 |
| USB2_TX_N | B9 | USB2_TXN | USB2_TXN 12 |
| USB2_RX_P | A8 | USB2_RXP | USB2_RXP 12 |
| USB2_RX_N | B8 | USB2_RXN | USB2_RXN 12 |
| USB2_RESREF | B11 | R506 200 1% | GND |

USB1_ID → TP501
USB2_ID → TP502

USB_P0_VDD33, USB_P0_VPH, USB_P1_VDD33, USB_P1_VPH

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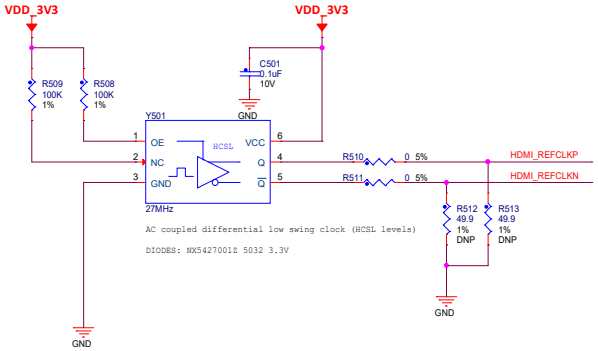


| | | | |
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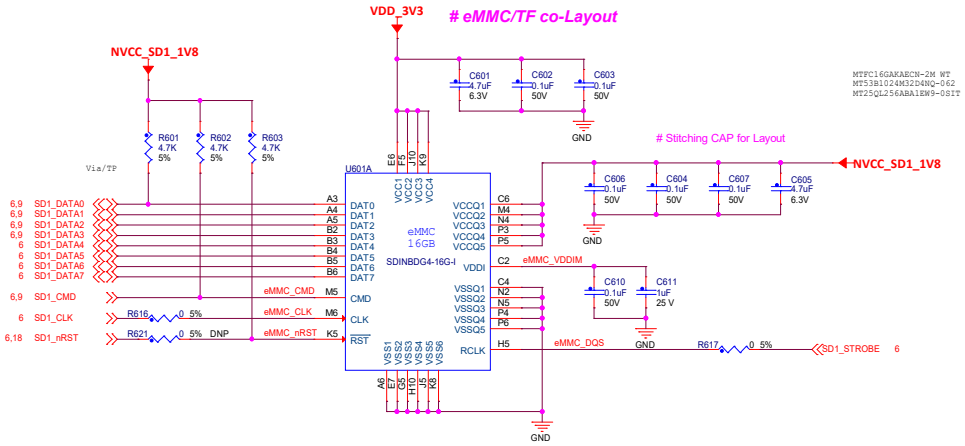
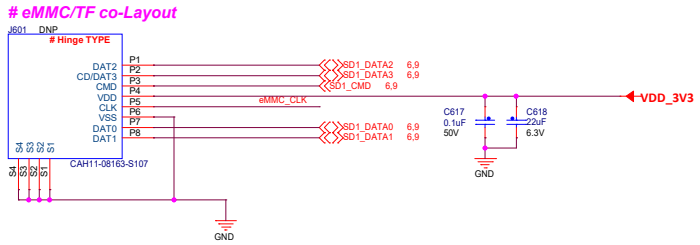
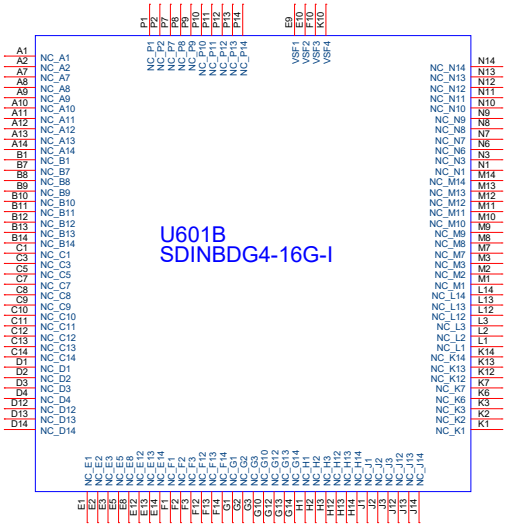
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: CPU PHY | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 8 of 23 | |

## eMMC 5.0 Footprint




## Hinge Type MicroSD

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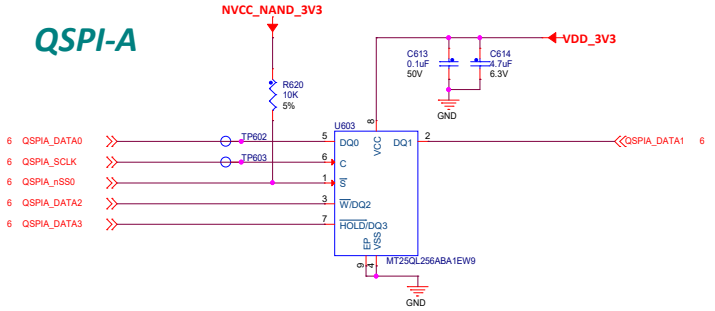



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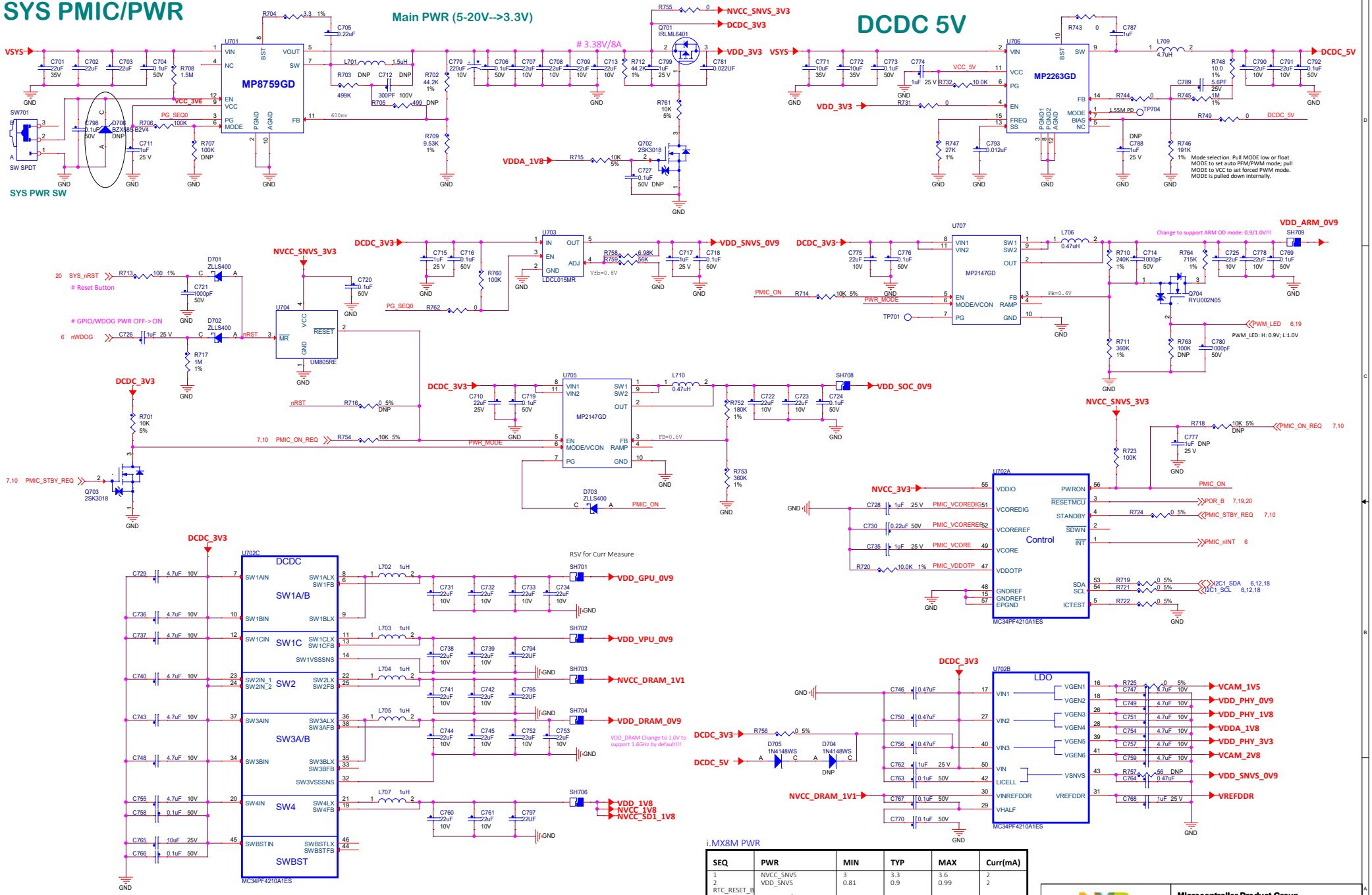
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: Flash | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 9 of 23 | |




i.MX8M PWR

| SEQ | PWR | MIN | TYP | MAX | Curr(mA) |
|---|---|---|---|---|---|
| 1 | NVCC_SNVS | 3 | 3.3 | 3.6 | 2 |
| 2 | VDD_SNVS | 0.81 | 0.9 | 0.99 | 2 |
| RTC_RESET_B | | | | | |
| 3 | VDD_SOC/VDDA_0P9 | 0.81 | 0.9 | 0.99 | 3600 |
| 4 | VDD_GPU | 0.81 | 0.9/1.0 | 1.1 | 2000 |
| 4 | VDD_VPU | 0.81 | 0.9/1.0 | 1.1 | 1000 |
| 4 | VDD_DRAM | 0.81 | 1.0 | 1.05 | 2500 |
| 4 | VDD_ARM | 0.81 | 0.9/1.0 | 1.1 | 4000 |
| 5 | VDDA_1P8_xxx | 1.62 | 1.8 | 1.89 | 250 |
| 5 | VDDA_DRAM | 1.71 | 1.8 | 1.89 | 50 |
| 6 | NVCC_DRAM | | 1.1/1.2/1.35 | | 2170 |
| 6 | NVCC_3V3 | 3 | 3.3 | 3.6 | 100 |
| 6 | NVCC_1V8 | 1.65 | 1.8 | 1.95 | 450 |
| 7 | 3.3V PHY | 3.069 | 3.3 | 3.63 | 100 |
| 7 | 1.8V PHY | 1.674 | 1.8 | 1.98 | 50 |
| 7 | 0.9V PHY | 0.837 | 0.9 | 0.99 | 250 |
| POR_B | | | | | |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| Drawn by: <JW> | Page Title: PMIC | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 10 of 23 | |

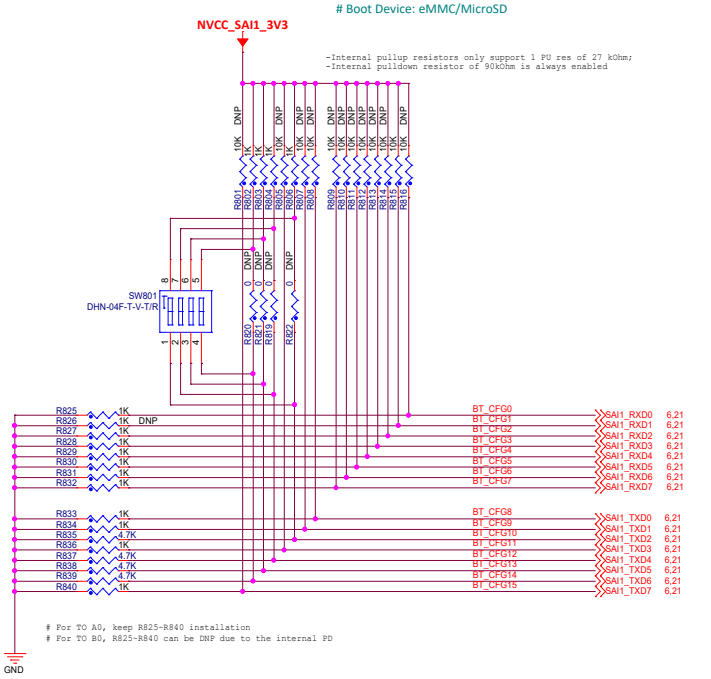
# Boot ROM Fuse

*<Default: eMMC BOOT>, QSPI boot is not supported by ROM*

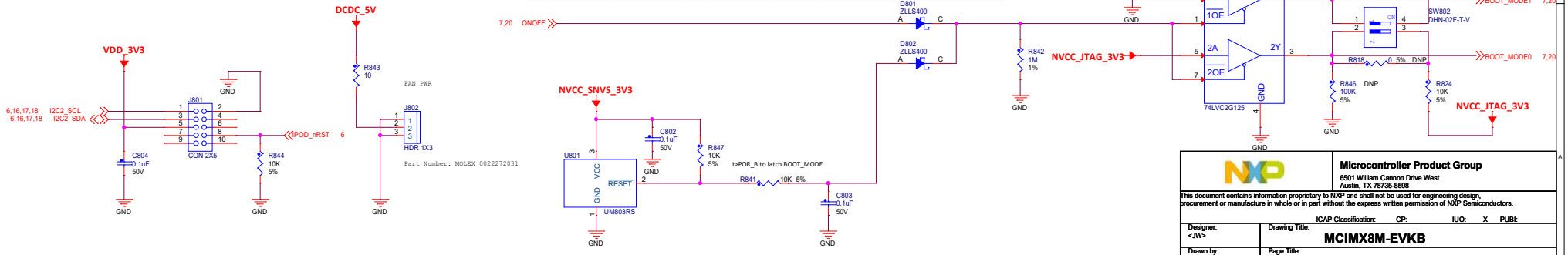
| | Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | 0x470[15:8] | **BOOT_CFG[15]** | **BOOT_CFG[14]** | **BOOT_CFG[13]** | **BOOT_CFG[12]** | **BOOT_CFG[11]** | **BOOT_CFG[10]** | **BOOT_CFG[9]** | **BOOT_CFG[8]** |
| | 0x470[15:8] | Infinit-Loop (Debug USE only)<br>0 - Disable<br>1 - Enable | 001 - SD/eSD | | | Port Select:<br>00 - eSDHC1<br>01 - eSDHC2 | | Power Cycle Enable<br>'0' - No power cycle<br>'1' - Enabled via | SD Loopback Clock Source Sel (for SDR50 and SDR104 only)<br>'0' - through SD pad<br>'1' - direct |
| | 0x470[15:8] | | 010 - MMC/eMMC | | | | | | |
| | 0x470[15:8] | | 011 - NAND | | | Pages In Block:<br>00 - 128<br>01 - 64<br>10 - 32<br>11 - 256 | | Nand_Row_address_bytes:<br>00 - 3<br>01 - 2<br>10 - 4<br>11 - 5 | |
| | 0x470[15:8] | | 100 - QSPI | | | QSPI Instance<br>0 - QuadSPI0<br>1 - Reserved | SDR SMP:<br>"000" : Default<br>"001-111" | | |
| | 0x470[15:8] | | 110 - SPI NOR | | | Port Select:<br>000 - eCSPI1<br>001 - eCSPI2 | | | SPI Addressing:<br>0 - 3-bytes (24-bit)<br>1 - 2-bytes (16-bit) |
| | 0x470[15:8] | Others - Reserved for future use | | | | | | | |
| | | **BOOT_CFG[7]** | **BOOT_CFG[6]** | **BOOT_CFG[5]** | **BOOT_CFG[4]** | **BOOT_CFG[3]** | **BOOT_CFG[2]** | **BOOT_CFG[1]** | **BOOT_CFG[0]** |
| **SD/eSD** | 0x470[7:0] | Fast Boot:<br>0 - Regular<br>1 - Fast Boot | Reserved | Reserved | Bus Width:<br>0 - 1-bit<br>1 - 4-bit | Speed<br>000 - Normal/SDR12<br>001 - High/SDR25<br>010 - SDR50<br>011 - SDR104<br>101 - Reserved for DDR50<br>Others - Reserved | | | Reserved |
| **MMC/eMMC** | 0x470[7:0] | | Bus Width:<br>000 - 1-bit<br>001 - 4-bit<br>010 - 8-bit<br>101 - 4-bit DDR (MMC 4.4)<br>110 - 8-bit DDR (MMC 4.4)<br>Else - reserved. | | | Speed<br>00 - Normal<br>01 - High<br>10 - Reserved for HS200<br>11 - Reserved | | USDHC1 IO VOLTAGE SELECTION<br>0 - 3.3V<br>1 - 1.8V | USDHC2 IO VOLTAGE SELECTION<br>0 - 3.3V<br>1 - 1.8V |
| **NAND** | 0x470[7:0] | BT_TOGGLEMODE | BOOT_SEARCH_COUNT:<br>00 - 2<br>01 - 2<br>10 - 4<br>11 - 8 | | Toggle Mode 33MHz Preamble Delay, Read Latency:<br>'000' - 16 GPMICLK cycles.<br>'001' - 1 GPMICLK cycles.<br>'010' - 2 GPMICLK cycles.<br>'011' - 3 GPMICLK cycles.<br>'100' - 4 GPMICLK cycles.<br>'101' - 5 GPMICLK cycles.<br>'110' - 6 GPMICLK cycles.<br>'111' - 7 GPMICLK cycles.<br>'1111'- 15 GPMICLK cycles. | | | Reserved |
| **QSPI** | 0x470[7:0] | HSPHS: Half Speed Phase Selection<br>0 : select sampling at non-inverted clock<br>1: select sampling at inverted clock | HSDLY: Half Speed Delay selection<br>0 : one clock delay<br>1: two clock delay | FSPHS: Full Speed Phase Selection<br>0 : select sampling at non-inverted clock<br>1: select sampling at inverted clock | FSDLY: Full Speed Delay selection<br>0 : one clock delay<br>1: two clock delay | Reserved | Reserved | Reserved | Reserved |
| **SPINOR** | 0x470[7:0] | CS select (SPI only):<br>00 - CS#0 (default)<br>01 - CS#1<br>10 - CS#2<br>11 - CS#3 | | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

| BMODE[1:0] | BOOT TYPE |
|---|---|
| 00 | Boot From Fuses |
| 01 | Serial Downloader |
| 10 | Internal Boot (Development) |
| 11 | Reserved |

# Boot Device: eMMC/MicroSD




| item | Power state | ONOFF | RST | OE | DIP SW | BM1 | BM0 | Note | Description |
|---|---|---|---|---|---|---|---|---|---|
| 1 | During Power Up | H (No press) | L | H | 1-4 : OFF; 2-3 : ON | 0 | 1 | Serial Downloader | Item 1/2 for system development |
| 2 | During Power Up | H (No press) | L | H | 1-4 : ON; 2-3 : OFF | 1 | 0 | Internal Boot | Item 2/3 for system upgrade |
| 3 | During Power Up | L (Press) | L | L | 1-4 : ON; 2-3 : OFF | 0 | 1 | Serial Downloader | |
| 4 | After Power Up | H (No press) | H | H | / | / | / | No power key event | Normal power key function |
| 5 | After Power Up | L (Short Press) | H | H | / | / | / | Power key event | |
| 6 | After Power Up | L (Long Press) | H | H | / | / | / | System power down | |





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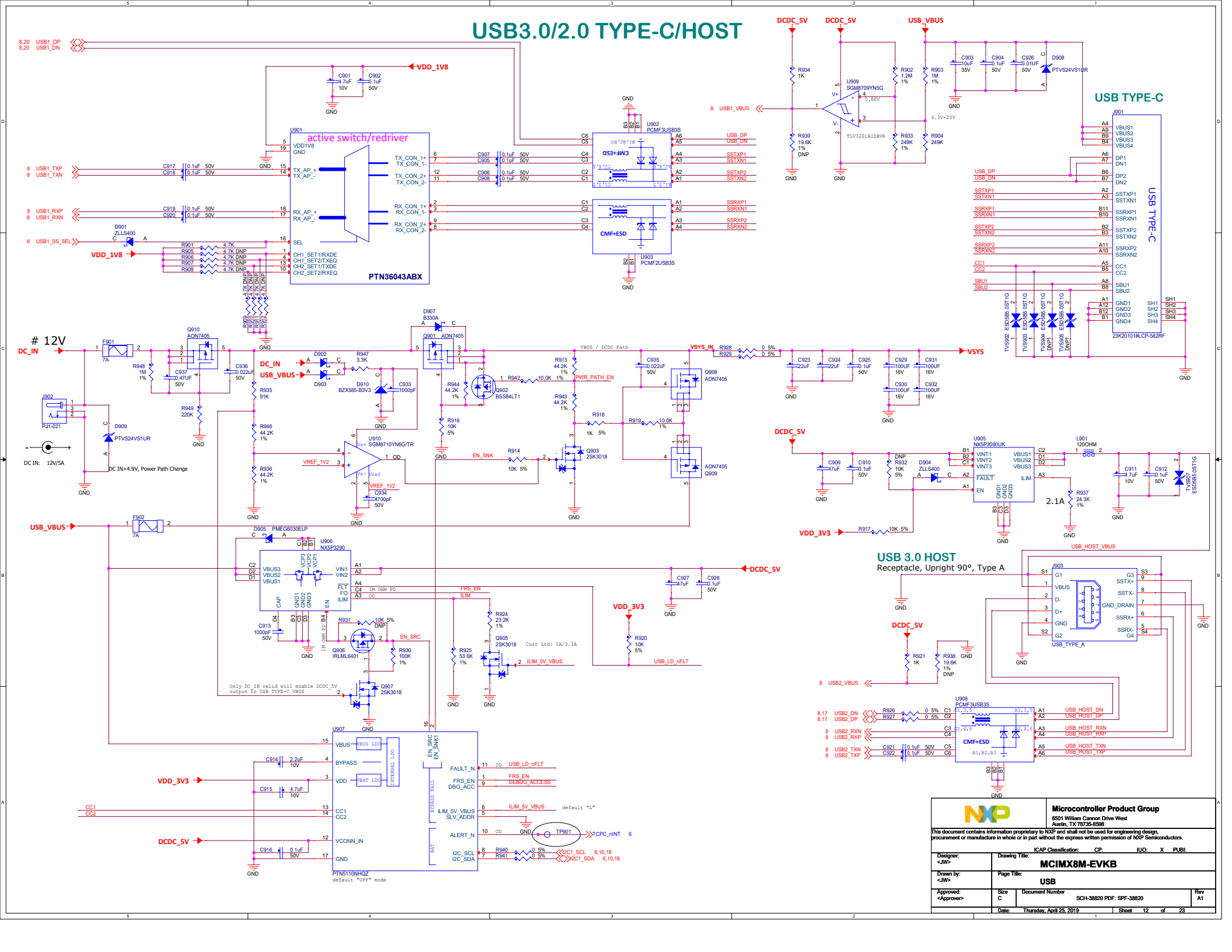
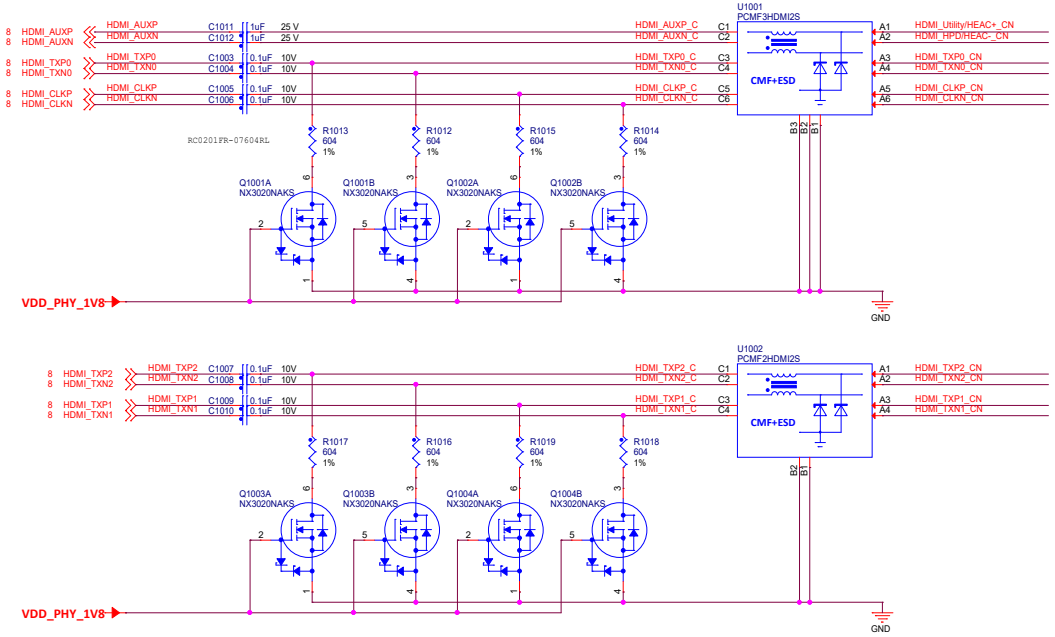
| | | | |
|---|---|---|---|
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: BOOT_CFG | | |
| Approved: <Approver> | Size: C | Document Number: SCH-38820 PDF: SPF-38820 | Rev: A1 |
| | Date: Thursday, April 25, 2019 | Sheet 11 of 23 | |

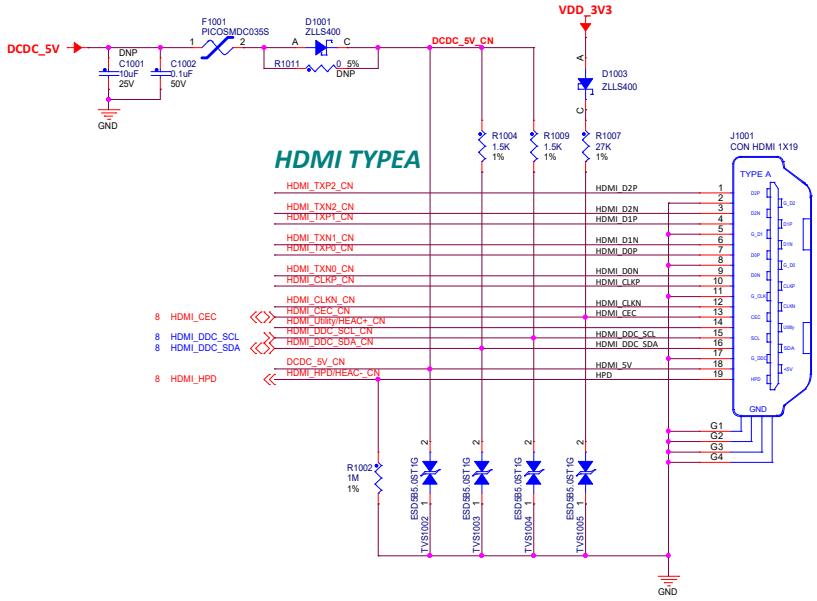
# USB3.0/2.0 TYPE-C/HOST



# HDMI 2.0a TX

## HDMI data EMI/ESD




| | |
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ICAP Classification: CP: IUO: X PUBI:

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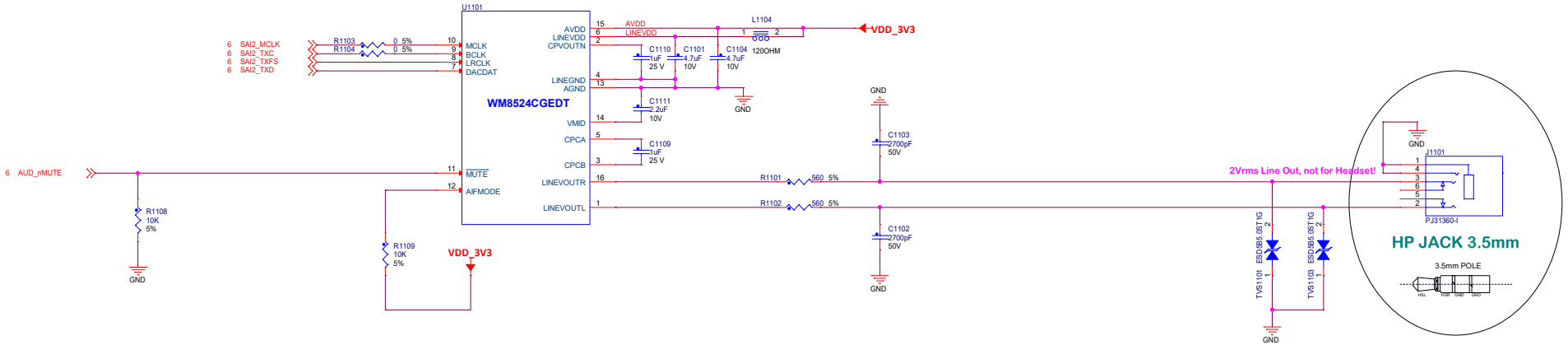
|---|---|---|---|
| Designer: <JW> | Drawing Title: **MCIMX8M-EVKB** | | |
| Drawn by: <JW> | Page Title: **HDMI** | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 13 of 23 | |

# Audio DAC

## 24-bit 192kHz Stereo DAC 2Vrms Line Out

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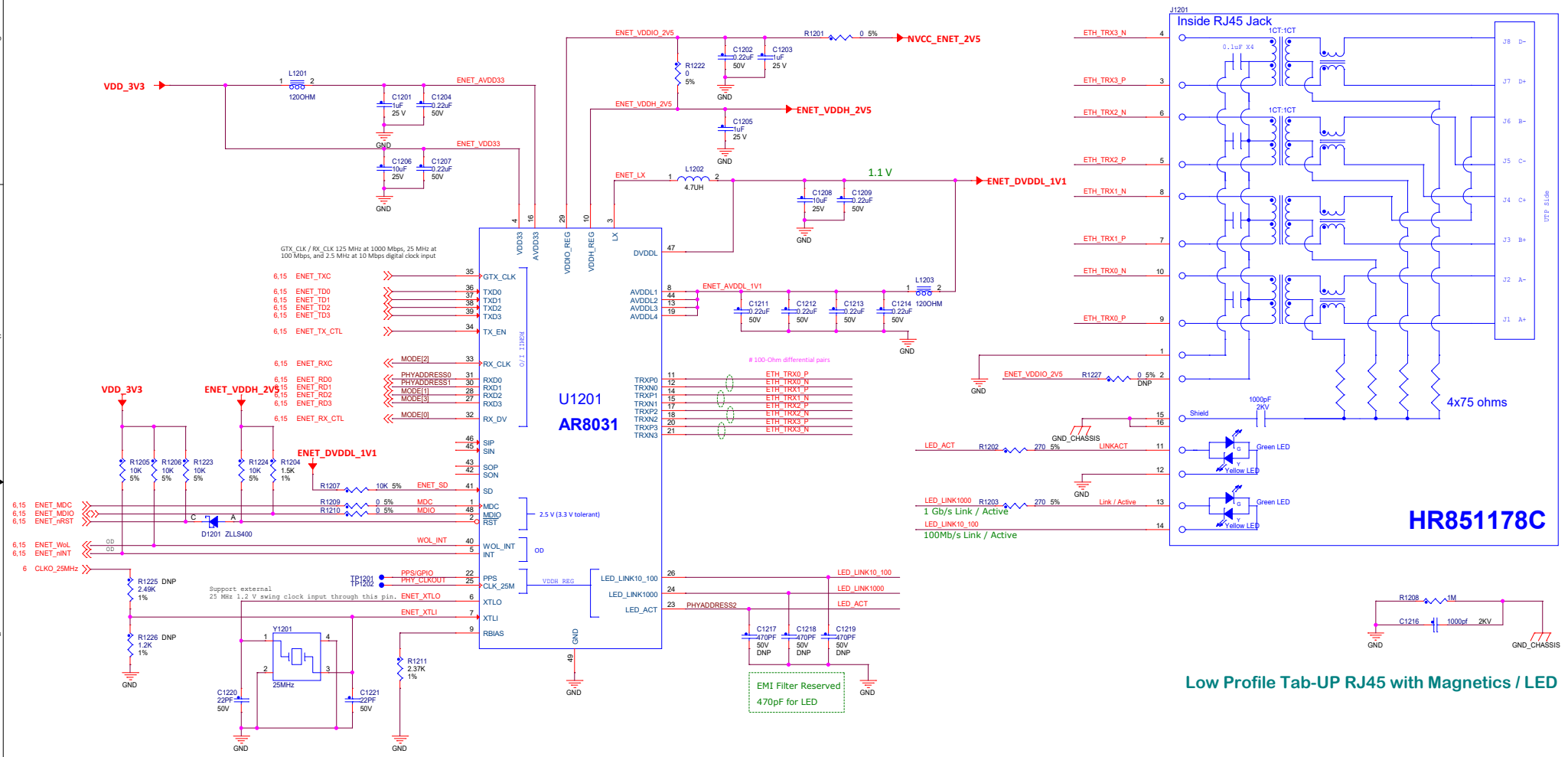
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | |
| Drawn by: <JW> | Page Title: CODEC | |
| Approved: <Approver> | Size C / Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 14 of 23 |

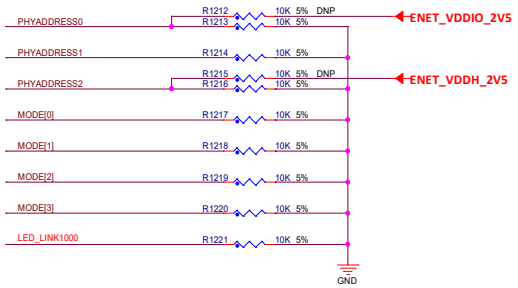
# RGMII 10/100/1000 Ethernet




## Power-on Strapping Pins

| PHY PIN | PHY CFG | Default | Definition |
|---|---|---|---|
| RXD0 | PHYADDRESS0 | 0 | LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00". |
| RXD1 | PHYADDRESS1 | 0 | |
| LED_ACT | PHYADDRESS2 | 1 | |
| RX_DV | MODE[0] | 0 | 0000 1000 Base-T, RGMII;<br>0001 1000 Base-T, SGMII;<br>0010 1000 Base-X, RGMII, 50Ω;<br>0011 1000 Base-X, RGMII, 75Ω;<br>0100 1000 Base-X/T, TRANS, 50Ω;<br>0101 1000 Base-X/T, TRANS, 75Ω;<br>0110 100 Base-FX, RGMII, 50Ω;<br>0111 100 Base-FX/TX, TRANS, 50Ω;<br>1011 RMII, copper fiber auto-detection;<br>1110 100 Base-FX, RGMII, 75Ω;<br>1111 100 Base-FX/TX, TRANS, 75Ω;<br>Others Reserved |
| RXD2 | MODE[1] | 0 | |
| RX_CLK | MODE[2] | 0 | |
| RXD3 | MODE[3] | 0 | |
| LED_LINK1000 | INT_SELECT | 1 | 0: INT ; 1:GPIO |

## Power-on Strapping Pins CFG





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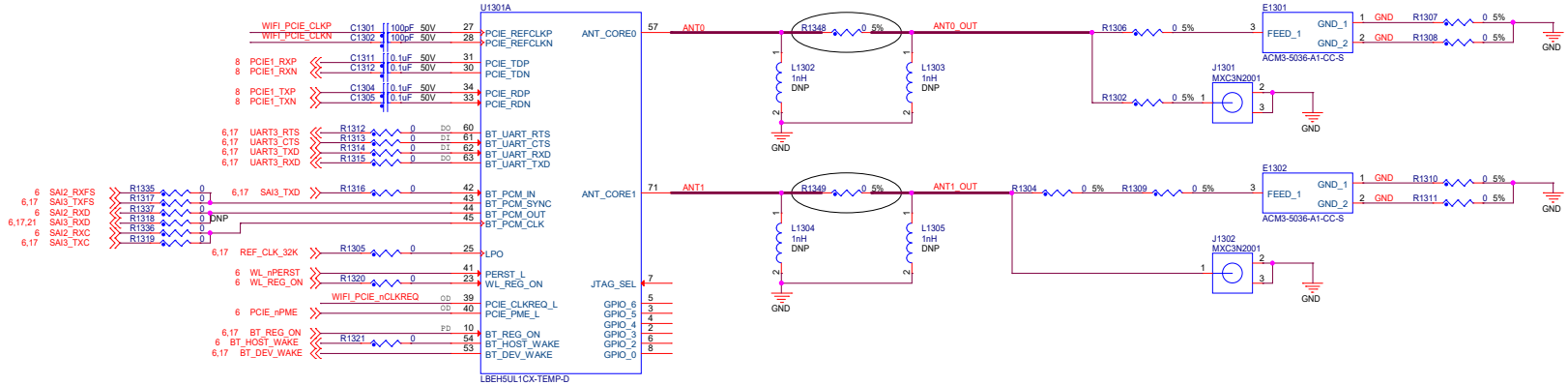
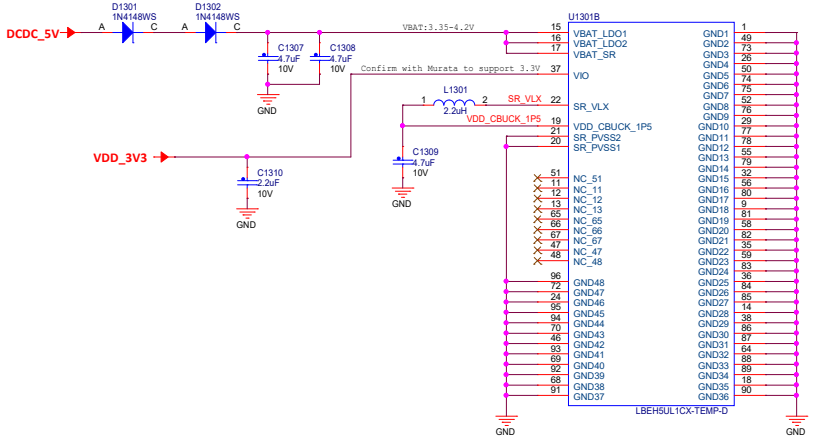
| | | | |
|---|---|---|---|
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: Ethernet | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 15 of 23 | |

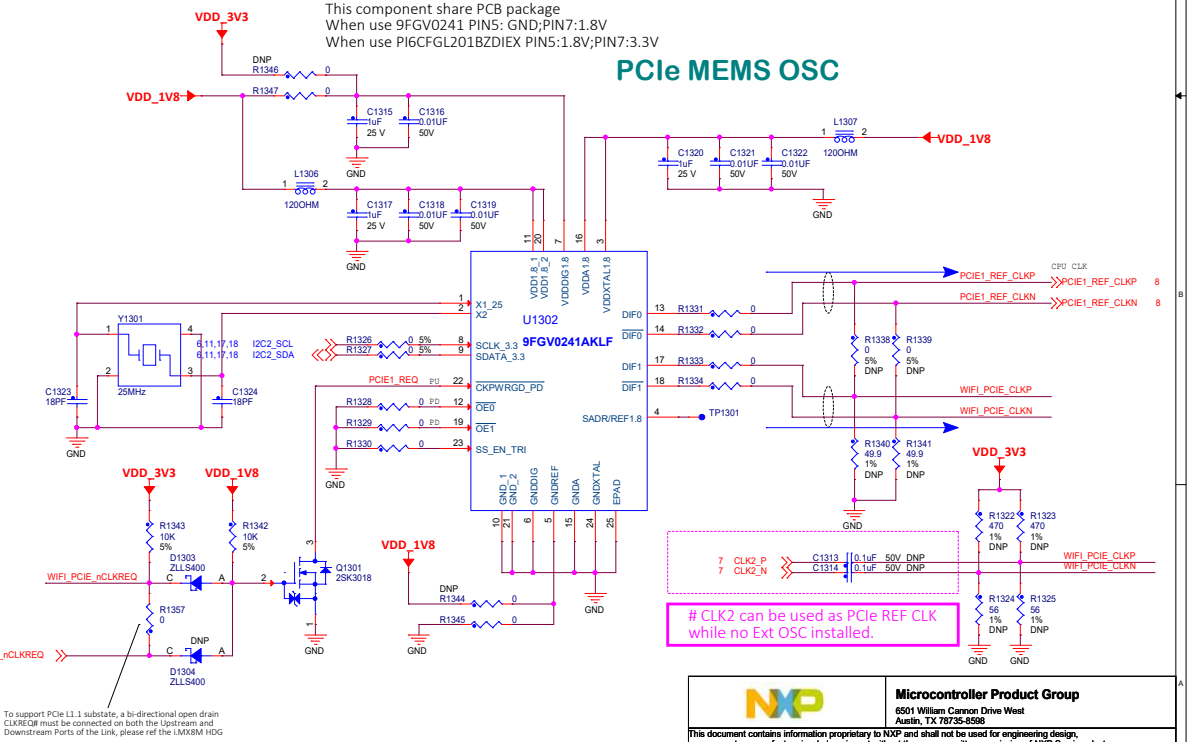
# WiFi/BT 802.11a/b/g/n/ac + Bluetooth 4.1/ EDR




NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

## PCIe MEMS OSC




To support PCIe L1.1 substate, a bi-directional open drain CLKREQ# must be connected on both the Upstream and Downstream Ports of the Link, please ref the LMX8M HDG

| | | |
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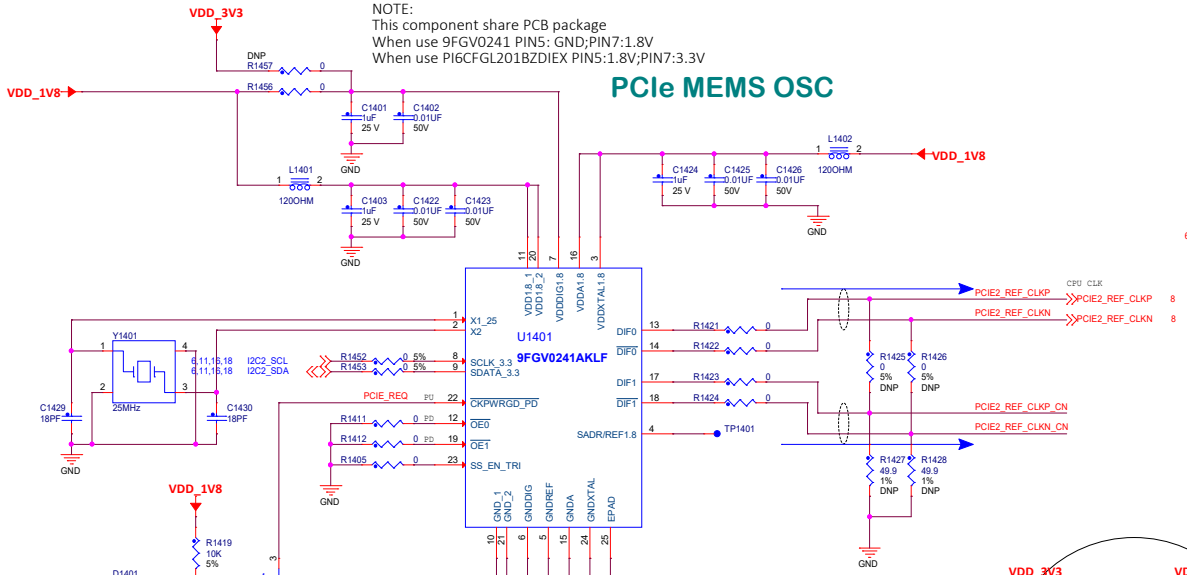
| | ICAP Classification: CP: IUO: X PUBI: | |
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | |
| Drawn by: <JW> | Page Title: WiFi/BT | |
| Approved: <Approver> | Size C / Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 16 of 23 |

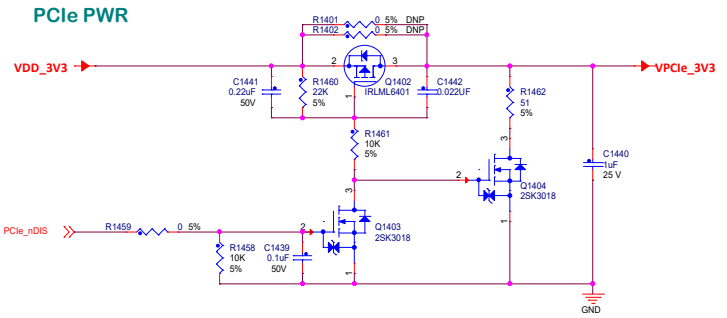
# PCIe M.2/NGFF

NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

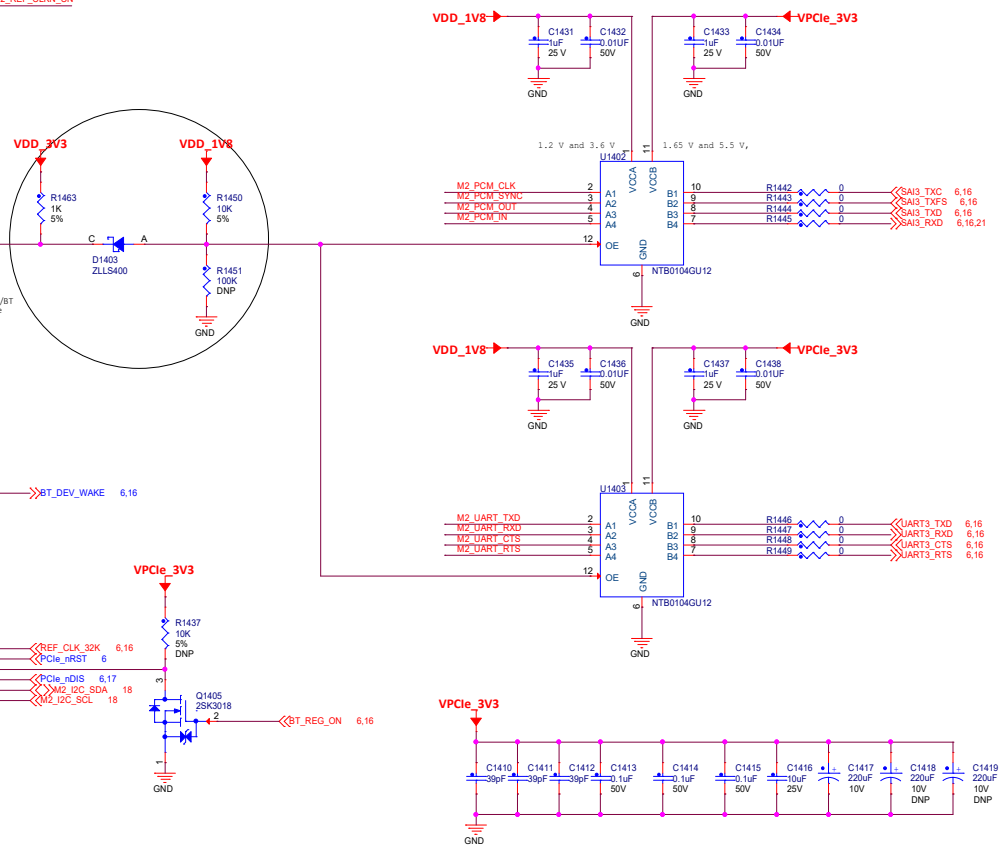
## PCIe MEMS OSC



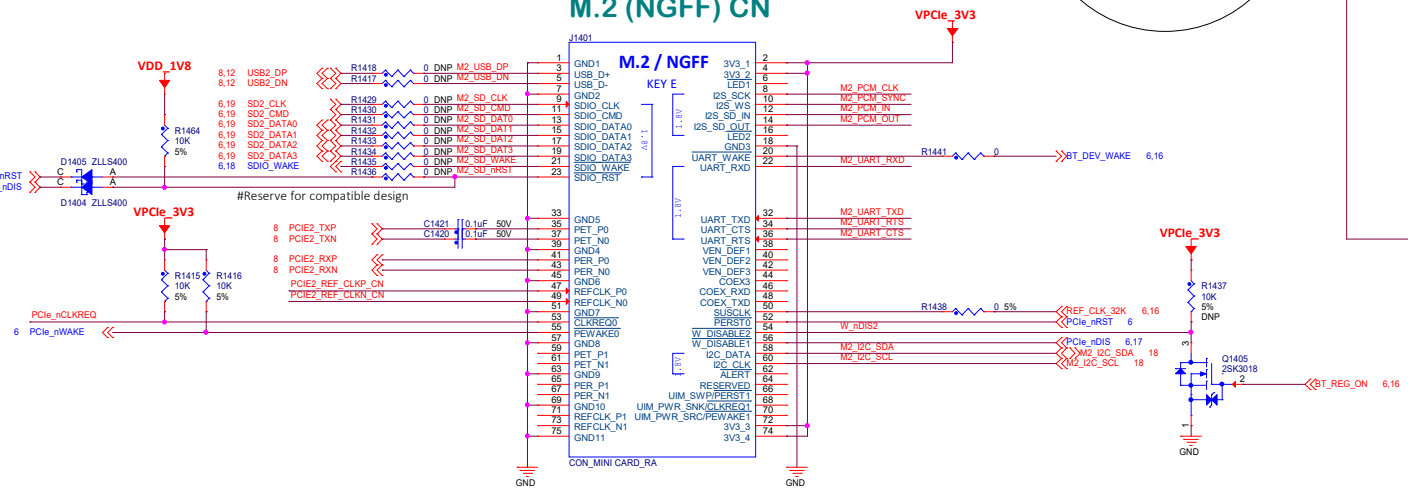

## PCIe PWR




## 3.3V->1.8V Level Shifter




## M.2 (NGFF) CN







DNP BH1401 .635" LONG
DNP BH1402 .635" LONG
DNP BH1403 .635" LONG
DNP BH1404 .635" LONG
DNP BH1405 SMTSO-M1.6-2.25ET
BH1406 SMTSO-M25
# Standoff for M.2
TP1402 TP1403 TP1404 TP1405 TP1406 TP1407



| | | | |
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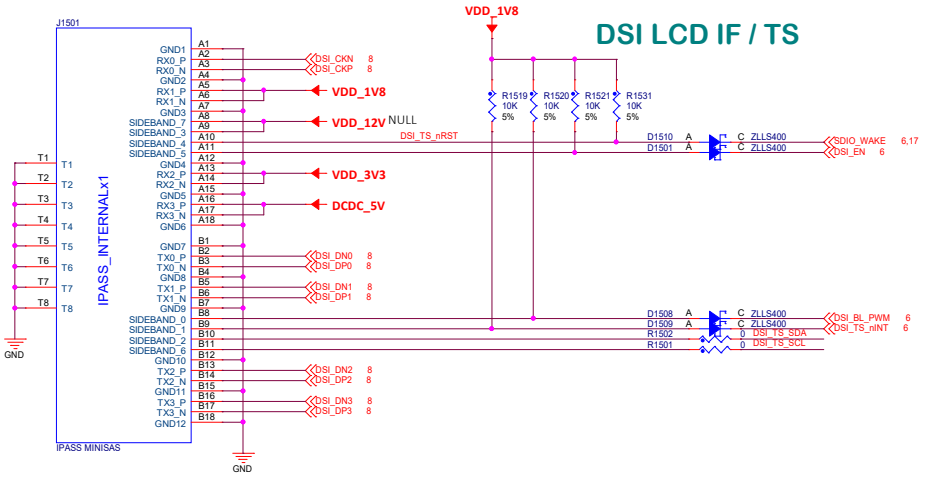
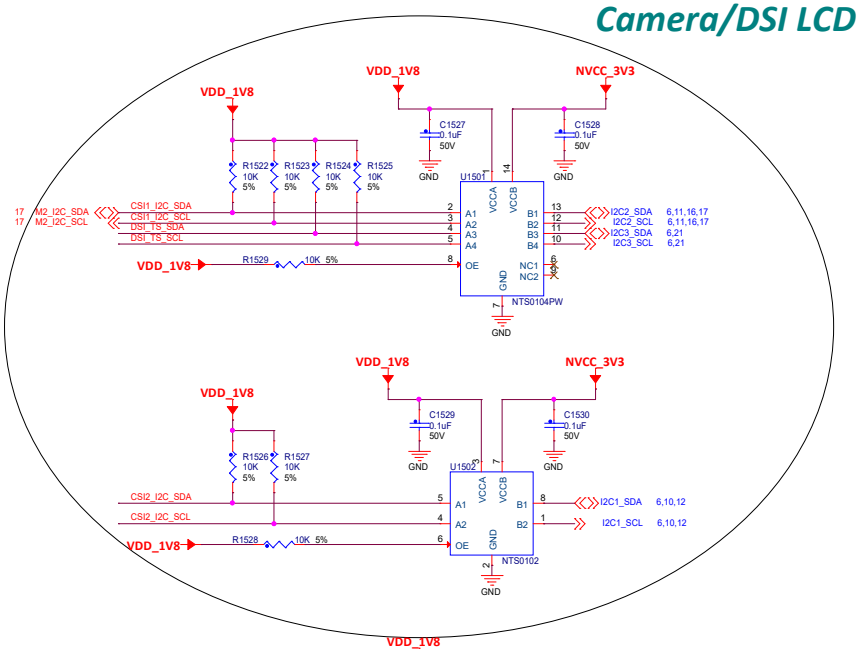
| ICAP Classification: | CP: | IUO: X | PUBI: |
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: mini-PCIe | | |
| Approved: <Approver> | Size: C | Document Number: SCH-38820 PDF: SPF-38820 | Rev: A1 |
| | Date: Thursday, April 25, 2019 | Sheet 17 of 23 | |

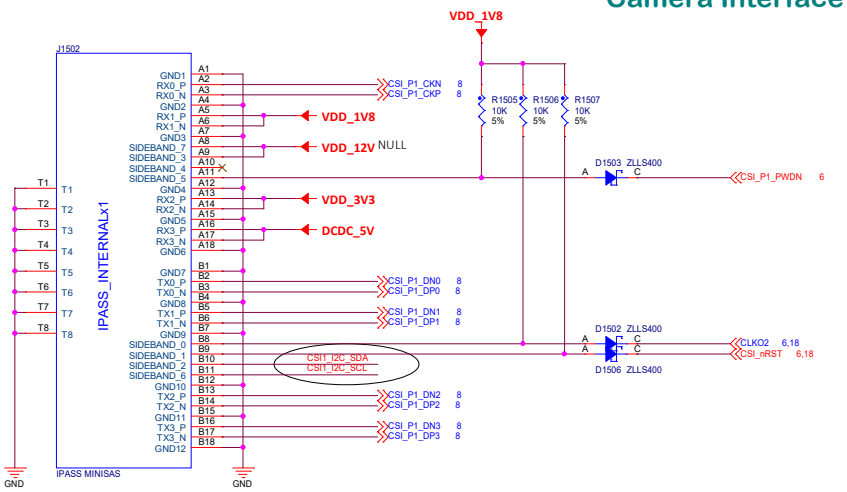
# Camera/DSI LCD

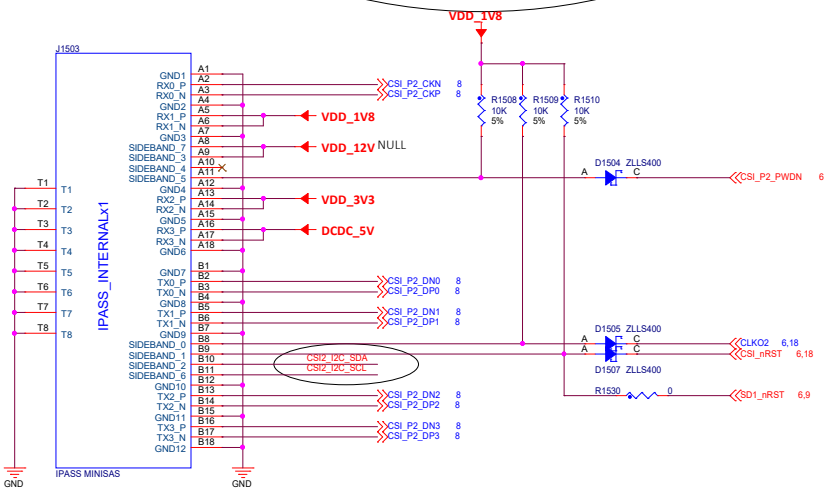
## DSI LCD IF / TS



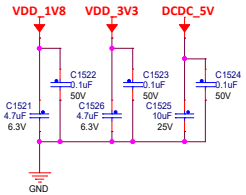



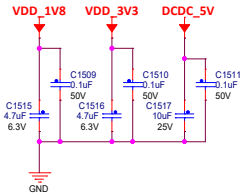

## Camera Interface

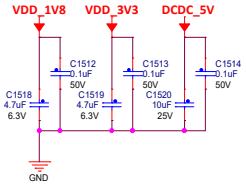



# NOTE: If Dual Camera worked at the same time with the same sensor, I2C need to be different port to aviode I2C ADDR conflict !!!






| | |
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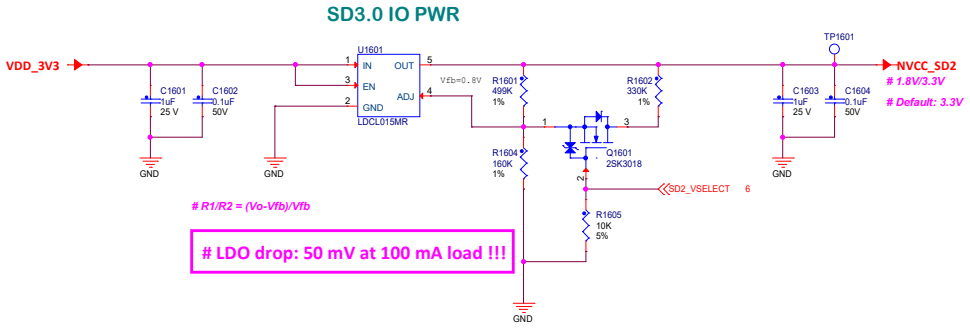
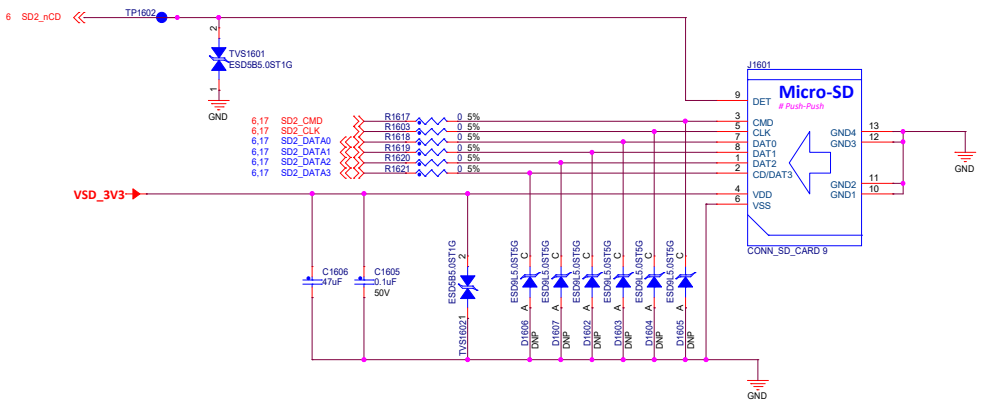
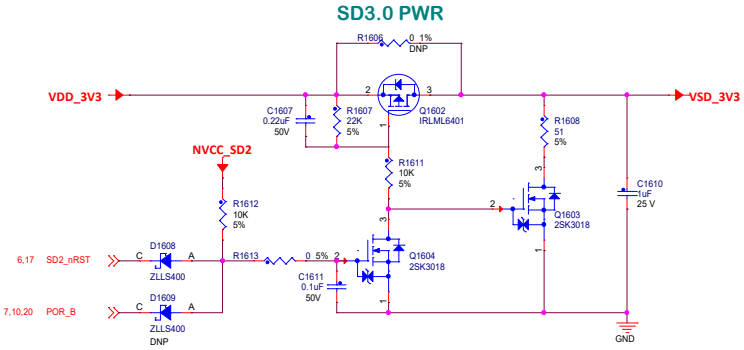
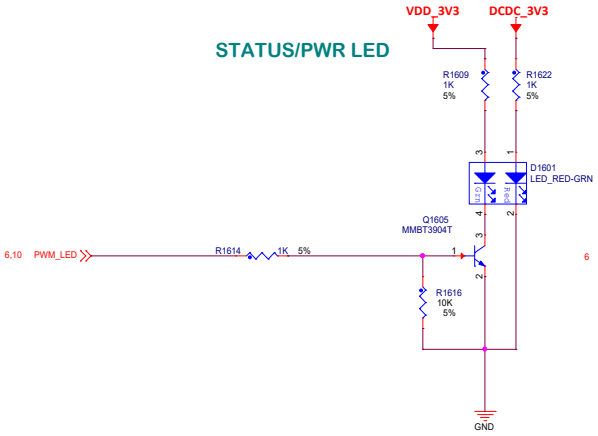
| Microcontroller Product Group | 6501 William Cannon Drive West, Austin, TX 78735-8598 |
| ICAP Classification: | CP: IUO: X PUBI: |
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB |
| Drawn by: <JW> | Page Title: MIPI/DSI/CSI |
| Approved: <Approver> | Size: C; Document Number: SCH-38820 PDF: SPF-38820; Rev: A1 |
| | Date: Thursday, April 25, 2019; Sheet 18 of 23 |

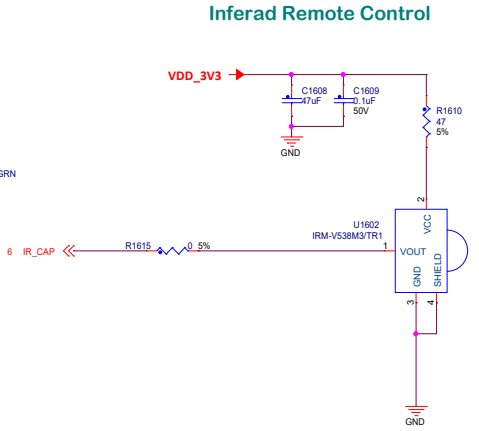
# MicroSD/Infrared/LED

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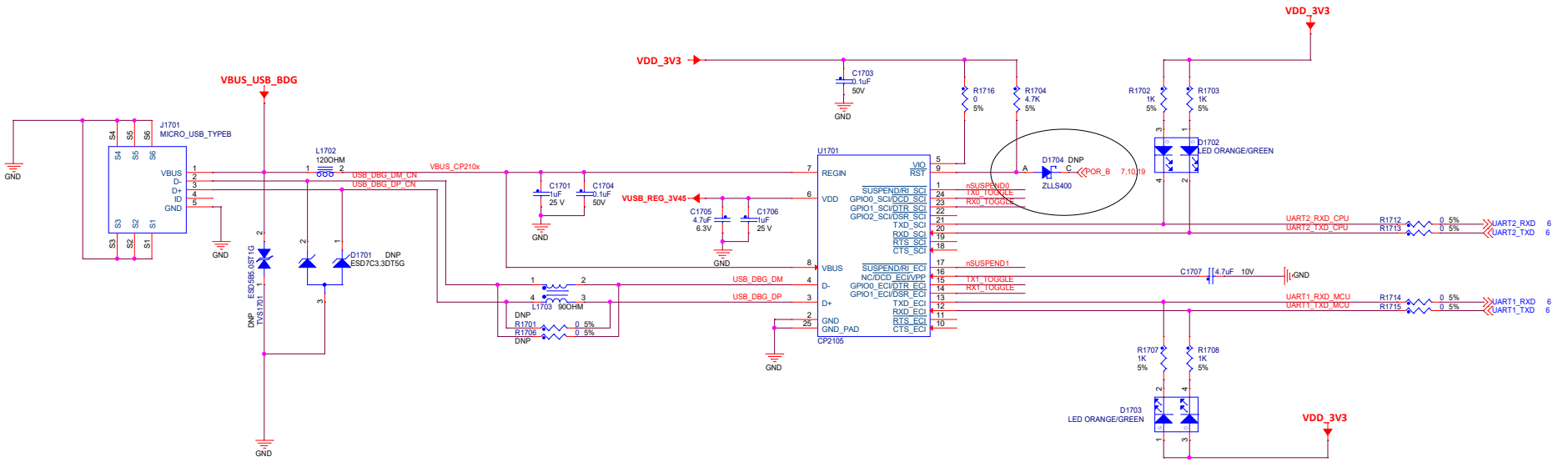
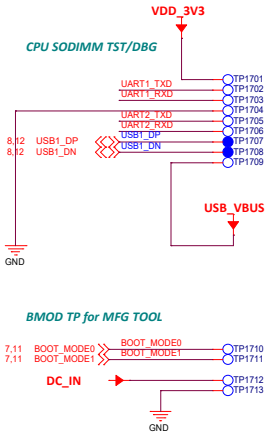
ICAP Classification: CP: IUO: X PUBI:

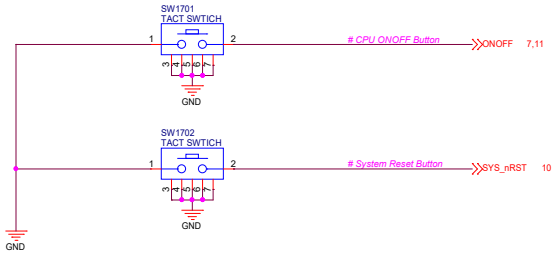
| | | | |
|---|---|---|---|
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | | |
| Drawn by: <JW> | Page Title: SD/IR/LED/BTN | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 19 of 23 | |

# UART-USB DBG




## TP for on-line MFG

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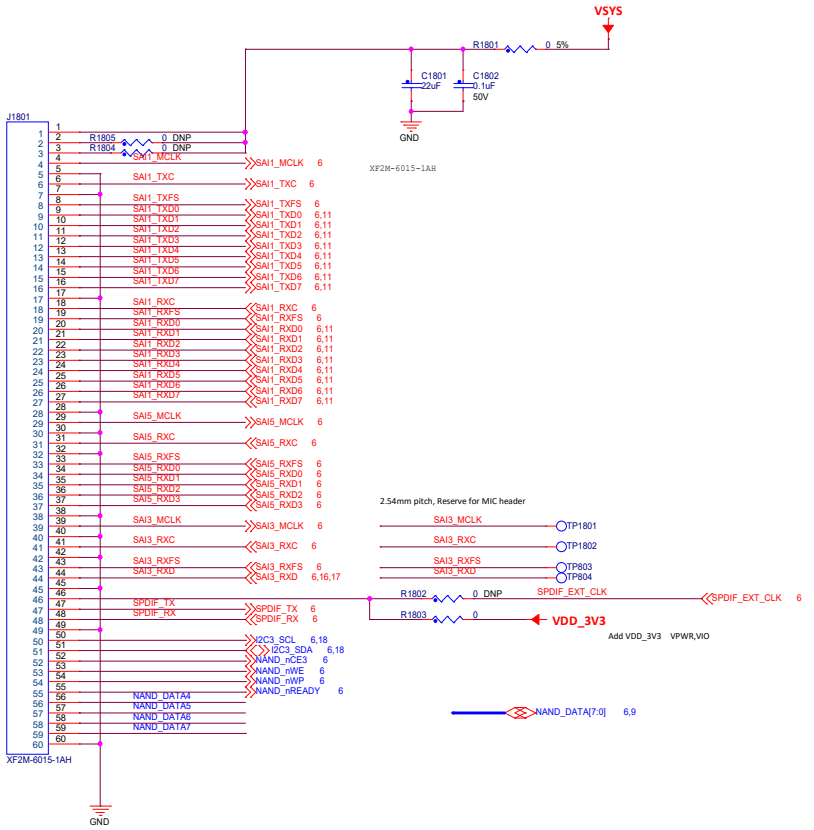
| ICAP Classification: CP: IUO: X PUBI: | | |
| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | |
| Drawn by: <JW> | Page Title: Debug UART | |
| Approved: <Approver> | Size C / Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 20 of 23 |

# EXP CN

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|---|---|---|
| | **Microcontroller Product Group** | |
| | 6501 William Cannon Drive West<br>Austin, TX 78735-8598 | |



ICAP Classification: CP: IUO: X PUBI:

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|---|---|---|---|
| Designer: <JW> | Drawing Title: **MCIMX8M-EVKB** | | |
| Drawn by: <JW> | Page Title: **Expansion CN** | | |
| Approved: <Approver> | Size C | Document Number SCH-38820 PDF: SPF-38820 | Rev A1 |
| | Date: Thursday, April 25, 2019 | Sheet 21 of 23 | |

# NOTE:

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6501 William Cannon Drive West
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| Designer: <JW> | Drawing Title: MCIMX8M-EVKB | |
| Drawn by: <JW> | Page Title: NOTE | |
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| | Date: Thursday, April 25, 2019 | Sheet 22 of 23 |

# i.MX8M IOMUX

| NAME | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | Alt6 Special EN | ALT7 | Alt7 Special EN |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TEST_MODE | tcu.TEST_MODE | tcu.TEST_MODE | | | | | | | | | |
| BOOT_MODE0 | ccmsrcgpcmix.BOOT_MODE[0] | ccmsrcgpcmix.BOOT_MODE[0] | | | | | | | | | |
| BOOT_MODE1 | ccmsrcgpcmix.BOOT_MODE[1] | ccmsrcgpcmix.BOOT_MODE[1] | | | | | | | | | |
| JTAG_MOD | cjtag_wrapper.MOD | cjtag_wrapper.MODE | | | | | | | | | |
| JTAG_TRST_B | cjtag_wrapper.TRST_B | cjtag_wrapper.TRST_B | | | | | | | | | |
| JTAG_TDI | cjtag_wrapper.TDI | cjtag_wrapper.TDI | | | | | | | | | |
| JTAG_TMS | cjtag_wrapper.TMS | cjtag_wrapper.TMS | | | | | | | | | |
| JTAG_TCK | cjtag_wrapper.TCK | cjtag_wrapper.TCK | | | | | | | | | |
| JTAG_TDO | cjtag_wrapper.TDO | cjtag_wrapper.TDO | | | | | | | | | |
| RTC | snvsmix.RTC | snvsmix.RTC | | | | | | | | | |
| PMIC_STBY_REQ | ccmsrcgpcmix.PMIC_STBY_REQ | ccmsrcgpcmix.PMIC_STBY_REQ | | | | | | | | | |
| PMIC_ON_REQ | snvsmix.PMIC_ON_REQ | snvsmix.PMIC_ON_REQ | | | | | | | | | |
| ONOFF | snvsmix.ONOFF | snvsmix.ONOFF | | | | | | | | | |
| POR_B | snvsmix.POR_B | snvsmix.POR_B | | | | | | | | | |
| RTC_RESET_B | snvsmix.RTC_POR_B | snvsmix.RTC_RESET_B | | | | | | | | | |
| GPIO1_IO00 | gpio1.IO[0] | gpio1.IO[0] | ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT | | | | anamix.REF_CLK_32K | ccmsrcgpcmix.EXT_CLK1 | | sjc.FAIL | |
| GPIO1_IO01 | gpio1.IO[1] | gpio1.IO[1] | pwm1.OUT | | | | anamix.REF_CLK_24M | ccmsrcgpcmix.EXT_CLK2 | | sjc.ACTIVE | ccmsrcgpcmix.src_system_rst |
| GPIO1_IO02 | gpio1.IO[2] | gpio1.IO[2] | wdog1.WDOG_B | | | | wdog1.WDOG_ANY | | | sjc.DE_B | sjc.sjc_gpucr1_reg[30] |
| GPIO1_IO03 | gpio1.IO[3] | gpio1.IO[3] | usdhc1.VSELECT | | | | sdma1.EXT_EVENT[0] | anamix.xtal_ok | | sjc.DONE | |
| GPIO1_IO04 | gpio1.IO[4] | gpio1.IO[4] | usdhc2.VSELECT | | | | sdma1.EXT_EVENT[1] | anamix.xtal_ok_iv | | usdhc1.TEST_TRIG | |
| GPIO1_IO05 | gpio1.IO[5] | gpio1.IO[5] | m4.NMI | | | | ccmsrcgpcmix.PMIC_READY | ccmsrcgpcmix.INT_BOOT | ccmsrcgpcmix.src_system_rst | usdhc2.TEST_TRIG | |
| GPIO1_IO06 | gpio1.IO[6] | gpio1.IO[6] | enet1.MDC | | | | usdhc1.CD_B | ccmsrcgpcmix.EXT_CLK3 | | ecspi1.TEST_TRIG | |
| GPIO1_IO07 | gpio1.IO[7] | gpio1.IO[7] | enet1.MDIO | | | | usdhc1.WP | ccmsrcgpcmix.EXT_CLK4 | | ecspi2.TEST_TRIG | |
| GPIO1_IO08 | gpio1.IO[8] | gpio1.IO[8] | enet1.1588_EVENT0_IN | | | | usdhc2.RESET_B | ccmsrcgpcmix.WAIT | | qspi.TEST_TRIG | |
| GPIO1_IO09 | gpio1.IO[9] | gpio1.IO[9] | enet1.1588_EVENT0_OUT | | | | sdma2.EXT_EVENT[0] | ccmsrcgpcmix.STOP | | rawnand.TEST_TRIG | |
| GPIO1_IO10 | gpio1.IO[10] | gpio1.IO[10] | usb1.OTG_ID | | | | | | | ocotp_ctrl_wrapper.FUSE_LATCHED | sjc.sjc_gpucr3_reg[14] |
| GPIO1_IO11 | gpio1.IO[11] | gpio1.IO[11] | usb2.OTG_ID | | | | ccmsrcgpcmix.PMIC_READY | | | caam_wrapper.RNG_OSC_OBS | |
| GPIO1_IO12 | gpio1.IO[12] | gpio1.IO[12] | usb1.OTG_PWR | | | | sdma2.EXT_EVENT[1] | ccmsrcgpcmix.OUT0 | | csu.CSU_ALARM_AUT[0] | |
| GPIO1_IO13 | gpio1.IO[13] | gpio1.IO[13] | usb1.OTG_OC | | | | pwm2.OUT | ccmsrcgpcmix.OUT1 | | csu.CSU_ALARM_AUT[1] | |
| GPIO1_IO14 | gpio1.IO[14] | gpio1.IO[14] | usb2.OTG_PWR | | | | pwm3.OUT | ccmsrcgpcmix.OUT2 | | csu.CSU_ALARM_AUT[2] | |
| GPIO1_IO15 | gpio1.IO[15] | gpio1.IO[15] | usb2.OTG_OC | | | | pwm4.OUT | ccmsrcgpcmix.CLKO1 | | csu.CSU_INT_DEB | |
| ENET_MDC | enet1.MDC | enet1.MDC | | | | | gpio1.IO[16] | ccmsrcgpcmix.CLKO2 | | | |
| ENET_MDIO | enet1.MDIO | enet1.MDIO | | | | | gpio1.IO[17] | | | | |
| ENET_TD3 | enet1.RGMII_TD3 | enet1.RGMII_TD3 | | | | | gpio1.IO[18] | | | | |
| ENET_TD2 | enet1.RGMII_TD2 | enet1.RGMII_TD2 | "INPUT=enet1.TX_CLK | | | | gpio1.IO[19] | | | | |
| ENET_TD1 | enet1.RGMII_TD1 | enet1.RGMII_TD1 | OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT" | | | | gpio1.IO[20] | | | | |
| ENET_TD0 | enet1.RGMII_TD0 | enet1.RGMII_TD0 | | | | | gpio1.IO[21] | | | | |
| ENET_TX_CTL | enet1.RGMII_TX_CTL | enet1.RGMII_TX_CTL | | | | | gpio1.IO[22] | | | | |
| ENET_TXC | enet1.RGMII_TXC | enet1.RGMII_TXC | | | | | gpio1.IO[23] | | | | |
| ENET_RX_CTL | enet1.RGMII_RX_CTL | enet1.RGMII_RX_CTL | enet1.TX_ER | | | | gpio1.IO[24] | | | | |
| ENET_RXC | enet1.RGMII_RXC | enet1.RGMII_RXC | | | | | gpio1.IO[25] | | | | |
| ENET_RD0 | enet1.RGMII_RD0 | enet1.RGMII_RD0 | enet1.RX_ER | | | | gpio1.IO[26] | | | | |
| ENET_RD1 | enet1.RGMII_RD1 | enet1.RGMII_RD1 | | | | | gpio1.IO[27] | | | | |
| ENET_RD2 | enet1.RGMII_RD2 | enet1.RGMII_RD2 | | | | | gpio1.IO[28] | | | | |
| ENET_RD3 | enet1.RGMII_RD3 | enet1.RGMII_RD3 | | | | | gpio1.IO[29] | | | | |
| SD1_CLK | usdhc1.CLK | usdhc1.CLK | | | | | gpio2.IO[0] | | | | |
| SD1_CMD | usdhc1.CMD | usdhc1.CMD | | | | | gpio2.IO[1] | | | | |
| SD1_DATA0 | usdhc1.DATA0 | usdhc1.DATA0 | | | | | gpio2.IO[2] | | | | |
| SD1_DATA1 | usdhc1.DATA1 | usdhc1.DATA1 | | | | | gpio2.IO[3] | | | | |
| SD1_DATA2 | usdhc1.DATA2 | usdhc1.DATA2 | | | | | gpio2.IO[4] | | | | |
| SD1_DATA3 | usdhc1.DATA3 | usdhc1.DATA3 | | | | | gpio2.IO[5] | | | | |
| SD1_DATA4 | usdhc1.DATA4 | usdhc1.DATA4 | | | | | gpio2.IO[6] | | | | |
| SD1_DATA5 | usdhc1.DATA5 | usdhc1.DATA5 | | | | | gpio2.IO[7] | | | | |
| SD1_DATA6 | usdhc1.DATA6 | usdhc1.DATA6 | | | | | gpio2.IO[8] | | | | |
| SD1_DATA7 | usdhc1.DATA7 | usdhc1.DATA7 | | | | | gpio2.IO[9] | | | | |
| SD1_RESET_B | usdhc1.RESET_B | usdhc1.RESET_B | | | | | gpio2.IO[10] | | | | |
| SD1_STROBE | usdhc1.STROBE | usdhc1.STROBE | | | | | gpio2.IO[11] | | | | |
| SD2_CD_B | usdhc2.CD_B | usdhc2.CD_B | | | | | gpio2.IO[12] | | | | |
| SD2_CLK | usdhc2.CLK | usdhc2.CLK | | | | | gpio2.IO[13] | ccmsrcgpcmix.OBSERVE0 | | observe_mux.OUT[0] | |
| SD2_CMD | usdhc2.CMD | usdhc2.CMD | | | | | gpio2.IO[14] | ccmsrcgpcmix.OBSERVE1 | | observe_mux.OUT[1] | |
| SD2_DATA0 | usdhc2.DATA0 | usdhc2.DATA0 | | | | | gpio2.IO[15] | ccmsrcgpcmix.OBSERVE2 | | observe_mux.OUT[2] | |
| SD2_DATA1 | usdhc2.DATA1 | usdhc2.DATA1 | | | | | gpio2.IO[16] | ccmsrcgpcmix.WAIT | | observe_mux.OUT[3] | |
| SD2_DATA2 | usdhc2.DATA2 | usdhc2.DATA2 | | | | | gpio2.IO[17] | ccmsrcgpcmix.STOP | | observe_mux.OUT[4] | |
| SD2_DATA3 | usdhc2.DATA3 | usdhc2.DATA3 | | | | | gpio2.IO[18] | ccmsrcgpcmix.EARLY_RESET | sjc.sjc_gpucr3_reg[14] | | |
| SD2_RESET_B | usdhc2.RESET_B | usdhc2.RESET_B | | | | | gpio2.IO[19] | ccmsrcgpcmix.SYSTEM_RESET | sjc.sjc_gpucr3_reg[14] | | |
| SD2_WP | usdhc2.WP | usdhc2.WP | | | | | gpio2.IO[20] | | | sim_m.HMASTLOCK | sjc.sjc_gpucr1_reg[11] |
| NAND_ALE | rawnand.ALE | rawnand.ALE | | | | | gpio3.IO[0] | | | sim_m.HPROT[0] | sjc.sjc_gpucr1_reg[11] |
| NAND_CE0_B | rawnand.CE0_B | rawnand.CE0_B | qspi.A_SCLK | | | | gpio3.IO[1] | | | sim_m.HPROT[1] | sjc.sjc_gpucr1_reg[11] |
| NAND_CE1_B | rawnand.CE1_B | rawnand.CE1_B | qspi.A_SS0_B | | | | gpio3.IO[2] | | | sim_m.HPROT[2] | sjc.sjc_gpucr1_reg[11] |
| NAND_CE2_B | rawnand.CE2_B | rawnand.CE2_B | qspi.A_SS1_B | | | | gpio3.IO[3] | | | sim_m.HPROT[3] | sjc.sjc_gpucr1_reg[11] |
| NAND_CE3_B | rawnand.CE3_B | rawnand.CE3_B | qspi.B_SS0_B | | | | gpio3.IO[4] | | | sim_m.HADDR[0] | sjc.sjc_gpucr1_reg[11] |
| NAND_CLE | rawnand.CLE | rawnand.CLE | qspi.B_SS1_B | | | | gpio3.IO[5] | | | sim_m.HADDR[1] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA00 | rawnand.DATA00 | rawnand.DATA00 | qspi.B_SCLK | | | | gpio3.IO[6] | | | sim_m.HADDR[2] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA01 | rawnand.DATA01 | rawnand.DATA01 | qspi.A_DATA[0] | | | | gpio3.IO[7] | | | sim_m.HADDR[3] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA02 | rawnand.DATA02 | rawnand.DATA02 | qspi.A_DATA[1] | | | | gpio3.IO[8] | | | sim_m.HADDR[4] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA03 | rawnand.DATA03 | rawnand.DATA03 | qspi.A_DATA[2] | | | | gpio3.IO[9] | | | sim_m.HADDR[5] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA04 | rawnand.DATA04 | rawnand.DATA04 | qspi.A_DATA[3] | | | | gpio3.IO[10] | | | sim_m.HADDR[6] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA05 | rawnand.DATA05 | rawnand.DATA05 | qspi.B_DATA[0] | | | | gpio3.IO[11] | | | sim_m.HADDR[7] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA06 | rawnand.DATA06 | rawnand.DATA06 | qspi.B_DATA[1] | | | | gpio3.IO[12] | | | sim_m.HADDR[8] | sjc.sjc_gpucr1_reg[11] |
| NAND_DATA07 | rawnand.DATA07 | rawnand.DATA07 | qspi.B_DATA[2] | | | | gpio3.IO[13] | | | sim_m.HADDR[9] | sjc.sjc_gpucr1_reg[11] |
| NAND_DQS | rawnand.DQS | rawnand.DQS | qspi.B_DATA[3] | | | | gpio3.IO[14] | | | sim_m.HADDR[10] | sjc.sjc_gpucr1_reg[11] |
| NAND_RE_B | rawnand.RE_B | rawnand.RE_B | qspi.A_DQS | | | | gpio3.IO[15] | | | sim_m.HADDR[11] | sjc.sjc_gpucr1_reg[11] |
| NAND_READY_B | rawnand.READY_B | rawnand.READY_B | qspi.B_DQS | | | | gpio3.IO[16] | | | sim_m.HADDR[12] | sjc.sjc_gpucr1_reg[11] |
| NAND_WE_B | rawnand.WE_B | rawnand.WE_B | | | | | gpio3.IO[17] | | | sim_m.HADDR[13] | sjc.sjc_gpucr1_reg[11] |
| NAND_WP_B | rawnand.WP_B | rawnand.WP_B | | | | | gpio3.IO[18] | | | sim_m.HADDR[14] | sjc.sjc_gpucr1_reg[11] |
| SAI5_RXFS | sai5.RX_SYNC | sai5.RX_SYNC | | | | | gpio3.IO[19] | | | | |
| SAI5_RXC | sai5.RX_BCLK | sai5.RX_BCLK | sai1.TX_DATA[0] | | | | gpio3.IO[20] | | | | |
| SAI5_RXD0 | sai5.RX_DATA[0] | sai5.RX_DATA[0] | sai1.TX_DATA[1] | | | | gpio3.IO[21] | | | | |
| SAI5_RXD1 | sai5.RX_DATA[1] | sai5.RX_DATA[1] | sai1.TX_DATA[2] | sai1.TX_SYNC | sai5.TX_SYNC | | gpio3.IO[22] | | | | |
| SAI5_RXD2 | sai5.RX_DATA[2] | sai5.RX_DATA[2] | sai1.TX_DATA[3] | sai1.TX_BCLK | sai5.TX_BCLK | | gpio3.IO[23] | | | | |
| SAI5_RXD3 | sai5.RX_DATA[3] | sai5.RX_DATA[3] | sai1.TX_DATA[4] | sai1.TX_SYNC | sai5.TX_DATA[0] | | gpio3.IO[24] | | | | |
| SAI5_MCLK | sai5.MCLK | sai5.MCLK | sai1.TX_DATA[5] | sai4.MCLK | | | gpio3.IO[25] | ccmsrcgpcmix.TESTER_ACK | ~ccmsrcgpcmix.src_en_system_clk | | |
| SAI1_RXFS | sai1.RX_SYNC | sai1.RX_SYNC | sai1.TX_BCLK | | | coresight.TRACE_CLK | gpio4.IO[0] | | | sim_m.HADDR[15] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXC | sai1.RX_BCLK | sai1.RX_BCLK | sai5.RX_SYNC | | | coresight.TRACE_CTL | gpio4.IO[1] | | | sim_m.HADDR[16] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD0 | sai1.RX_DATA[0] | sai1.RX_DATA[0] | sai5.RX_BCLK | | | coresight.TRACE[0] | gpio4.IO[2] | ccmsrcgpcmix.BOOT_CFG[0] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[17] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD1 | sai1.RX_DATA[1] | sai1.RX_DATA[1] | sai5.RX_DATA[0] | | | coresight.TRACE[1] | gpio4.IO[3] | ccmsrcgpcmix.BOOT_CFG[1] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[18] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD2 | sai1.RX_DATA[2] | sai1.RX_DATA[2] | sai5.RX_DATA[1] | | | coresight.TRACE[2] | gpio4.IO[4] | ccmsrcgpcmix.BOOT_CFG[2] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[19] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD3 | sai1.RX_DATA[3] | sai1.RX_DATA[3] | sai5.RX_DATA[2] | | | coresight.TRACE[3] | gpio4.IO[5] | ccmsrcgpcmix.BOOT_CFG[3] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[20] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD4 | sai1.RX_DATA[4] | sai1.RX_DATA[4] | sai5.RX_DATA[3] | sai6.RX_BCLK | | coresight.TRACE[4] | gpio4.IO[6] | ccmsrcgpcmix.BOOT_CFG[4] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[21] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD5 | sai1.RX_DATA[5] | sai1.RX_DATA[5] | sai6.TX_BCLK | sai6.RX_DATA[0] | sai1.RX_SYNC | coresight.TRACE[5] | gpio4.IO[7] | ccmsrcgpcmix.BOOT_CFG[5] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[22] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD6 | sai1.RX_DATA[6] | sai1.RX_DATA[6] | sai6.RX_SYNC | sai6.RX_SYNC | | coresight.TRACE[6] | gpio4.IO[8] | ccmsrcgpcmix.BOOT_CFG[6] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[23] | sjc.sjc_gpucr1_reg[11] |
| SAI1_RXD7 | sai1.RX_DATA[7] | sai1.RX_DATA[7] | sai6.TX_SYNC | sai1.TX_DATA[4] | sai1.TX_DATA[7] | coresight.TRACE[7] | gpio4.IO[9] | ccmsrcgpcmix.BOOT_CFG[7] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[24] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXFS | sai1.TX_SYNC | sai6.MCLK | | | | coresight.EVENTO | gpio4.IO[10] | | | sim_m.HADDR[25] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXC | sai1.TX_BCLK | sai5.TX_SYNC | | | | coresight.EVENT1 | gpio4.IO[11] | | | sim_m.HADDR[26] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD0 | sai1.TX_DATA[0] | sai5.TX_BCLK | | | | coresight.TRACE[8] | gpio4.IO[12] | ccmsrcgpcmix.BOOT_CFG[8] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[27] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD1 | sai1.TX_DATA[1] | sai5.TX_DATA[0] | | | | coresight.TRACE[9] | gpio4.IO[13] | ccmsrcgpcmix.BOOT_CFG[9] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[28] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD2 | sai1.TX_DATA[2] | sai5.TX_DATA[1] | | | | coresight.TRACE[10] | gpio4.IO[14] | ccmsrcgpcmix.BOOT_CFG[10] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[29] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD3 | sai1.TX_DATA[3] | sai5.TX_DATA[2] | | | | coresight.TRACE[11] | gpio4.IO[15] | ccmsrcgpcmix.BOOT_CFG[11] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[30] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD4 | sai1.TX_DATA[4] | sai5.TX_DATA[3] | | sai6.TX_BCLK | | coresight.TRACE[12] | gpio4.IO[16] | ccmsrcgpcmix.BOOT_CFG[12] | ccmsrcgpcmix.src_system_rst | sim_m.HADDR[31] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD5 | sai1.TX_DATA[5] | sai6.RX_BCLK | | sai6.TX_DATA[0] | | coresight.TRACE[13] | gpio4.IO[17] | ccmsrcgpcmix.BOOT_CFG[13] | ccmsrcgpcmix.src_system_rst | sim_m.HBURST[0] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD6 | sai1.TX_DATA[6] | sai6.RX_DATA[0] | | sai6.TX_SYNC | | coresight.TRACE[14] | gpio4.IO[18] | ccmsrcgpcmix.BOOT_CFG[14] | ccmsrcgpcmix.src_system_rst | sim_m.HBURST[1] | sjc.sjc_gpucr1_reg[11] |
| SAI1_TXD7 | sai1.TX_DATA[7] | sai6.RX_SYNC | | | | coresight.TRACE[15] | gpio4.IO[19] | ccmsrcgpcmix.BOOT_CFG[15] | ccmsrcgpcmix.src_system_rst | sim_m.HBURST[2] | sjc.sjc_gpucr1_reg[11] |
| SAI1_MCLK | sai1.MCLK | sai6.MCLK | | sai1.TX_BCLK | | | gpio4.IO[20] | | | sim_m.HRESP | sjc.sjc_gpucr1_reg[11] |
| SAI2_RXFS | sai2.RX_SYNC | sai5.MCLK | | | | | gpio4.IO[21] | | | sim_m.HSIZE[0] | sjc.sjc_gpucr1_reg[11] |
| SAI2_RXC | sai2.RX_BCLK | sai5.TX_SYNC | | | | | gpio4.IO[22] | | | sim_m.HSIZE[1] | sjc.sjc_gpucr1_reg[11] |
| SAI2_RXD0 | sai2.RX_DATA[0] | sai5.TX_BCLK | | | | | gpio4.IO[23] | | | sim_m.HSIZE[2] | sjc.sjc_gpucr1_reg[11] |
| SAI2_TXFS | sai2.TX_SYNC | sai5.TX_DATA[0] | | | | | gpio4.IO[24] | | | sim_m.HWRITE | sjc.sjc_gpucr1_reg[11] |
| SAI2_TXC | sai2.TX_BCLK | sai5.TX_DATA[1] | | | | | gpio4.IO[25] | | | sim_m.HREADYOUT | sjc.sjc_gpucr1_reg[11] |
| SAI2_TXD0 | sai2.TX_DATA[0] | sai5.TX_DATA[2] | | | | | gpio4.IO[26] | | | tpsmp.CLK | sjc.sjc_gpucr1_reg[11] |
| SAI2_MCLK | sai2.MCLK | sai5.TX_DATA[3] | | | | | gpio4.IO[27] | | | tpsmp.HDATA_DIR | sjc.sjc_gpucr1_reg[11] |
| SAI3_RXFS | sai3.RX_SYNC | sai5.MCLK | | sai5.RX_SYNC | | | gpio4.IO[28] | | | tpsmp.HTRANS[0] | sjc.sjc_gpucr1_reg[11] |
| SAI3_RXC | sai3.RX_BCLK | gpt1.CAPTURE1 | | sai5.RX_BCLK | | | gpio4.IO[29] | | | tpsmp.HTRANS[1] | sjc.sjc_gpucr1_reg[11] |
| SAI3_RXD | sai3.RX_DATA[0] | gpt1.CAPTURE2 | | sai5.RX_DATA[0] | | | gpio4.IO[30] | | | tpsmp.HDATA[0] | sjc.sjc_gpucr1_reg[11] |
| SAI3_TXFS | sai3.TX_SYNC | gpt1.COMPARE1 | | sai5.RX_DATA[1] | | | gpio4.IO[31] | | | tpsmp.HDATA[1] | sjc.sjc_gpucr1_reg[11] |
| SAI3_TXC | sai3.TX_BCLK | gpt1.CLK | | sai5.RX_DATA[2] | | | gpio5.IO[0] | | | tpsmp.HDATA[2] | sjc.sjc_gpucr1_reg[11] |
| SAI3_TXD | sai3.TX_DATA[0] | gpt1.COMPARE2 | | sai5.RX_DATA[3] | | | gpio5.IO[1] | | | tpsmp.HDATA[3] | sjc.sjc_gpucr1_reg[11] |
| SAI3_MCLK | sai3.MCLK | gpt1.COMPARE3 | | sai5.MCLK | | | gpio5.IO[2] | | | tpsmp.HDATA[4] | sjc.sjc_gpucr1_reg[11] |
| SPDIF_TX | spdif1.OUT | pwm4.OUT | | | | | gpio5.IO[3] | | | tpsmp.HDATA[5] | sjc.sjc_gpucr1_reg[11] |
| SPDIF_RX | spdif1.IN | pwm3.OUT | | | | | gpio5.IO[4] | | | tpsmp.HDATA[6] | sjc.sjc_gpucr1_reg[11] |
| SPDIF_EXT_CLK | spdif1.EXT_CLK | pwm2.OUT | | | | | gpio5.IO[5] | | | tpsmp.HDATA[7] | sjc.sjc_gpucr1_reg[11] |
| ECSPI1_SCLK | ecspi1.SCLK | pwm1.OUT | | | | | gpio5.IO[6] | | | tpsmp.HDATA[8] | sjc.sjc_gpucr1_reg[11] |
| ECSPI1_MOSI | ecspi1.MOSI | uart3.RX | | | | | gpio5.IO[7] | | | tpsmp.HDATA[9] | sjc.sjc_gpucr1_reg[11] |
| ECSPI1_MISO | ecspi1.MISO | uart3.TX | | | | | gpio5.IO[8] | | | tpsmp.HDATA[10] | sjc.sjc_gpucr1_reg[11] |
| ECSPI1_SS0 | ecspi1.SS0 | uart3.CTS_B | | | | | gpio5.IO[9] | | | tpsmp.HDATA[11] | sjc.sjc_gpucr1_reg[11] |
| ECSPI2_SCLK | ecspi2.SCLK | uart3.RTS_B | | | | | gpio5.IO[10] | | | tpsmp.HDATA[12] | sjc.sjc_gpucr1_reg[11] |
| ECSPI2_MOSI | ecspi2.MOSI | uart4.RX | | | | | gpio5.IO[11] | | | tpsmp.HDATA[13] | sjc.sjc_gpucr1_reg[11] |
| ECSPI2_MISO | ecspi2.MISO | uart4.TX | | | | | gpio5.IO[12] | | | tpsmp.HDATA[14] | sjc.sjc_gpucr1_reg[11] |
| ECSPI2_SS0 | ecspi2.SS0 | uart4.CTS_B | | | | | gpio5.IO[13] | | | tpsmp.HDATA[15] | sjc.sjc_gpucr1_reg[11] |
| I2C1_SCL | i2c1.SCL | uart4.RTS_B | | | | | gpio5.IO[14] | | | tpsmp.HDATA[16] | sjc.sjc_gpucr1_reg[11] |
| I2C1_SDA | i2c1.SDA | enet1.MDC | | | | | gpio5.IO[15] | | | tpsmp.HDATA[17] | sjc.sjc_gpucr1_reg[11] |
| I2C2_SCL | i2c2.SCL | enet1.MDIO | | | | | gpio5.IO[16] | | | tpsmp.HDATA[18] | sjc.sjc_gpucr1_reg[11] |
| I2C2_SDA | i2c2.SDA | enet1.1588_EVENT1_IN | | | | | gpio5.IO[17] | | | tpsmp.HDATA[19] | sjc.sjc_gpucr1_reg[11] |
| I2C3_SCL | i2c3.SCL | enet1.1588_EVENT1_OUT | | gpt2.CLK | | | gpio5.IO[18] | | | tpsmp.HDATA[20] | sjc.sjc_gpucr1_reg[11] |
| I2C3_SDA | i2c3.SDA | pwm4.OUT | | gpt3.CLK | | | gpio5.IO[19] | | | tpsmp.HDATA[21] | sjc.sjc_gpucr1_reg[11] |
| I2C4_SCL | i2c4.SCL | pwm3.OUT | | pcie1.CLKREQ_B | | | gpio5.IO[20] | | | tpsmp.HDATA[22] | sjc.sjc_gpucr1_reg[11] |
| I2C4_SDA | i2c4.SDA | pwm2.OUT | | pcie2.CLKREQ_B | | | gpio5.IO[21] | | | tpsmp.HDATA[23] | sjc.sjc_gpucr1_reg[11] |
| UART1_RXD | uart1.RX | pwm1.OUT | | | | | gpio5.IO[22] | | | tpsmp.HDATA[24] | sjc.sjc_gpucr1_reg[11] |
| UART1_TXD | uart1.TX | ecspi3.SCLK | | | | | gpio5.IO[23] | | | tpsmp.HDATA[25] | sjc.sjc_gpucr1_reg[11] |
| UART2_RXD | uart2.RX | ecspi3.MOSI | | | | | gpio5.IO[24] | | | tpsmp.HDATA[26] | sjc.sjc_gpucr1_reg[11] |
| UART2_TXD | uart2.TX | ecspi3.MISO | | | | | gpio5.IO[25] | | | tpsmp.HDATA[27] | sjc.sjc_gpucr1_reg[11] |
| UART3_RXD | uart3.RX | ecspi3.SS0 | | | | | gpio5.IO[26] | | | tpsmp.HDATA[28] | sjc.sjc_gpucr1_reg[11] |
| UART3_TXD | uart3.TX | uart1.CTS_B | | | | | gpio5.IO[27] | | | tpsmp.HDATA[29] | sjc.sjc_gpucr1_reg[11] |
| UART4_RXD | uart4.RX | uart1.RTS_B | | pcie1.CLKREQ_B | | | gpio5.IO[28] | | | tpsmp.HDATA[30] | sjc.sjc_gpucr1_reg[11] |
| UART4_TXD | uart4.TX | uart2.CTS_B | | pcie2.CLKREQ_B | | | gpio5.IO[29] | | | tpsmp.HDATA[31] | sjc.sjc_gpucr1_reg[11] |
| | | uart2.RTS_B | | | | | | | | | |

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