3 Performance data

3.1 CV/CC output voltage characteristics

The board V-I characteristic is measured at the PCB output connector, at both 115 and 230 V_{AC}, under different line and load conditions.

The figures below show the measurement results: the load regulation is very accurate and barely affected by the USB connector contact resistance (≈30 mΩ).

Figure 9. Output characteristic at 115 V_{AC}

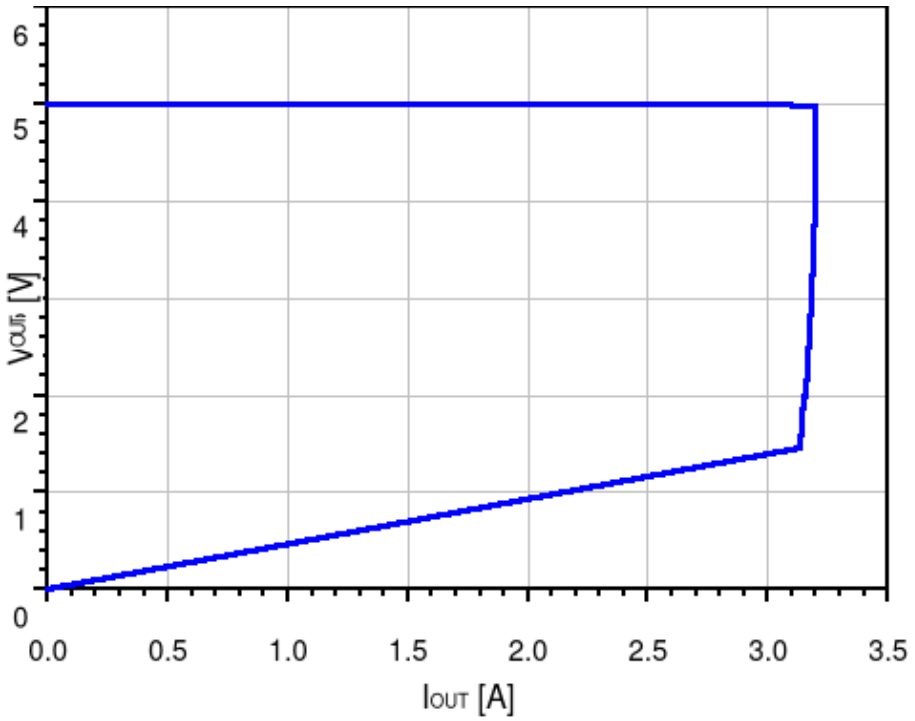
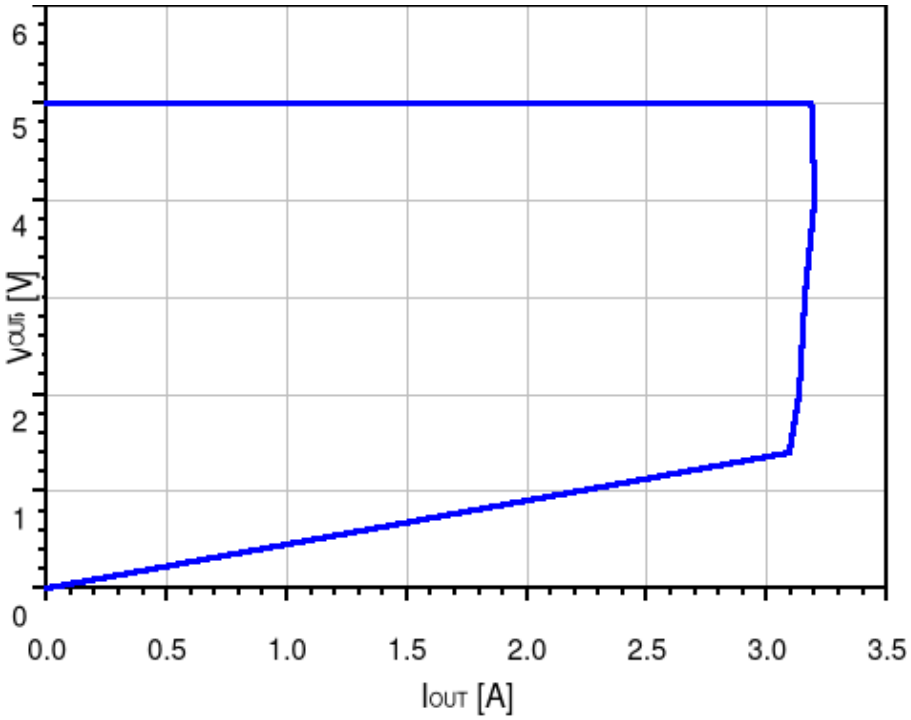


Figure 10. **Output characteristic at 230 V_{AC}**



3.2 Efficiency and light load measurements

Converter efficiency and no-load consumption are measured at nominal input voltages (115 V_{AC} and 230 V_{AC}): the rated average power is compared with the European Code of Conduct revision 5 - Tier 2 (EuCoC) requirements.

Figure 11. **Efficiency vs. output power**

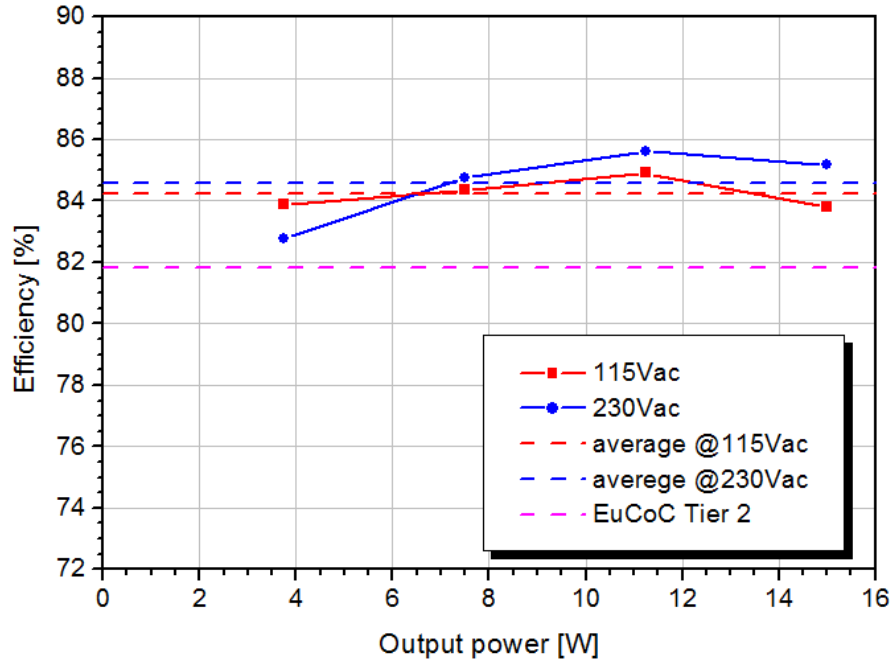


Table 4. Average efficiency of the rated output load

% of rated power	Efficiency	
	115 V_{AC}	230 V_{AC}
25%	83.89%	82.78%
50%	84.36%	84.75%
75%	84.91%	85.62%
100%	83.80%	85.18%
Average	84.24%	84.58%
EU Code of Conduct rev. 5 – Tier 2 limit : 81.84%		

Table 5. Efficiency at 10% of the rated output load

Input voltage	Efficiency
115 V_{AC}	81.36 %
230 V_{AC}	77.97 %
EU Code of Conduct rev. 5 – Tier 2 limit : 72.48%	

Table 6. No load consumption

Input voltage	Input power
115 V_{AC}	12.1 mW
230 V_{AC}	12.3 mW

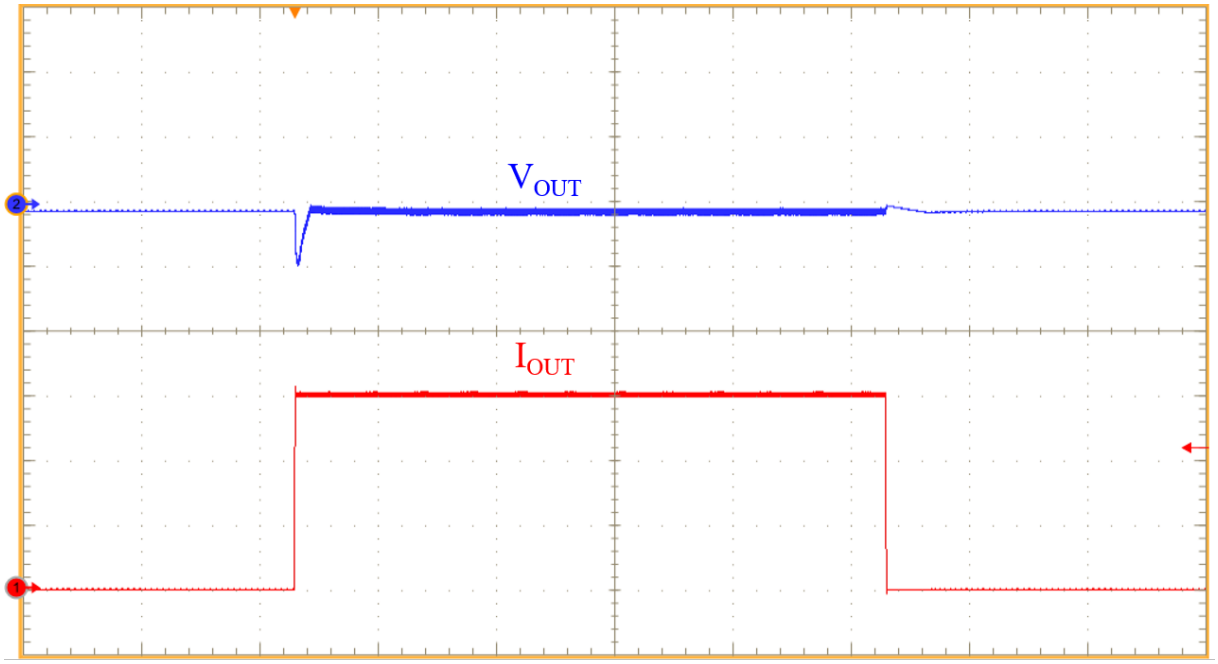
4 Typical waveforms

4.1 Dynamic load regulation response

The board V-I characteristic is measured at the PCB output connector at both 115 V_{AC} and 230 V_{AC} for different line and load conditions.

The board is subjected to dynamic load variations from 0% to 100% of the nominal load. The following figures show no abnormal oscillation in the output and the overshoot and undershoot values are acceptable.

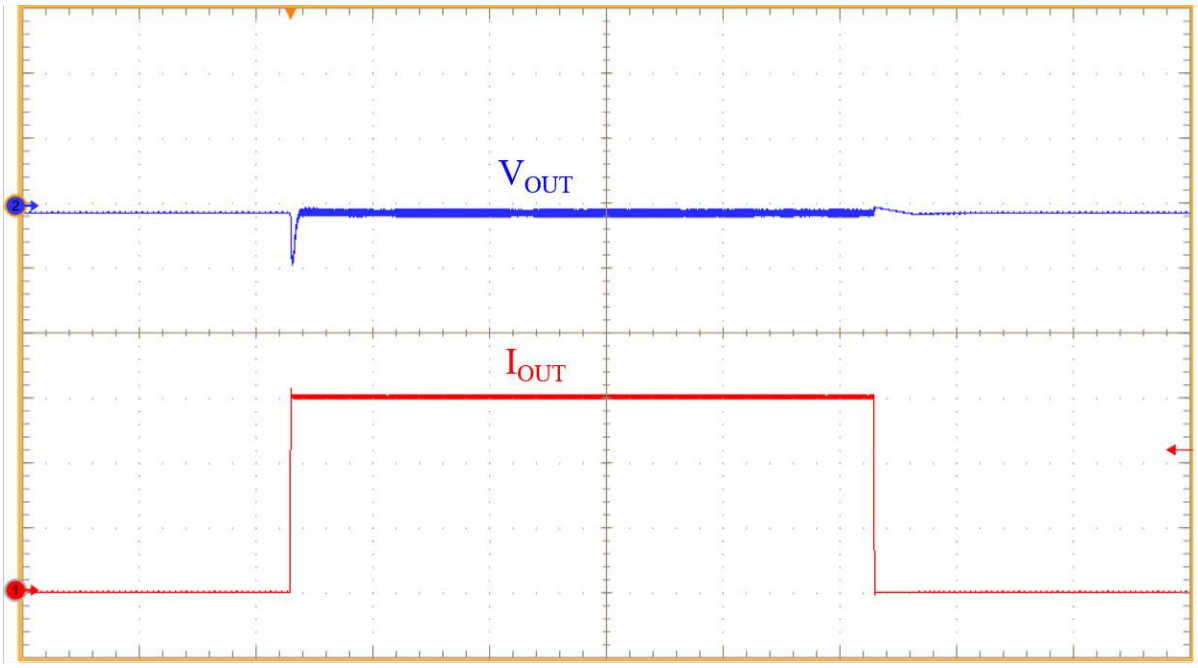
Figure 12. Dynamic load regulation from no load to full load at 115 V_{AC}



Ch1 1A/div
Ch2 500mV/div
Ch2 offset 5V
M 20.0ms/div

Ch1 (Max): 3.1A
Ch2 (Max): 5V
Ch2 (Max): 4.6V

Figure 13. **Dynamic load regulation from no load to full load at 230 V_{AC}**



4.2 Switching waveforms

The drain voltage and the drain current waveforms are given for the two nominal input voltages and for the minimum and the maximum voltage of the converter input operating range.

The following figures show the drain voltage and the drain current waveforms for the two nominal input voltages. They also show the minimum and maximum converter input operating voltage during converter constant voltage mode (CV).

Figure 14. **Normal operation in CC mode at full load and 90 V_{AC}**

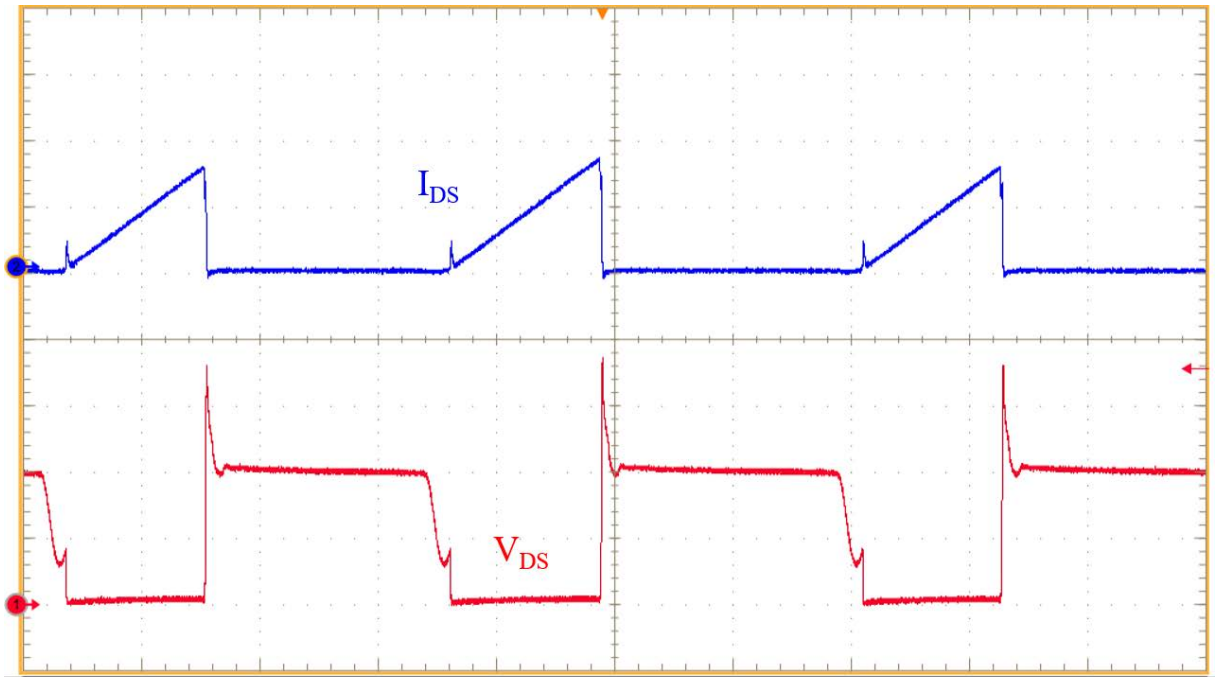


Figure 15. **Normal operation in CV mode at full load and 115 V_{AC}**

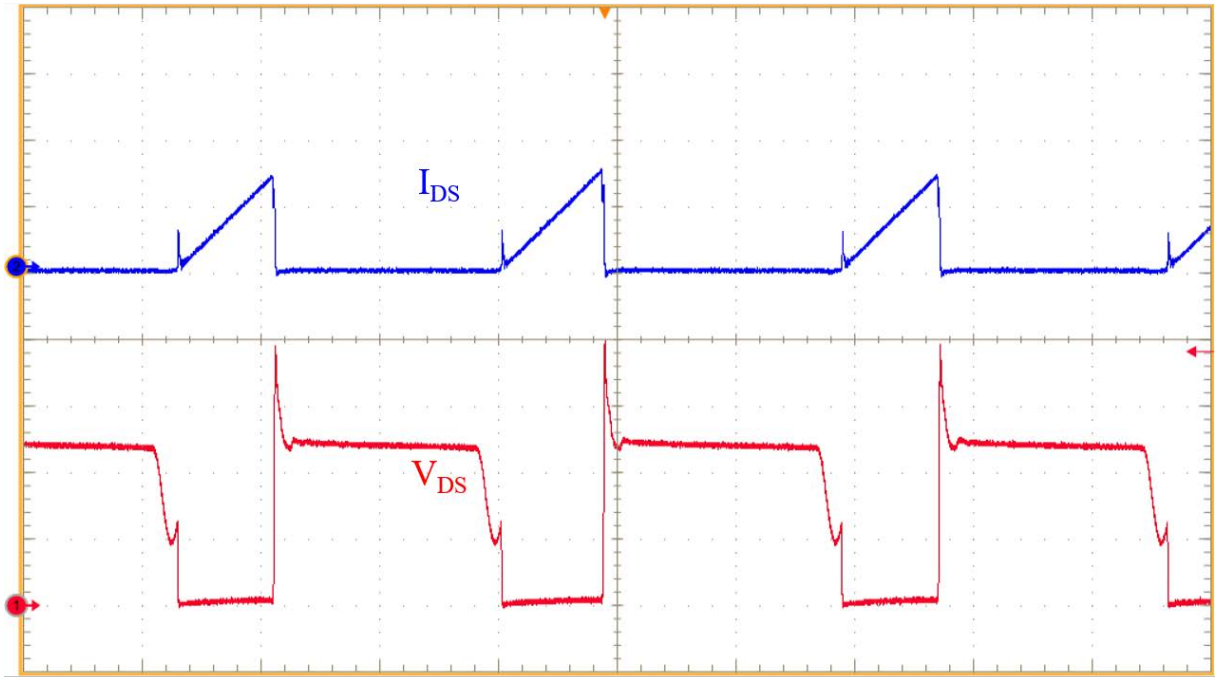
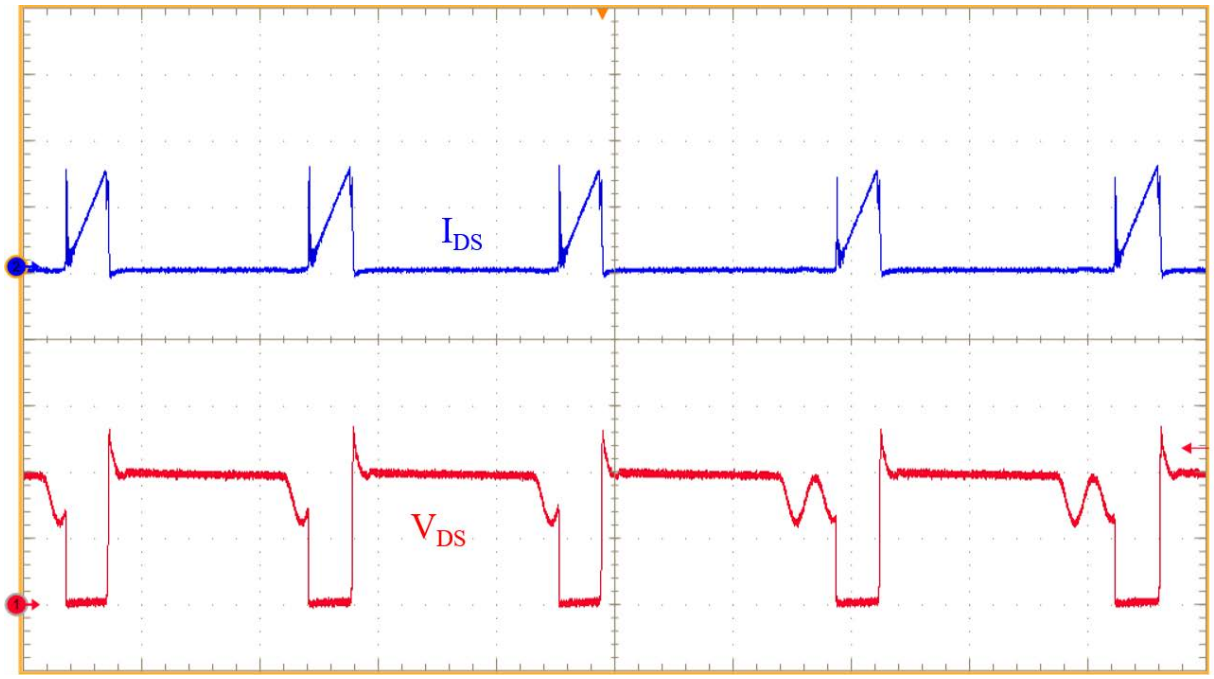


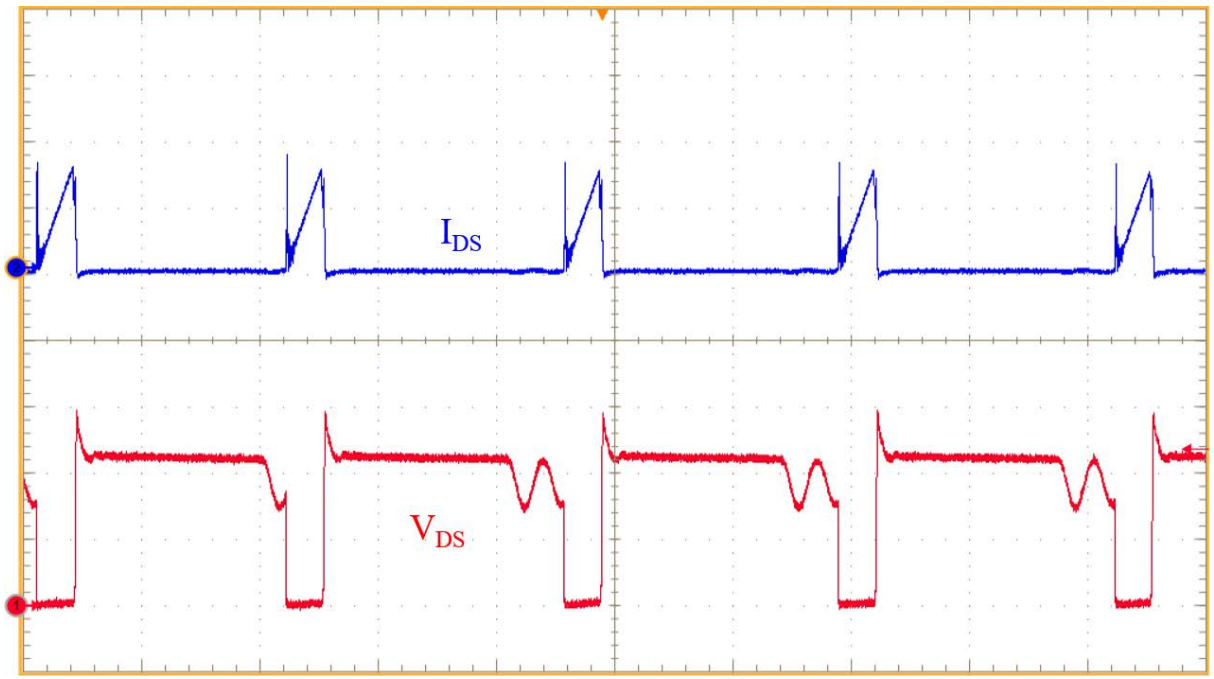
Figure 16. **Normal operation in CV mode at full load and 230 V_{AC}**



Ch1 200V/div
Ch2 400mA/div
M 5.0µs/div

Ch1 (Freq): 87.3kHz
Ch1 (Max): 563V
Ch2 (Max): 610.0mA

Figure 17. **Normal operation in CV mode at full load and 264 V_{AC}**



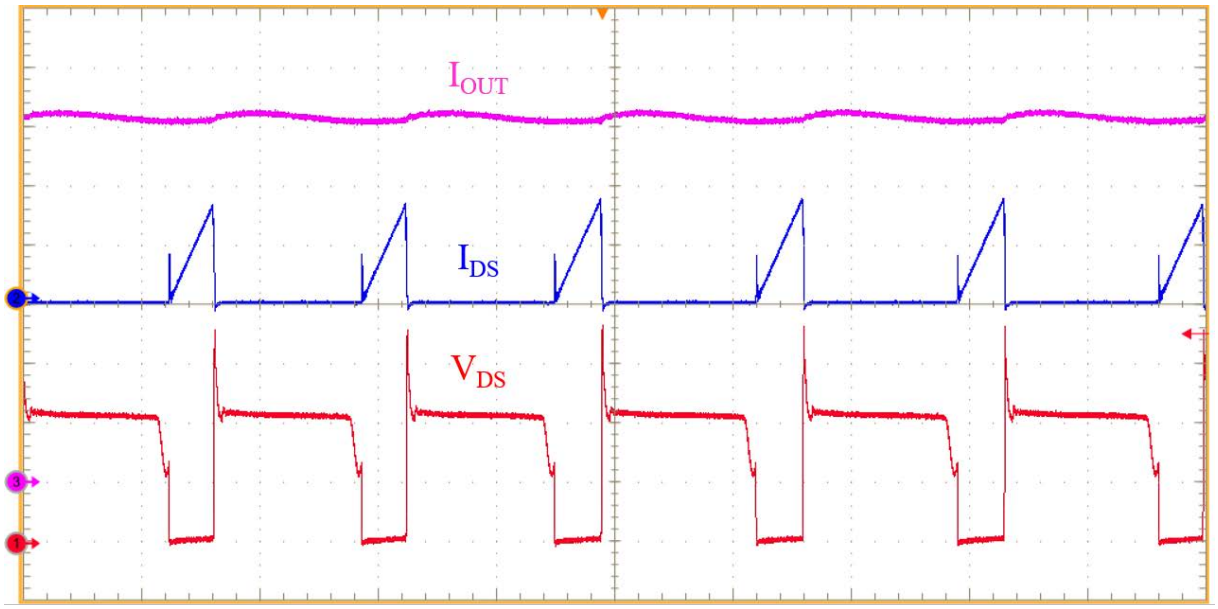
Ch1 200V/div
Ch2 400mA/div
M 5.0µs/div

Ch1 (Freq): 91.0kHz
Ch1 (Max): 590V
Ch2 (Max): 602.0mA

In order to simulate the operation constant current mode (CC mode), the electronic load has been set in constant voltage at 3V, so that this voltage is imposed on the charger output from the E-load: the charger is forced to enter CC mode, thus regulating the output current at its nominal value.

Figure 15 and Figure 16 show the CC mode typical waveforms.

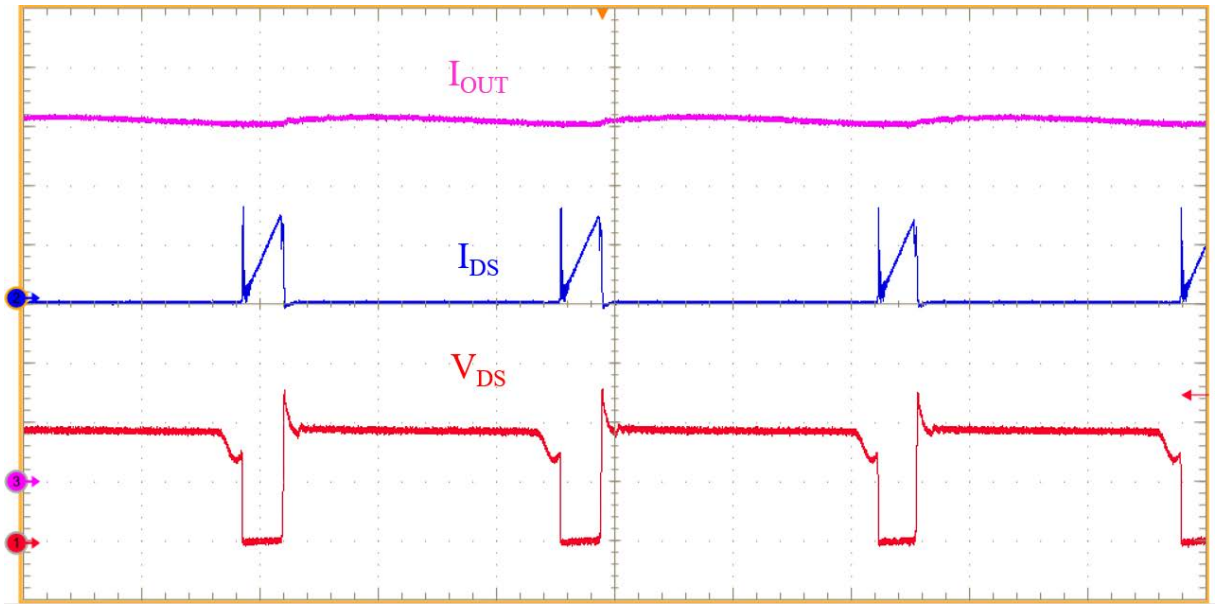
Figure 18. Normal operations in CC mode with V_{OUT} = 3 V and 115 V_{AC}



Ch1 100V/div
Ch2 400mA/div
Ch3 500mA/div
M 10.0µs/div

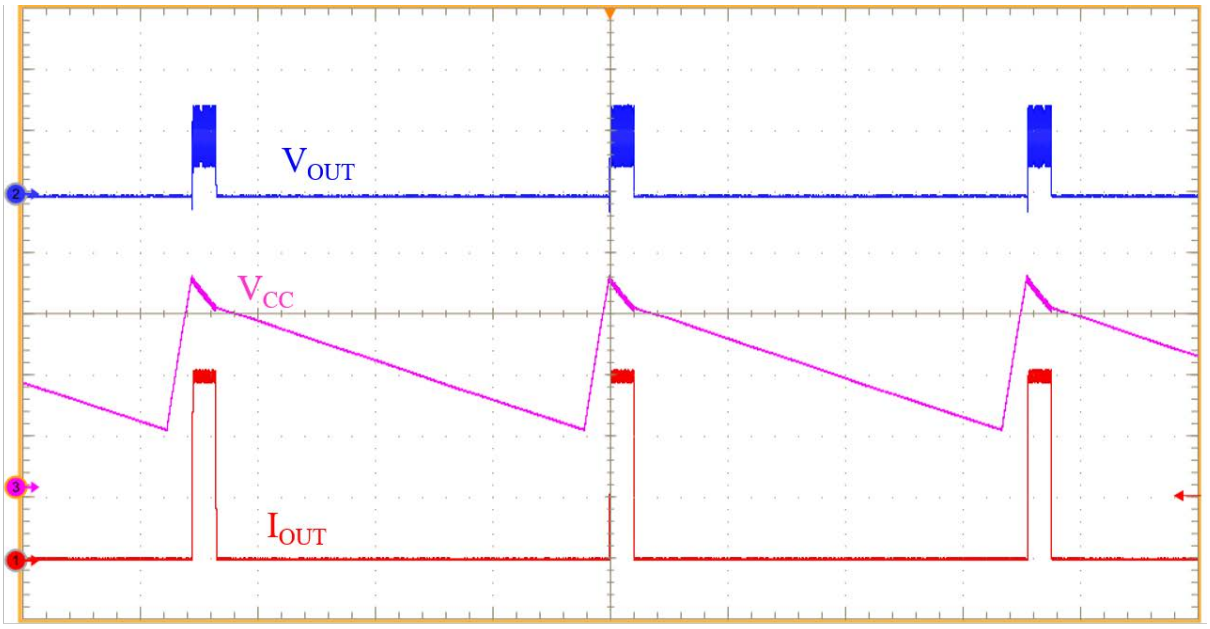
Ch1 (Freq): 61.4kHz
Ch1 (Max): 368.0V
Ch2 (Max): 673.3mA
Ch3 (Max): 3.08A

Figure 19. **Normal operations in CC mode with V_{OUT} = 3 V and 230 V_{AC}**



The converter is also tested in short-circuit to trigger the output UVP protection, which protect the converter in case of output short circuit: the typical waveforms are shown in Figure 17.

Figure 20. **Short-circuit protection**



Ch1 1A/div
Ch2 300mV/div
Ch3 5V/div
M 100ms/div

Ch1 (Max): 3.12A
Ch2 (Max): 17.3V
Ch3 (Min): 4.6V

4.3 Output overvoltage protection

The output overvoltage protection is tested by shorting the opto-diode. This causes the converter to operate in open loop and the excess power (with respect to the load) charges the output capacitance, increasing the output voltage as the OVP is tripped and the converter stops switching.

The figures below show how the converter stops switching and enters protection mode when the voltage reaches OVP threshold (set by the R4 and R5 voltage dividers).

Figure 21. **Output OVP protection: protection triggering**

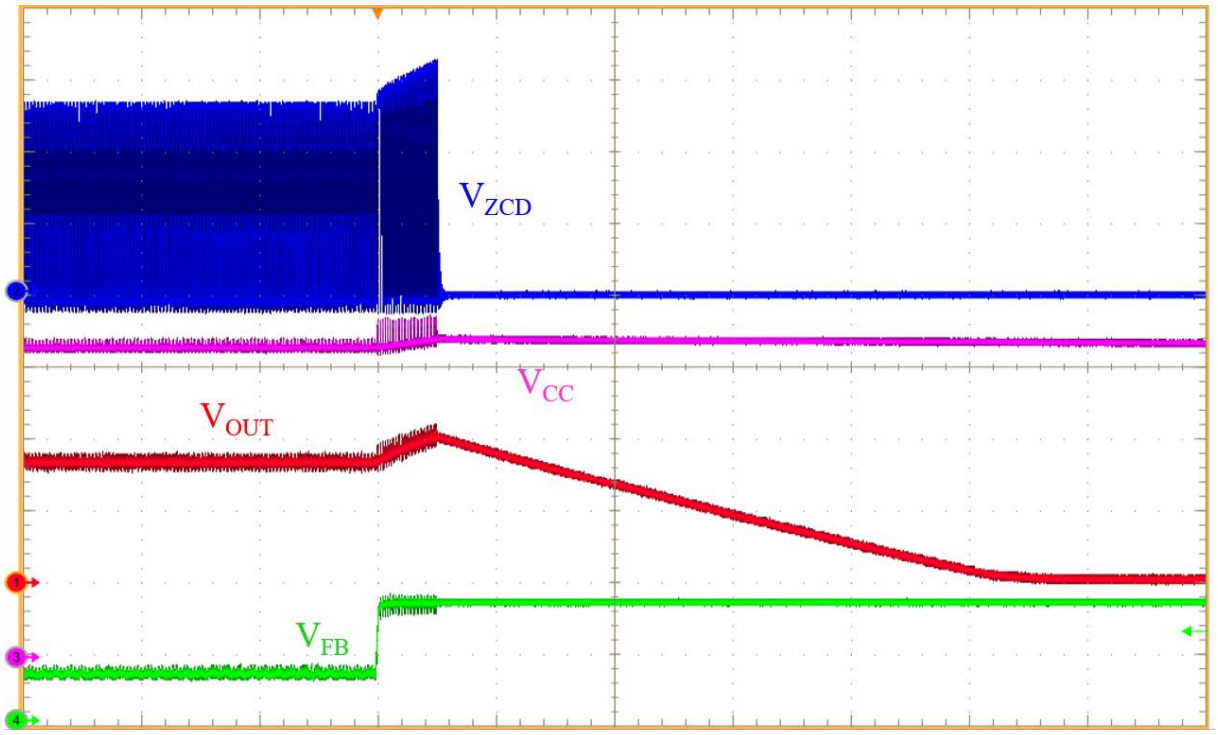


Figure 22. **Output OVP protection: zoom**

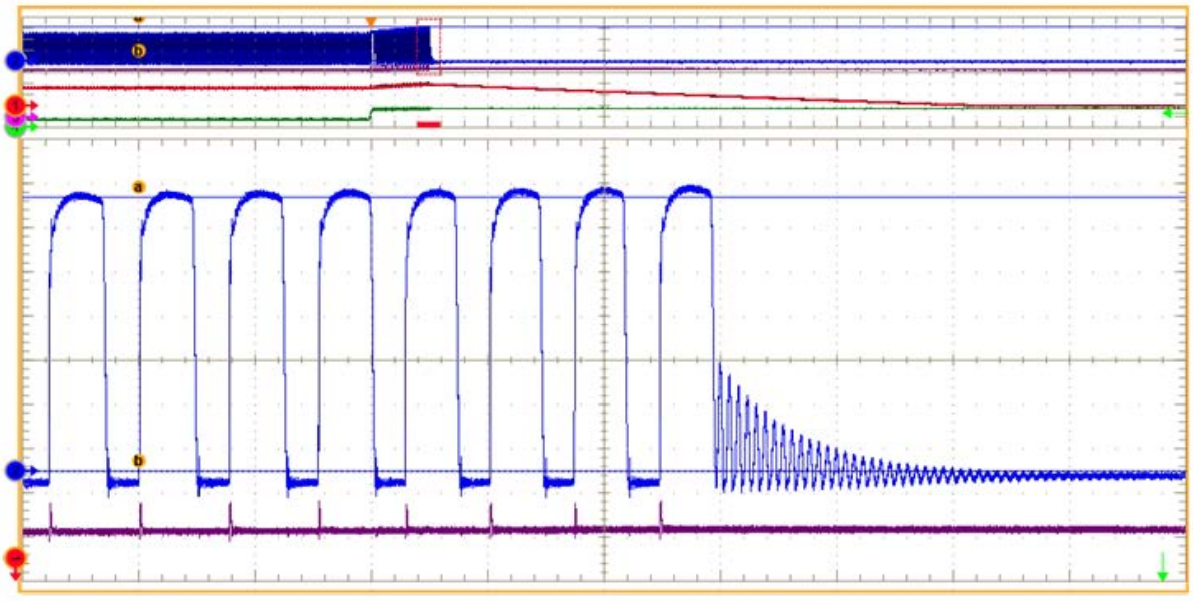
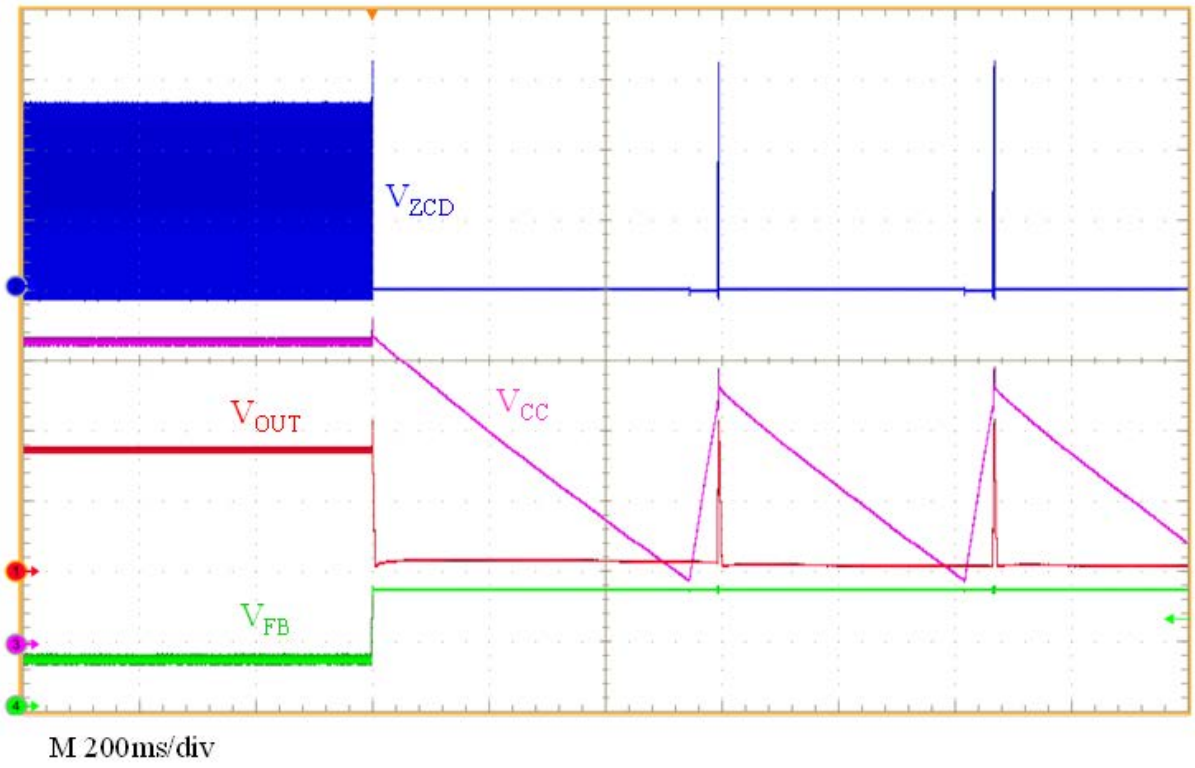


Figure 23. **Output OVP protection: zoom.**



5 Conducted noise measurements

A pre-compliance test for EN55022 (Class B) European normative was performed using an average measurement detector of the conducted noise emissions at full load and nominal mains voltages.

The results show a comfortable margin between the measurements and the respective limits

Figure 24. CE average measurement at 115 V_{AC} and full load

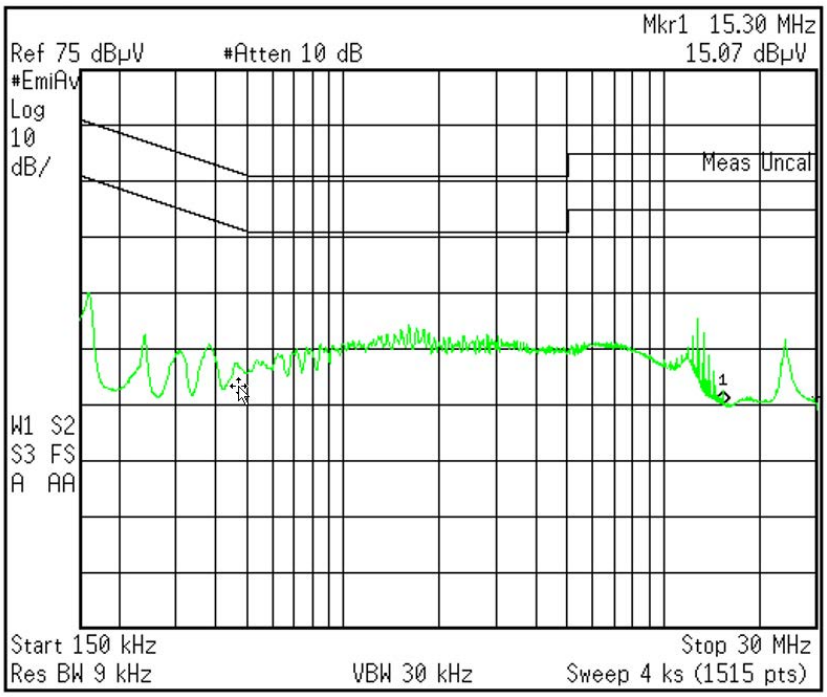
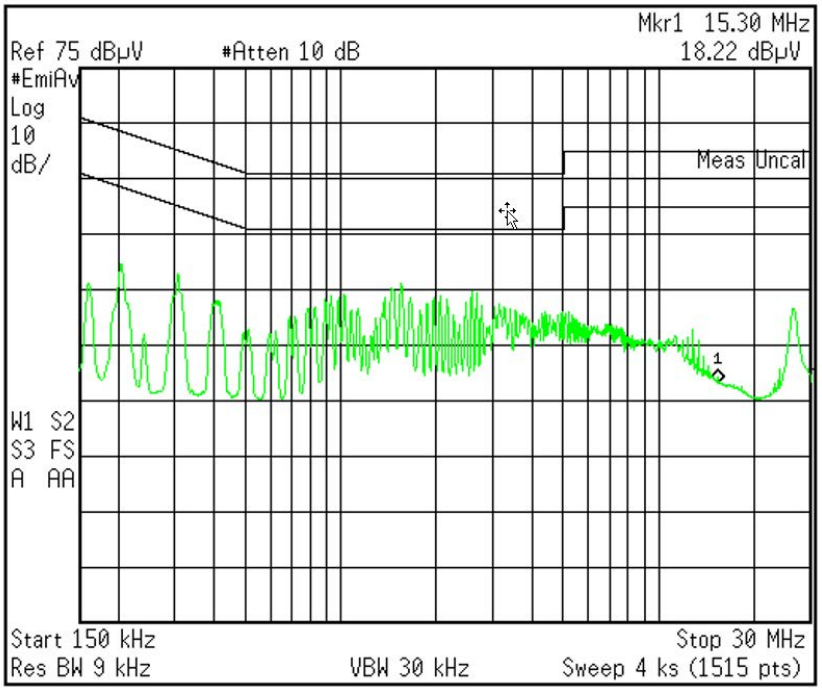


Figure 25. CE average measurement at 230 V_{AC} and full load.



6 Immunity tests

The board was subjected to immunity tests according to IEC61000. The results are classified according the criteria given by the standard:

1. Normal performance
2. Temporary degradation or loss of function or performance, with automatic return to normal operation
3. Temporary degradation or loss of function with external intervention to re-cover normal operation
4. Degradation or loss of function, need substitution of damaged components to recover normal operation

6.1 ESD Immunity test (IEC 61000-4-2)

The test was performed on a single test board. The input voltage was set to 230 V_{AC} and the output was loaded to full load and proper operation was verified through a current probe on the output.

The test conditions are listed below:

- Contact discharge and Air discharge methods
- Discharge circuit: 150pF/330Ω
- Polarity: positive / negative

Table 7. ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	A
L vs. PE	10 kV	Negative	PASS	A
N vs. PE	10 kV	Positive	PASS	A
N vs. PE	10 kV	Negative	PASS	A

Table 8. ESD contact discharge test results with PE connected on secondary GND

Noise injection	ESD level	Polarity	Result	Criterion
L vs. GND	8 kV	Positive	PASS	A
L vs. GND	8 kV	Negative	PASS	A
N vs. GND	8 kV	Positive	PASS	A
N vs. GND	8 kV	Negative	PASS	A

Table 9. ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	A
Horizontal coupling plane	20 kV	Negative	PASS	A
Vertical coupling plane	20 kV	Positive	PASS	A
Vertical coupling plane	20 kV	Negative	PASS	A

6.2 Surge immunity test (IEC 61000-4-5)

The test was performed on a single test board. The input voltage was set to $230V_{AC}$ and the output was loaded with 10% of the nominal load and proper operation was verified connecting a current probe on the output.

The test conditions are listed below:

- Repetition rate: 1 minute
- Applied to: input lines vs. EARTH – Common Mode
- Applied to: both input line (L vs. N) – Differential Mode
- A network made up by a varistor and two Y1 capacitors is connected across the AC line connector according to the norm.

The test results are listed in the following tables.

Table 10. Common mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	A
N vs. PE	2 kV	Positive	PASS	A
L vs. PE	2 kV	Negative	PASS	A
N vs. PE	2 kV	Negative	PASS	A

Table 11. Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	A
L vs. N	2 kV	Negative	PASS	A

The tests performed show that the board is able to withstand lightning disturbances applied on the input line in Common Mode and Differential Mode for each severity level.

According to the standard, the application can be classified as level 3.

6.3 Burst immunity test (IEC 61000-4-4)

The test was performed on a single test board. The input voltage was set to $230V_{AC}$ and the output was loaded with 10% of the nominal load and proper operation was verified connecting a current probe on the output.

The test conditions are listed below:

- Polarity: positive/negative
- Burst duration: 15 ms ± 20 % at 5 kHz
- Burst period: 300 ms ± 20 %
- Duration time: 1 minute
- Applied to: AC lines through integrated capacitive coupling clamp.

Table 12. Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L / PE	4 kV	Positive	PASS	A
N / PE	4 kV	Positive	PASS	A
L / N	4 kV	Positive	PASS	A

Noise injection	Burst level	Polarity	Result	Criterion
L / PE	4 kV	Negative	PASS	A
N / PE	4 kV	Negative	PASS	A
L / N	4 kV	Negative	PASS	A

7 Thermal tests

A thermal analysis of the board was performed using an IR camera.

The board was submitted to full load at nominal input voltage and the thermal map was taken 30 minutes after the power on at ambient temperature (25 °C).

The following figures show the results.

Figure 26. Thermal map at 115 V_{AC} and full load (bottom side)

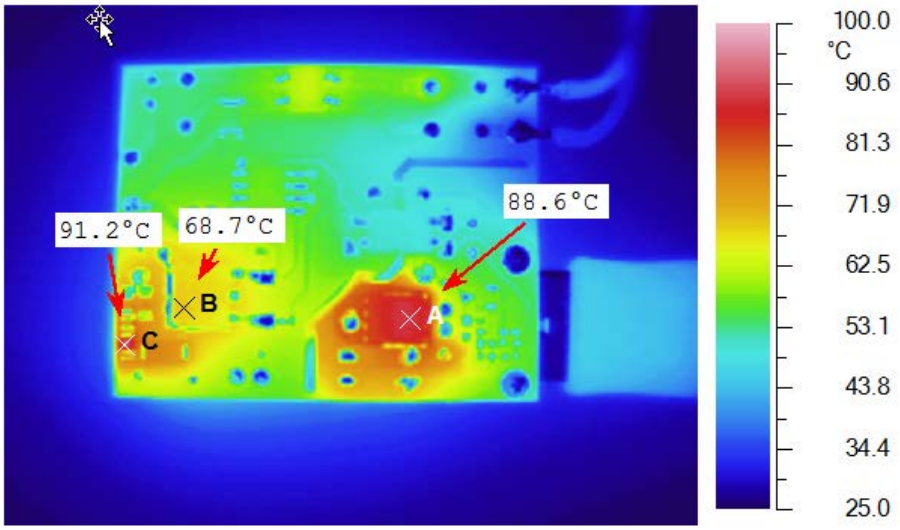


Figure 27. Thermal map at 115 V_{AC} and full load (top side)

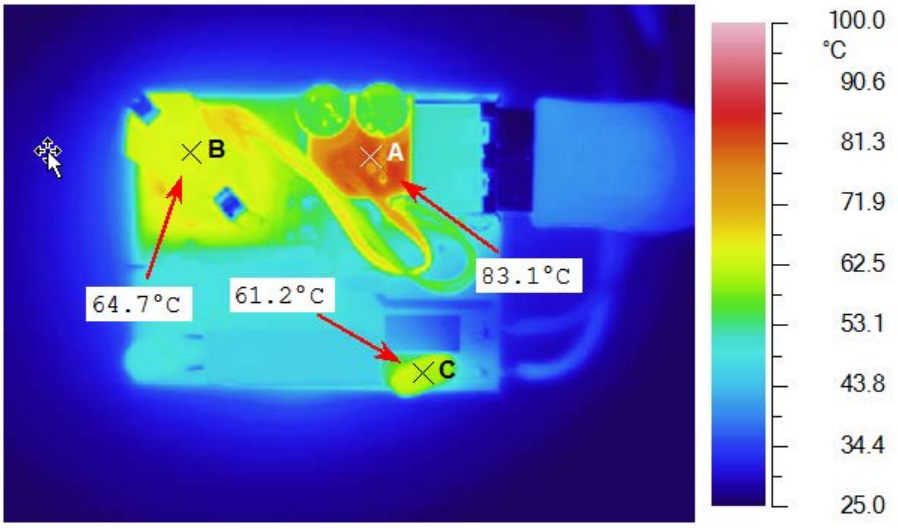


Figure 28. **Thermal map at 115 V_{AC} and full load (transformer)**

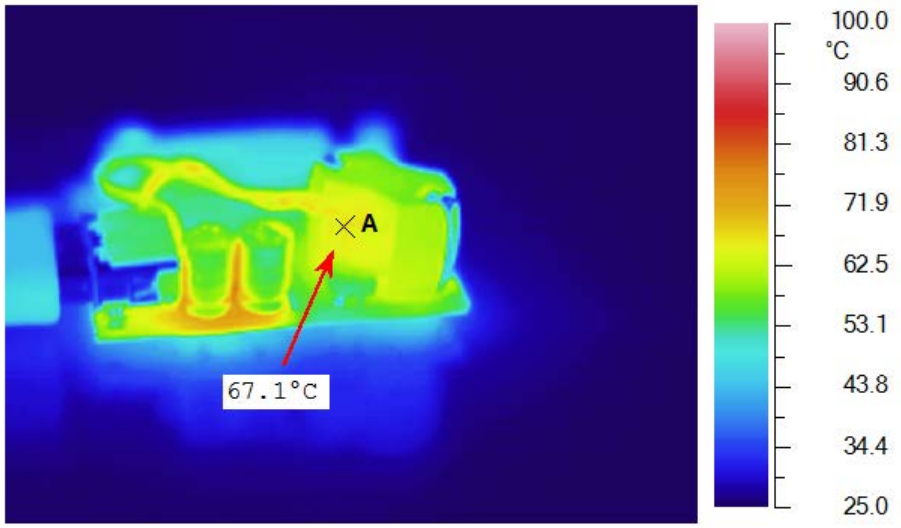


Figure 29. **Thermal map at 230 V_{AC} and full load (bottom side)**

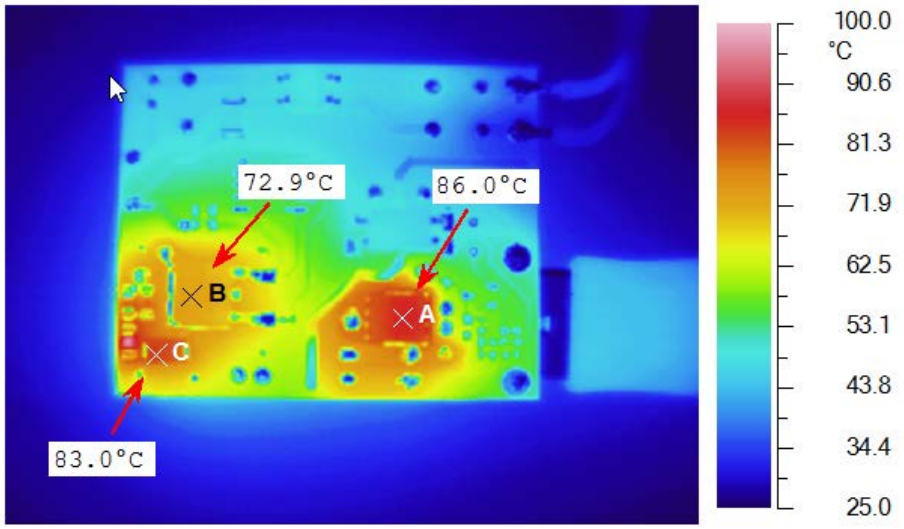


Figure 30. Thermal map at 230 V_{AC} and full load (top side)

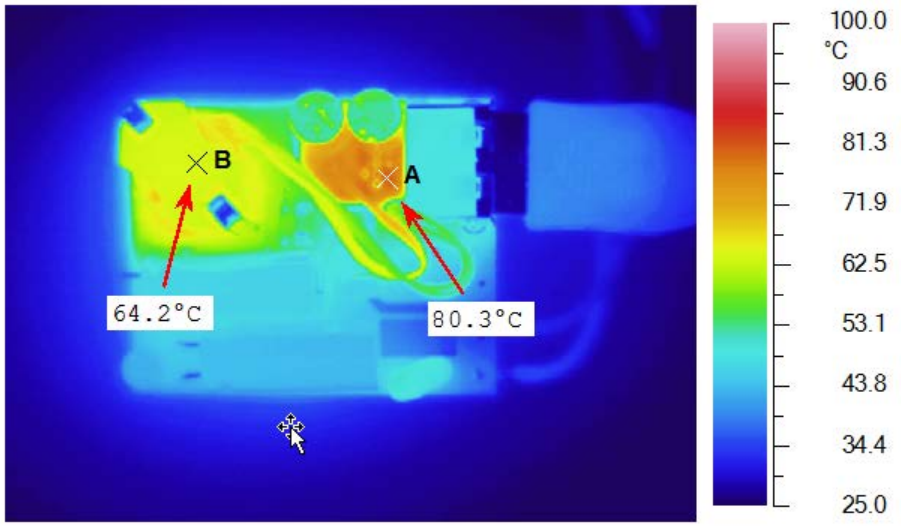
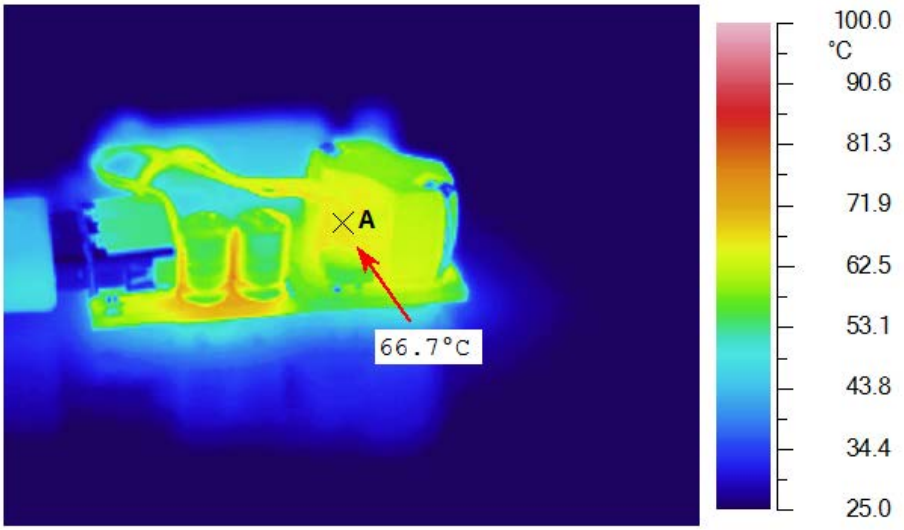



Figure 31. Thermal map at 230 V_{AC} and full load (transformer)