ARM Cortex® -M0

32-bit Microcontroller

NuMicro® Family
NDA102 Series
Datasheet

The information described in this document is the exclusive intellectual property of Nuvoton Technology Corporation and shall not be reproduced without permission from Nuvoton.

Nuvoton is providing this document only for reference purposes of NuMicro microcontroller based system design. Nuvoton assumes no responsibility for errors or omissions.

All data and specifications are subject to change without notice.

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

TABLE OF CONTENTS

1 GENERAL DESCRIPTION 7
2 FEATURES 8
3 ABBREVIATIONS 12
4 PARTS INFORMATION LIST AND PIN CONFIGURATION 13
4.1 NuMicro® NDA102 Naming Rule 13
4.2 NuMicro® NDA102 Series Selection Guide 14
4.3 Pin Configuration 15
4.3.1 TSSOP 28-Pin 15
4.4 Pin Description 16
4.4.1 NDA102 Series Pin Description 16
4.4.2 GPIO Multi-function Pin Summary 20
5 BLOCK DIAGRAM 23
5.1 NuMicro® NDA102 Block Diagram 23
6 FUNCTIONAL DESCRIPTION 24
6.1 ARM® Cortex®-M0 Core 24
6.1.1 Overview 24
6.1.2 Features 25
6.2 System Manager 26
6.2.1 Overview 26
6.2.2 System Reset 26
6.2.3 Power Modes and Wake-up Sources 32
6.2.4 System Power Architecture 35
6.2.5 System Memory Mapping 36
6.2.6 Register Protection 37
6.2.7 Memory Organization 39
6.2.8 System Timer (SysTick) 42
6.2.9 Nested Vectored Interrupt Control (NVIC) 47
6.2.10 System Control Registers 67
6.3 Clock Controller 76
6.3.1 Overview 76
6.3.2 Auto Trim 78
6.3.3 System Clock and SysTick Clock 78
6.3.4 Peripherals Clock Source Selection 79
6.3.5 Power-down Mode Clock 81
6.3.6 Frequency Divider Output 81
6.4 Flash Memory Controller (FMC) 83
6.4.1 Overview 83
6.4.2 Features 83
6.5 General Purpose I/O (GPIO) 84
6.5.1 Overview 84
6.5.2 Features 84

6.5.3 GPIO Interrupt and Wake-up Function 85
6.6 Timer Controller (TIMER) 86
6.6.1 Overview 86
6.6.2 Features 86
6.7 Enhanced Input Capture Timer (ECAP) 87
6.7.1 Overview 87
6.7.2 Features 87
6.8 Enhanced PWM Generator (EPWM) 88
6.8.1 Overview 88
6.8.2 Features 88
6.9 Basic PWM Generator (BPWM) 90
6.9.1 Overview 90
6.9.2 Features 90
6.10 Watchdog Timer (WDT) 91
6.10.1 Overview 91
6.10.2 Features 91
6.11 USCI – Universal Serial Control Interface Controller 92
6.11.1 Overview 92
6.11.2 Features 92
6.12 USCI – UART Mode 93
6.12.1 Overview 93
6.12.2 Features 93
6.13 USCI – SPI Mode 94
6.13.1 Overview 94
6.13.2 Features 94
6.14 USCI – I^2C Mode 96
6.14.1 Overview 96
6.14.2 Features 96
6.15 Hardware Divider (HDIV) 97
6.15.1 Overview 97
6.15.2 Features 97
6.16 Analog to Digital Converter (ADC) 98
6.16.1 Overview 98
6.16.2 Features 98
6.17 Analog Comparator (ACMP) 99
6.17.1 Overview 99
6.17.2 Features 99
6.18 Programmable Gain Amplifier (PGA) 100
6.18.1 Overview 100
6.18.2 Features 100
7 APPLICATION CIRCUIT 101
8 ELECTRICAL CHARACTERISTICS 102
8.1 Absolute Maximum Ratings 102

8.2 DC Electrical Characteristics 103
8.3 AC Electrical Characteristics 108
8.3.1 External Input Clock 108
8.3.2 External 4~24 MHz High Speed Crystal (HXT) 108
8.3.3 External 32.768 kHz XTAL Oscillator (LXT) 108
8.3.4 Typical Crystal Application Circuits 108
8.3.5 48 MHz Internal High Speed RC Oscillator (HIRC) 109
8.3.6 10 kHz Internal Low Speed RC Oscillator (LIRC) 109
8.4 Analog Characteristics 110
8.4.1 12-bit SAR ADC 110
8.4.2 LDO & Power Management 111
8.4.3 Low Voltage Reset 111
8.4.4 Brown-out Detector 112
8.4.5 Power-on Reset 112
8.4.6 Comparator 113
8.4.7 PGA 113
8.5 Flash DC Electrical Characteristics 115
9 PACKAGE DIMENSIONS 116
9.1 28-Pin TSSOP (4.4x9.7x1.0 mm) 116
10 REVISION HISTORY 117

List of Figures

Figure 4.1-1 NuMicro® NDA102 Series Selection Code 13
Figure 4.3-1 NuMicro® NDA102 Series TSSOP 28-pin Diagram 15
Figure 4.3-2 NuMicro® NDA102 Series TSSOP 28-pin Multi-function Diagram 15
Figure 5.1-1 NuMicro® NDA102 Block Diagram 23
Figure 6.1-1 Functional Block Diagram 24
Figure 6.2-1 System Reset Resources 27
Figure 6.2-2 nRESET Reset Waveform 29
Figure 6.2-3 Power-on Reset (POR) Waveform 29
Figure 6.2-4 Low Voltage Reset (LVR) Waveform 30
Figure 6.2-5 Brown-out Detector (BOD) Waveform 31
Figure 6.2-6 Power Mode State Machine 32
Figure 6.2-7 NuMicro® NDA102 Series Power Architecture Diagram 35
Figure 6.2-8 NuMicro® NDA102 Flash, Security and Configuration Map 39
Figure 6.2-9 SRAM Block Diagram 41
Figure 6.3-1 Clock Generator Block Diagram 76
Figure 6.3-2 Clock Generator Global View Diagram 77
Figure 6.3-3 System Clock Block Diagram 78
Figure 6.3-4 SysTick Clock Control Block Diagram 79
Figure 6.3-5 Peripherals Bus Clock Source Selection for PCLK 80
Figure 6.3-6 Clock Source of Frequency Divider 82
Figure 6.3-7 Block Diagram of Frequency Divider 82
Figure 6.5-1 I/O Pin Block Diagram 84
Figure 6.13-1 SPI Master Mode Application Block Diagram (x=0, 1) 94
Figure 6.13-2 SPI Slave Mode Application Block Diagram (x=0, 1) 94
Figure 6.14-1 I^2C Bus Timing 96
Figure 8.3-1 NDA102 Typical Crystal Application Circuit 109

List of Tables

Table 3-1 List of Abbreviations 12
Table 4.2-1 NuMicro® NDA102 Series Selection Guide 14
Table 4.4-1 TSSOP28 Pin Description 19
Table 4.4-2 TSSOP28 Multi-function Pin Summary 22
Table 6.2-1 Reset Value of Registers 28
Table 6.2-2 Power Mode Difference Table 32
Table 6.2-3 Clocks in Power Modes 33
Table 6.2-4 Condition of Entering Power-down Mode Again 34
Table 6.2-5 Memory Mapping Table 36
Table 6.2-6 Protected Registers 38
Table 6.2-7 Address Space Assignments for On-Chip Modules 40
Table 6.2-8 Exception Model 48
Table 6.2-9 System Interrupt Map Vector Table 49
Table 6.2-10 Vector Table Format 49
Table 6.3-1 Peripheral Clock Source Selection Table 81

1 GENERAL DESCRIPTION

The NuMicro® NDA102 series 32-bit microcontrollers are embedded with ARM® Cortex®-M0 core for industrial applications which need high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NDA102 series can run up to 48 MHz and operate at 2.1V ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NDA102 offers 29.5 Kbytes embedded program Flash, size configurable Data Flash (shared with program Flash), 2 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 4 Kbytes SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NDA102 to reduce component count, board space and system cost. These useful functions make the NDA102 powerful for a wide range of applications.

Additionally, the NDA102 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.1V to 5.5V
- Memory
  - 29.5 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM)
  - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - ◆ Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25℃, 5V)
    - ◆ Dynamically calibrating the HIRC OSC to 48 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 22 general-purpose I/O (GPIO) pins and 1 Reset pin for QFN-33 package
  - Four I/O modes:
    - ◆ Quasi-bidirectional input/output
    - ◆ Push-Pull output
    - ◆ Open-Drain output
    - ◆ Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode

- Supports software selectable slew rate control
- GPIO built-in Pull-up/Pull-low resistor for selection

- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous operation modes
  - 24-bit up counter value is readable through CNT (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
  - Timer0, Timer1 and Systick provided with Continuous capture function to capture at most 4 edges continuously on one signal
- Continuous Capture
  - Timer0, Timer1 and Systick have support Continuous capture function can Continuous Capture 4 edge on one signal
- Enhanced Input Capture
  - One unit of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - PWM Trigger
    - ADC Trigger
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- PWM
  - Supports a built-in 16-bit PWM clock generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Supports Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control

- Hardware fault brake and software brake protections
- Supports rising, falling, central, period, and fault break interrupts
- Supports duty/period trigger A/D conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function

- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - Supports to be configured as UART, SPI or I²C individually
  - Supports programmable baud-rate generator
- ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 700 kSPS
  - Supports 2 sample/hold
  - Up to 8-ch single-end input from I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Supports temperature sensor for measurement chip temperature
  - Supports Simultaneous and Sequential function to continuous conversion 4 channels maximum.
- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13
  - Unity gain frequency up to 8 MHz
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming) and ICP (In-Circuit Programming)

- BOD (Brown-out Detector)
  - 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 28-pin TSSOP

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
DAP	Debug Access Port
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NDA102 Naming Rule

Figure 4.1-1 NuMicro® NDA102 Series Selection Code

4.2 NuMicro® NDA102 Series Selection Guide

* USCI can be set to UART, SPI or I^2C

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity	Comp.	PWM	ADC	PGA	ISP ICP IAP	IRC 10 kHz 48 MHz	Package
							USCI*							
NDA102EC1	29.5 KB	4 KB	Configurable	2.5 KB	up to 22	2x32-bit	2	2	8	8x12-bit	v	v	v	TSSOP28

Table 4.2-1 NuMicro® NDA102 Series Selection Guide

4.3 Pin Configuration

4.3.1 TSSOP 28-Pin

Figure 4.3-1 NuMicro® NDA102 Series TSSOP 28-pin Diagram

Figure 4.3-2 NuMicro® NDA102 Series TSSOP 28-pin Multi-function Diagram

4.4 Pin Description

4.4.1 NDA102 Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

MFP only configures the ouput data or input data of PAD; the direction of PAD is configured by PMD.

The priority of MFP in the same multi-function was GPA > GPB > GPC > GPD.

The type A of multi-function needs to be configured to be input port.

4.4.1.1 NDA102 Series TSSOP28 Pin Description

Pin No.	Pin Name	Type	MFP*	Description
1	V_{DD}	A	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
2	PD.6	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
3	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP2	ADC0 channel0 analog input.
	ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
4	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP2	ADC0 channel1 analog input.
	ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P1	I	MFP7	Enhanced Input Capture input pin
5	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP2	ADC0 channel2 analog input.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P2	I	MFP7	Enhanced Input Capture input pin
6	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH0	A	MFP2	ADC1 channel0 analog input.
	ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
	TM1	I/O	MFP7	Timer1 event counter input / toggle output
7	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP2	ADC0 channel4 analog input.

Pin No.	Pin Name	Type	MFP*	Description
	STADC	I	MFP3	ADC external trigger input.
	ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.
	ACMP1_P1	A	MFP5	Analog comparator1 positive input pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
8	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
9	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_N	A	MFP5	Analog comparator1 negative input pin.
	PGA_I	A	MFP6	PGA input pin
	TM0	I/O	MFP7	Timer0event counter input / toggle output
10	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH2	A	MFP2	ADC1 channel2 analog input.
	BRAKE	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
11	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	ADC1_CH1	A	MFP2	ADC1 channel1 analog input.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
12	PD.3	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
13	NC			No Connection
14	NC			No Connection
15	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel3 analog input.

Pin No.	Pin Name	Type	MFP*	Description
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
16	PD.4	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
17	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin
	ACMP1_P2	A	MFP5	Analog comparator1 positive input pin.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
18	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_O	O	MFP5	Analog comparator1 output.
	PGA_O	A	MFP6	PGA output pin
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
19	PD.5	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
20	PA.5	I/O	MFP0	General purpose digital I/O pin.
	XT_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
21	PA.4	I/O	MFP0	General purpose digital I/O pin.
	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.
22	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.

Pin No.	Pin Name	Type	MFP*	Description
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
23	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
24	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
25	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
26	PC.4	I/O	MFP0	General purpose digital I/O pin.
	ECAP_P3	I	MFP7	Enhanced Input Capture input pin
27	LDO_CAP	A	MFP0	LDO output pin.
28	V_{SS}	A	MFP0	Ground pin for digital circuit.

Table 4.4-1 TSSOP28 Pin Description

4.4.2 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_P0	PB.0	MFP4	A	Comparator0 positive input pin.
	ACMP0_P1	PB.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_P2	PB.2	MFP4	A	Comparator0 positive input pin.
	ACMP0_N	PB.4	MFP4	A	Comparator0 negative input pin.
	ACMP0_P3	PC.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_O	PA.5	MFP4	O	Comparator0 output pin.
ACMP1	ACMP1_P1	PC.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_N	PB.3	MFP5	A	Comparator1 negative input pin.
	ACMP1_O	PC.3	MPF5	O	Comparator1 output pin.
	ACMP1_P2	PD.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_P0	PC.0	MFP5	A	Comparator1 positive input pin.
ADC0	ADC0_CH0	PB.0	MFP2	A	ADC0 analog input channel 0.
	ADC0_CH1	PB.1	MFP2	A	ADC0 analog input channel 1.
	ADC0_CH2	PB.2	MFP2	A	ADC0 analog input channel 2.
	ADC0_CH4	PC.1	MFP2	A	ADC0 analog input channel 4.
	ADC0_CH3	PC.0	MFP2	A	ADC0 analog input channel 3.
ADC1	ADC1_CH0	PB.4	MFP2	A	ADC1 analog input channel 0.
	ADC1_CH2	PC.2	MFP2	A	ADC1 analog input channel 2.
	ADC1_CH1	PD.2	MFP2	A	ADC1 analog input channel 1.
BPWM	BPWM_CH1	PB.2	MFP3	O	Basic PWM channel 1 output
	BPWM_CH0	PC.0	MFP3	O	Basic PWM channel 0 output
	BPWM_CH1	PD.3	MFP3	O	Basic PWM channel 1 output
	BPWM_CH0	PD.4	MFP3	O	Basic PWM channel 0 output
CCAP	CCAP_P1	PC.2	MFP7	I	Continuous Capture Input
	CCAP_P0	PD.2	MFP7	I	Continuous Capture Input
CLKO	CLKO	PA.0	MFP1	O	Clock output pin.
ECAP	ECAP_P0	PB.0	MFP7	I	Input capture channel 0
	ECAP_P1	PB.1	MFP7	I	Input capture channel 1
	ECAP_P2	PB.2	MFP7	I	Input capture channel 2

EPWM	BRAKE	PC.2	MFP3	I	EPWM brake pin.
	EPWM_CH5	PA.5	MFP3	O	Enhanced PWM output pin.
	EPWM_CH4	PA.4	MFP3	O	Enhanced PWM output pin.
	EPWM_CH3	PA.3	MFP3	O	Enhanced PWM output pin.
	EPWM_CH2	PA.2	MFP3	O	Enhanced PWM output pin.
	EPWM_CH1	PA.1	MFP3	O	Enhanced PWM output pin.
	EPWM_CH0	PA.0	MFP3	O	Enhanced PWM output pin.
I^2C	I2C1_SDA	PC.2	MFP8	I/O	I^2C1 data pin.
	I2C0_SDA	PD.2	MFP8	I/O	I^2C0 data pin.
	I2C0_SCL	PD.1	MFP8	I/O	I^2C0 clock pin.
	I2C1_SCL	PC.0	MFP8	I/O	I^2C1 clock pin.
	I2C0_SCL	PA.3	MFP8	I/O	I^2C0 clock pin.
	I2C0_SDA	PA.2	MFP8	I/O	I^2C0 data pin.
	I2C1_SDA	PA.1	MFP8	I/O	I^2C1 data pin.
	I2C1_SCL	PA.0	MFP8	I/O	I^2C1 clock pin.
ICE	ICE_DAT	PD.2	MFP1	I/O	Serial wired debugger data pin
	ICE_CLK	PD.1	MFP1	I	Serial wired debugger clock pin
nRESET	nRESET			I	External reset pin, internal pull-high.
PGA	PGA_I	PB.3	MFP6	A	PGA analog input pin.
	PGA_O	PC.3	MFP6	A	PGA analog output pin.
SPI0	SPI0_MOSI	PC.1	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PC.2	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	PD.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_CLK	PC.3	MFP9	I/O	SPI0 clock pin.
	SPI0_CLK	PD.1	MFP9	I/O	SPI0 clock pin.
	SPI0_SS	PC.0	MFP9	I	SPI0 slave selection pin.
	SPI0_CLK	PA.3	MFP9	I/O	SPI0 clock pin.
	SPI0_MOSI	PA.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PA.1	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_SS	PA.0	MFP9	I	SPI0 slave selection pin.
SPI1	SPI1_MISO	PC.1	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_MOSI	PC.2	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	PD.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_SS	PC.3	MFPA	I/O	SPI1 Slave Select

	SPI1_SS	PD.1	MFPA	I/O	SPI1 Slave Select
	SPI1_CLK	PC.0	MFPA	I/O	SPI1 clock pin.
	SPI1_SS	PA.3	MFPA	I	SPI1 slave selection pin.
	SPI1_MISO	PA.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	PA.1	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_CLK	PA.0	MFPA	I/O	SPI1 clock pin.
STADC	STADC	PC.1	MFP3	I	External ADC trigger input pin.
TM0	TM0	PB.3	MFP7	I	Timer0 event counter input / toggle output
TM1	TM1	PB.4	MFP7	I	Timer1 event counter input / toggle output
UART0	UART0_RXD	PD.2	MFPB	I	UART0 data receiver input pin.
	UART0_TXD	PD.1	MFPB	O	UART0 data transmitter output pin.
	UART0_TXD	PA.3	MFPB	O	UART0 data transmitter output pin.
	UART0_RXD	PA.2	MFPB	I	UART0 data receiver input pin.
	UART0_TXD	PD.5	MFPB	O	UART0 data transmitter output pin.
	UART0_RXD	PD.6	MFPB	I	UART0 data receiver input pin.
UART1	UART1_RXD	PC.2	MFPB	I	UART1 data receiver input pin.
	UART1_TXD	PC.0	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PA.1	MFPB	I	UART1 data receiver input pin.
	UART1_TXD	PA.0	MFPB	O	UART1 data transmitter output pin.
	UART1_TXD	PD.3	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PD.4	MFPB	I	UART1 data receiver input pin.
XT	XT_OUT	PA.5	MPF1	A	External crystal output pin.
	XT_IN	PA.4	MFP1	A	External crystal input pin.

Table 4.4-2 TSSOP28 Multi-function Pin Summary

5 BLOCK DIAGRAM

5.1 NuMicro® NDA102 Block Diagram

Figure 5.1-1 NuMicro® NDA102 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

6.1.1 Overview

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes – Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

Figure 6.1-1 Functional Block Diagram

6.1.2 Features

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (SCS_AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])

Figure 6.2-1 System Reset Resources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-5.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	0x001	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG 0	-	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])								
BODRSTEN (SYS_BODCTL[3])								
XTLEN (CLK_PWRCTL[1:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	0x1	-	-

HCLKSEL (CLK_CLKSEL0[1:0])	0x8	0x8	0x8	0x8	0x8	0x8	0x8	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-
XLTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-
LIRCSTB (CLK_STATUS[3])	0x0							
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-
WDT_CTL	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
ISPEN (FMC_ISPCTL[16])								
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[20:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET

voltage is lower than 0.2 V_{DD} and the state keeps longer than 16.8 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 36 us (glitch filter). The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-On Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF (SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF (SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the waveform of Power-On reset.

Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

Low Voltage Reset detects AV_{DD} during system operation. When the AV_{DD} voltage is lower than

V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-4 shows the Low Voltage Reset waveform.

Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN (SYS_BODCTL[0]) and BODVL (SYS_BODCTL[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BODEN, BODVL and BODRSTEN is set by Flash controller user configuration register CBODEN (CONFIG0[12]), CBOV (CONFIG0[15:13]) and CBORST (CONFIG0[12]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-Out Detector waveform.

Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF (SYS_RSTSTS[2]).

6.2.2.6 CPU Reset, CHIP Reset and SYSTEM Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST (SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS (FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG setting. User can set the CHIPRST (SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (FMC_ISPCTL[1]) will not be reloaded from CONFIG setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ (SCS_AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, SPI, ACMP, BOD and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

Figure 6.2-6 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.

2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.

3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.

4. If WDT clock source is selected as LIRC and LIRC is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt

LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
BPWM	ON	ON	Halt
EPWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
USCI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt
ECAP	ON	ON	Halt
HDIV	ON	ON	Halt
PGA	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, SPI, BOD, ACMP and GPIO

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN (CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear SYS_BODCTL[BODIF].
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
USCI UART	Incoming data wake-up	After software writes 1 to clear WKF (UUART_WKSTS[0]).

USCI SPI	SS transaction wake-up	After software writes 1 to clear WKF (USPI_WKSTS[0]).
USCI I^2C	Data toggle	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
ACMP	Comparator Power-down Wake-Up Interrupt	After software writes 1 to clear ACMPF0 (ACMP_STATUS[0]) and ACMPF1 (ACMP_STATUS[1]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.5V power for digital operation.
- A built-in capacitor for internal voltage regulator

The output of internal voltage regulator, LDO, does not require an external capacitor and doesn't bond out to external pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}).

Figure 6.2-7 NuMicro® NDA102 Series Power Architecture Diagram

6.2.5 System Memory Mapping

	NDA102EC1	
4 GB	Reserved	0xFFFF_FFFF | 0xE000_F000
	System Control	0xE000_EFFF 0xE000_E000
	Reserved	0xE000_E00F | 0x6002_0000
	Reserved	0x6001_FFFF 0x6000_0000
	Reserved	0x5FFF_FFFF | 0x5020_0000
	AHB	0x501F_FFFF 0x5000_0000
	Reserved	0x4FFF_FFFF | 0x4020_0000
	APB	0x401F_FFFF | 0x4000_0000
1 GB	Reserved	0x3FFF_FFFF | 0x2000_1000
	4 KB SRAM	0x2000_0FFF 0x2000_0000
0.5 GB	Reserved	0x1FFF_FFFF | 0x0000_7600
	29.5 KB on-chip Flash (NDA102)	0x0000_75FF | 0x0000_0000
0 GB		

System Control

System Control	0xE000_ED00	SCS_BA
External Interrupt Control	0xE000_E100	SCS_BA
System Timer Control	0xE000_E010	SCS_BA

AHB peripherals

FMC	0x5000_C000	FMC_BA
GPIO Control	0x5000_4000	GP_BA
Interrupt Multiplexer Control	0x5000_0300	INT_BA
Clock Control	0x5000_0200	CLK_BA
System Global Control	0x5000_0000	SYS_BA

APB peripherals

ECAP Control	0x401B_0000	ECAP_BA
USCI1 Control	0x4017_0000	USCI1_BA
BPWM Control	0x4014_0000	BPWM_BA
PGA Control	0x400F_0000	PGA_BA
ADC Control	0x400E_0000	ADC_BA
ACMP 0/1 Control	0x400D_0000	ACMP_BA
USCI0 Control	0x4007_0000	USCI0_BA
EPWM Control	0x4004_0000	EPWM_BA
Timer0/Timer1 Control	0x4001_0000	TMR01_BA
WDT Control	0x4000_4000	WDT_BA

Table 6.2-5 Memory Mapping Table

6.2.6 Register Protection

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check REGLCTL (SYS_REGLCTL [0]), “1” is protection disable, “0” is protection enable. Then user can update the target protected register value and then write any data to SYS_REGLCTL to enable register protection.

The protected registers are listed in Table 6.2-6.

Register	Bit	Description
SYS_IPRST0	[1] CPURST	Processor Core One-shot Reset (Write Protect)
	[0] CHIPRST	Chip One-shot Reset (Write Protect)
SYS_BODCTL	[15] LVREN	Low Voltage Reset Enable Control (Write Protect)
	[6] BODLPM	Brown-out Detector Low Power Mode (Write Protect)
	[4] BODRSTEN	Brown-out Reset Enable Control (Write Protect)
	[3:1] BODVL	Brown-out Detector Threshold Voltage Selection (Write Protect)
	[0] BODEN	Brown-out Detector Enable Control (Write Protect)
SYS_PORCTL	[15:0] POROFF	Power-on Reset Enable Control (Write Protect)
INT_NMICTL	[8] NMISELEN	NMI Interrupt Enable Control (Write Protected)
CLK_PWRCTL	[11:10] HXTGAIN	HXT Gain Control (Write Protect)
	[7] PDEN	System Power-down Enable Control (Write Protect)
	[5] PDWKIEN	Power-down Mode Wake-up Interrupt Enable Control (Write Protect)
	[4] PDWKDLY	Wake-up Delay Counter Enable Control (Write Protect)
	[3] LIRCEN	LIRC Enable Control (Write Protect)
	[2] HIRCEN	HIRC Enable Control (Write Protect)
	[1:0] XTLEN	XTL Enable Control (Write Protect)
CLK_APBCLK	[0] WDTCKEN	Watchdog Timer Clock Enable Control (Write Protect)
CLK_CLKSEL0	[4:3] STCLKSEL	Cortex®-M0 SysTick Clock Source Selection (Write Protect)
	[1:0] HCLKSEL	HCLK Clock Source Selection (Write Protect)
CLK_CLKSEL1	[1:0] WDTSEL	Watchdog Timer Clock Source Selection (Write Protect)
FMC_ISPCTL	[6] ISPFF	ISP Fail Flag (Write Protect)
	[5] LDUEN	LDROM Update Enable Control (Write Protect)
	[4] CFGUEN	CONFIG Update Enable Control (Write Protect)

	[3] APUEN	APROM Update Enable Control (Write Protect)
	[2] SPUEN	SPROM Update Enable Control (Write Protect)
	[1] BS	Boot Select (Write Protect)
	[0] ISPEN	ISP Enable Control (Write Protect)
FMC_ISPTRG	[0] ISPGO	ISP Start Trigger (Write Protect)
FMC_ISPSTS	[6] ISPFF	ISP Fail Flag (Write Protect)
TIMER0_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
TIMER1_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
WDT_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
	[7] WDTEN	Watchdog Timer Enable Control (Write Protect)
	[6] INTEN	Watchdog Timer Time-out Interrupt Enable Control (Write Protect)
	[4] WKEN	Watchdog Timer Time-out Wake-up Function Control (Write Protect)
	[1] RSTEN	Watchdog Timer Time-out Reset Enable Control (Write Protect)
	[0] RSTCNT	Reset Watchdog Timer Up Counter (Write Protect)

Table 6.2-6 Protected Registers

6.2.7 Memory Organization

6.2.7.1 Overview

The NuMicro® NDA102 series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown in Figure 6.2-8. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NDA102 series only supports little-endian data format.

Figure 6.2-8 NuMicro® NDA102 Flash, Security and Configuration Map

6.2.7.2 System Memory Map

The NDA102 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NDA102 series only supports little-endian data format.

The memory locations assigned to each on-chip controllers are shown in Table 6.2-7.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_75FF	FLASH_BA	FLASH Memory Space (29.5KB)
0x0010_0000 – 0x0010_07FF	LD_BA	Loader Memory Space (2 KB)
0x0020_0000 – 0x0020_01FF	SP0_BA	Security Program Memory 0 Space (0.5 KB)
0x0024_0000 – 0x0024_01FF	SP1_BA	Security Program Memory 1 Space (0.5 KB)
0x0028_0000 – 0x0028_01FF	SP2_BA	Security Program Memory 2 Space (0.5 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Control Register
APB Controllers Space (0x4000_0000 ~ 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4004_0000 – 0x4004_3FFF	EPWM_BA	Enhance PWM Control Registers
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator 0/1 Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	ADC Control Registers
0x400F_0000 – 0x400F_3FFF	PGA_BA	Programmable Gain Amplifier Control Register
0x4014_0000 – 0x4014_3FFF	BPWM_BA	Basic PWM Control Registers
0x4017_0000 – 0x4017_3FFF	USCI1_BA	USCI1 Control Registers
0x401B_0000 – 0x401B_3FFF	ECAP_BA	Enhanced Input Capture Timer Register
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Modules

6.2.7.3 SRAM Memory Organization

The NDA102 supports embedded SRAM with total 4 Kbytes size.

- Supports total 4 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

Figure 6.2-9 SRAM Block Diagram

6.2.8 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit cleared-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

An RTOS tick timer fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.

A high-speed alarm timer uses Core clock.

A variable rate alarm or signal timer – the duration range is dependent on the reference clock used and the dynamic range of the counter.

A simple counter can be used by software to measure task completion time.

An internal Clock Source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on read.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.8.1 System Timer Control Register Map

R: read only**, W:** write only**, R/W:** both read and write**, W&C:** write 1 to clear

Register	Offset	R/W	Description	Reset Value
SCS Base Address: **SCS_BA = 0xE000_E000**				
SYST_CTL	SCS_BA+0x10	R/W	SysTick Control and Status	0x0000_0004
SYST_RVR	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX
SYST_CVR	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

6.2.8.2 System Timer Control Register Description

SysTick Control and Status （SYST_CTL）

Register	Offset	R/W	Description	Reset Value
SYST_CTL	SCS_BA+0x10	R/W	SysTick Control and Status	0x0000_0004

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							**COUNTFLAG**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**CLKSRC**	**TICKINT**	**ENABLE**

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**COUNTFLAG**	**System Tick Counter Flag** Return 1 If Timer Counted to 0 Since Last Time this Register Was Read 0 = COUNTFLAG is cleared on read or by a write to the Current Value register. 1 = COUNTFLAG is set by a count transition from 1 to 0.
[15:3]	**Reserved**	Reserved.
[2]	**CLKSRC**	**System Tick Clock Source Select Bit** 0 = Clock source is optional, refer to STCLKSEL. 1 = Core clock used for SysTick timer.
[1]	**TICKINT**	**System Tick Interrupt Enable Bit** 0 = Counting down to 0 will not cause the SysTick exception to be pended. User can use COUNTFLAG to determine if a count to zero has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick Current Value register by a register write in software will not cause SysTick to be pended.
[0]	**ENABLE**	**System Tick Counter Enable Bit** 0 = System Tick counter Disabled. 1 = System Tick counter will operate in a multi-shot manner.

SysTick Reload Value Register (SYST_RVR）

Register	Offset	R/W	Description	Reset Value
SYST_RVR	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RELOAD							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RELOAD							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RELOAD							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**RELOAD**	**System Tick Reload Value** Value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register （SYST_CVR）

Register	Offset	R/W	Description	Reset Value
SYST_CVR	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CURRENT							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CURRENT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURRENT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

6.2.9 Nested Vectored Interrupt Control (NVIC)

6.2.9.1 Overview

The Cortex®-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features.

6.2.9.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.9.3 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by the NDA102 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as 0 and the lowest priority is denoted as 3. The default priority of all the user-configurable interrupts is 0. Note that the priority 0 is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	**BOD_OUT**	Brown-Out low voltage detected interrupt
17	1	**WDTPINT**	Watchdog Timer interrupt
18	2	**USCI0**	USCI0 interrupt
19	3	**USCI1**	USCI1 interrupt
20	4	**GP_INT**	External interrupt from GPA ~ GPD pins
21	5	**EPWM_INT**	EPWM interrupt
22	6	**BRAKE0_INT**	EPWM brake interrupt from PWM0 or PWM_BRAKE pin
23	7	**BRAKE1_INT**	EPWM brake interrupt from PWM1
24	8	**BPWM0_INT**	BPWM0 interrupt
25	9	**BPWM1_INT**	BPWM1 interrupt
26	10	Reserved	Reserved
27	11	Reserved	Reserved
28	12	Reserved	Reserved
29	13	Reserved	Reserved
30	14	Reserved	Reserved
31	15	**ECAP_INT**	Enhanced Input Capture interrupt
32	16	**CCAP_INT**	Continues Input Capture interrupt
33	17	Reserved	Reserved

34	18	Reserved	Reserved
35	19	Reserved	Reserved
36	20	Reserved	Reserved
37	21	**HIRCTRIM_INT**	HIRC TRIM interrupt
38	22	**TMR0_INT**	Timer 0 interrupt
39	23	**TMR1_INT**	Timer 1 interrupt
40	24	Reserved	Reserved
41	25	Reserved	Reserved
42	26	**ACMP_INT**	Analog Comparator 0 or Comparator 1 interrupt
43	27	Reserved	Reserved
44	28	**PWRWU_INT**	Chip wake-up from Power-down state interrupt
45	29	**ADC0_INT**	ADC0 interrupt
46	30	**ADC1_INT**	ADC1 interrupt
47	31	**ADCWCMP_INT**	ADC Window Compare interrupt

Table 6.2-9 System Interrupt Map Vector Table

6.2.9.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-10 Vector Table Format

6.2.9.5 Operation Description

The NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used

to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.9.6 NVIC Control Registers Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCS Base Address: **SCS_BA = 0xE000_E000**				
NVIC_ISER	SCS_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-Enable Control Register	0x0000_0000
NVIC_ICER	SCS_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-Enable Control Register	0x0000_0000
NVIC_ISPR	SCS_BA+0x200	R/W	IRQ0 ~ IRQ31 Set-Pending Control Register	0x0000_0000
NVIC_ICPR	SCS_BA+0x280	R/W	IRQ0 ~ IRQ31 Clear-Pending Control Register	0x0000_0000
NVIC_IPR0	SCS_BA+0x400	R/W	IRQ0 ~ IRQ3 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR1	SCS_BA+0x404	R/W	IRQ4 ~ IRQ7 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR2	SCS_BA+0x408	R/W	IRQ8 ~ IRQ11 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR3	SCS_BA+0x40C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR4	SCS_BA+0x410	R/W	IRQ16 ~ IRQ19 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR5	SCS_BA+0x414	R/W	IRQ20 ~ IRQ23 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR6	SCS_BA+0x418	R/W	IRQ24 ~ IRQ27 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR7	SCS_BA+0x41C	R/W	IRQ28 ~ IRQ31 Interrupt Priority Control Register	0x0000_0000

IRQ0 ~ IRQ31 Set-enable Control Register (NVIC_ISER)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER	SCS_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-Enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Enable Register** Enable one or more interrupts. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Write operation: 0 = No effect. 1 = Write 1 to enable associated interrupt. Read operation: 0 = Associated interrupt status Disabled. 1 = Associated interrupt status Enabled. Read value indicates the current enable status.

IRQ0 ~ IRQ31 Clear-enable Control Register (NVIC_ICER)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER	SCS_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-Enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CLRENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLRENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLRENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLRENA							

Bits	Description	
[31:0]	**CLRENA**	**Interrupt Disable Register** Disable one or more interrupts. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Write operation: 0 = No effect. 1 = Write 1 to disable associated interrupt. Read operation: 0 = Associated interrupt status Disabled. 1 = Associated interrupt status Enabled. **Note:** Read value indicates the current enable status.

IRQ0 ~ IRQ31 Set-pending Control Register (NVIC_ISPR)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR	SCS_BA+0x200	R/W	IRQ0 ~ IRQ31 Set-Pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Set Interrupt Pending Register** Write operation: 0 = No effect. 1 = Write 1 to set pending state. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Read operation: 0 = Associated interrupt in not in pending status. 1 = Associated interrupt is in pending status. **Note:** Read value indicates the current pending status.

IRQ0 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR	SCS_BA+0x280	R/W	IRQ0 ~ IRQ31 Clear-Pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CLRPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLRPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLRPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLRPEND							

Bits	Description	
[31:0]	**CLRPEND**	**Clear Interrupt Pending Register** Write operation: 0 = No effect. 1 = Write 1 to clear pending state. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Read operation: 0 = Associated interrupt in not in pending status. 1 = Associated interrupt is in pending status. **Note:** Read value indicates the current pending status.

IRQ0 ~ IRQ3 Interrupt Priority Register (NVIC_IPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR0	SCS_BA+0x400	R/W	IRQ0 ~ IRQ3 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_3		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_2		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_1		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_0		**Reserved**					

Bits	Description	
[31:30]	**PRI_3**	**Priority of IRQ3** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_2**	**Priority of IRQ2** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_1**	**Priority of IRQ1** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_0**	**Priority of IRQ0** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ4 ~ IRQ7 Interrupt Priority Register (NVIC_IPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR1	SCS_BA+0x404	R/W	IRQ4 ~ IRQ7 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_7		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_6		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_5		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4		**Reserved**					

Bits	Description	
[31:30]	**PRI_7**	**Priority of IRQ7** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_6**	**Priority of IRQ6** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_5**	**Priority of IRQ5** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4**	**Priority of IRQ4** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ8 ~ IRQ11 Interrupt Priority Register (NVIC_IPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR2	SCS_BA+0x408	R/W	IRQ8 ~ IRQ11 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_10		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_9		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_8		**Reserved**					

Bits	Description	
[31:30]	**PRI_11**	**Priority of IRQ11** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_10**	**Priority of IRQ10** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_9**	**Priority of IRQ9** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_8**	**Priority of IRQ8** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ12 ~ IRQ15 Interrupt Priority Register (NVIC_IPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR3	SCS_BA+0x40C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_13		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_12		**Reserved**					

Bits	Description	
[31:30]	**PRI_15**	**Priority of IRQ15** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of IRQ14** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_13**	**Priority of IRQ13** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_12**	**Priority of IRQ12** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ16 ~ IRQ19 Interrupt Priority Register (NVIC_IPR4)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR4	SCS_BA+0x410	R/W	IRQ16 ~ IRQ19 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_19		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_18		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_17		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_16		**Reserved**					

Bits	Description	
[31:30]	**PRI_19**	**Priority of IRQ19** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_18**	**Priority of IRQ18** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_17**	**Priority of IRQ17** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_16**	**Priority of IRQ16** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ20 ~ IRQ23 Interrupt Priority Register (NVIC_IPR5)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR5	SCS_BA+0x414	R/W	IRQ20 ~ IRQ23 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_23		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_22		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_21		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_20		**Reserved**					

Bits	Description	
[31:30]	**PRI_23**	**Priority of IRQ23** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_22**	**Priority of IRQ22** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_21**	**Priority of IRQ21** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_20**	**Priority of IRQ20** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ24 ~ IRQ27 Interrupt Priority Register (NVIC_IPR6)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR6	SCS_BA+0x418	R/W	IRQ24 ~ IRQ27 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_27		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_26		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_25		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_24		**Reserved**					

Bits	Description	
[31:30]	**PRI_27**	**Priority of IRQ27** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_26**	**Priority of IRQ26** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_25**	**Priority of IRQ25** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_24**	**Priority of IRQ24** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

IRQ28 ~ IRQ31 Interrupt Priority Register (NVIC_IPR7)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR7	SCS_BA+0x41C	R/W	IRQ28 ~ IRQ31 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_31		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_30		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_29		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_28		**Reserved**					

Bits	Description	
[31:30]	**PRI_31**	**Priority of IRQ31** 0 denotes the highest priority and 3 denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_30**	**Priority of IRQ30** 0 denotes the highest priority and 3 denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_29**	**Priority of IRQ29** 0 denotes the highest priority and 3 denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_28**	**Priority of IRQ28** 0 denotes the highest priority and 3 denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

6.2.9.7 *Interrupt Source Control Registers*

Besides the interrupt control registers associated with the NVIC, the NDA102 series also implements some specific control registers to facilitate the interrupt functions, including ”NMI source selection” and “IRQ number identity”, which are described below.

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
INT Base Address: **INT_BA = 0x5000_0300**				
INT_NMICTL	INT_BA+0x80	R/W	NMI Source Interrupt Select Control Register	0x0000_0000
INT_IRQSTS	INT_BA+0x84	R/W	MCU IRQ Number Identity Register	0x0000_0000

NMI Interrupt Source Select Control Register (INT_NMICTL)

Register	Offset	R/W	Description	Reset Value
INT_NMICTL	INT_BA+0x80	R/W	NMI Source Interrupt Select Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**NMISELEN**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**NMISEL**				

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8]	**NMISELEN**	**NMI Interrupt Enable Bit (Write Protected)** 0 = NMI interrupt Disabled. 1 = NMI interrupt Enabled. **Note:** This bit is the protected bit, and programming it needs to write 0x59, 0x16, and 0x88 to address 0x5000_0100 to disable register protection. Refer to the register SYS_REGLCTL at address SYS_BA+0x100.
[7:5]	**Reserved**	Reserved.
[4:0]	**NMISEL**	**NMI Interrupt Source Selection** The NMI interrupt to Cortex®-M0 can be selected from one of the peripheral interrupt by setting NMTSEL.

MCU Interrupt Request Source Register (INT_IRQSTS)

Register	Offset	R/W	Description	Reset Value
INT_IRQSTS	INT_BA+0x84	R/W	MCU IRQ Number Identity Register	0x0000_0000

31	30	29	28	27	26	25	24
IRQ							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IRQ							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IRQ							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IRQ							

Bits	Description	
[31:0]	**IRQ**	**MCU IRQ Source Register** The IRQ collects all the interrupts from the peripherals and generates the synchronous interrupt to Cortex®-M0 core. There is one mode to generate interrupt to Cortex®-M0 - the normal mode. The IRQ collects all interrupts from each peripheral and synchronizes them then interrupts the Cortex®-M0. When the IRQ[n] is 0, setting IRQ[n] to 1 will generate an interrupt to Cortex®-M0 NVIC[n]. When the IRQ[n] is 1 (i.e. an interrupt is assert), setting 1 to the MCU_bit[n] will clear the interrupt and setting IRQ[n] 0 has no effect.

6.2.10 System Control Registers

Key control and status features of Cortex®-M0 are managed centrally in a System Control Block within the System Control Registers.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.10.1 System Control Register Memory Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCS Base Address: **SCS_BA = 0xE000_E000**				
SCS_CPUID	SCS_BA+0xD00	R	CPUID Base Register	0x410C_C200
SCS_ICSR	SCS_BA+0xD04	R/W	Interrupt Control State Register	0x0000_0000
SCS_AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCS_SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SCS_SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SCS_SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

6.2.10.2 System Control Register Description

CPUID Base Register (CPUID)

Register	Offset	R/W	Description	Reset Value
SCS_CPUID	SCS_BA+0xD00	R	CPUID Base Register	0x410C_C200

31	30	29	28	27	26	25	24
IMPLEMENTER							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved				**PART**			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PARTNO							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PARTNO				**REVISION**			

Bits	Description	
[31:24]	**IMPLEMENTER**	**Implementer Code** Implementer code assigned by ARM (ARM = 0x41).
[23:20]	**Reserved**	Reserved.
[19:16]	**PART**	**Architecture of the Processor** Reads as 0xC for ARMv6-M parts
[15:4]	**PARTNO**	**Part Number of the Processor** Reads as 0xC20.
[3:0]	**REVISION**	**Revision Number** Reads as 0x0

Interrupt Control State Register (ICSR)

Register	Offset	R/W	Description	Reset Value
SCS_ICSR	SCS_BA+0xD04	R/W	Interrupt Control State Register	0x0000_0000

31	30	29	28	27	26	25	24
NMIPENDSET	**Reserved**		**PENDSVSET**	**PENDSVCLR**	**PENDSTSET**	**PENDSTCLR**	**Reserved**
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISRPREEMPT	**ISRPENDING**	**Reserved**	**VECTPENDING**				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
VECTPENDING				**Reserved**			**VECTACTIVE**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VECTACTIVE							

Bits	Description	
[31]	**NMIPENDSET**	**NMI Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes NMI exception state to pending. Read Operation: 0 = NMI exception not pending. 1 = NMI exception pending. **Note:** Because NMI is the highest-priority exception, normally the processor entersthe NMI exception handler as soon as it detects a write of 1 to this bit. Entering thehandler then clears this bit to 0. This means a read of this bit by the NMI exceptionhandler returns 1 only if the NMI signal is reasserted while the processor is executingthat handler.
[30:29]	**Reserved**	Reserved.
[28]	**PENDSVSET**	**PendSV Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note:** Writing 1 to this bit is the only way to set the PendSV exception state to pending
[27]	**PENDSVCLR**	**PendSV Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the PendSV exception. This bit is write-only. To clear the PENDSV bit, you must “write 0 to PENDSVSET andwrite 1 to PENDSVCLR” at the same time.
[26]	**PENDSTSET**	**SysTick Exception Set-pending Bit**

		Write Operation: 0 = No effect. 1 = Changes SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	**PENDSTCLR**	**SysTick Exception Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the SysTick exception. **Note:** This bit is write-only. When you want to clear PENDST bit, you must "write 0 toPENDSTSET and write 1 to PENDSTCLR" at the same time.
[24]	**Reserved**	Reserved.
[23]	**ISRPREEMPT**	**Interrupt Preempt Bit(Read Only)** If set, a pending exception will be serviced on exit from the debug halt state
[22]	**ISRPENDING**	**Interrupt Pending Flag,Excluding NMI and Faults (Read Only)** 0 = Interrupt not pending. 1 = Interrupt pending.
[21]	**Reserved**	Reserved.
[20:12]	**VECTPENDING**	**Exception Number of the Highest Priority Pending Enabled Exception** 0 = No pending exceptions. Non-zero = Exception number of the highest priority pending enabled exception.
[11:9]	**Reserved**	Reserved.
[8:0]	**VECTACTIVE**	**Contains the Active Exception Number** 0 = Thread mode. Non-zero = Exception number of the currently active exception.

Application Interrupt and Reset Control Register (AIRCR)

Register	Offset	R/W	Description	Reset Value
SCS_AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

31	30	29	28	27	26	25	24
VECTORKEY							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VECTORKEY							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**SYSRESETREQ**	**VECTCLRACTIVE**	**Reserved**

Bits	Description	
[31:16]	**VECTORKEY**	**Register Access Key** Write Operation: When writing to this register, the VECTORKEY field need to be set to 0x05FA, otherwise the write operation would be ignored. The VECTORKEY filed is used to prevent accidental write to this register from resetting the system or clearing of the exception status. Read Operation: Read as 0xFA05.
[15:3]	**Reserved**	Reserved.
[2]	**SYSRESETREQ**	**System Reset Request** Writing this bit 1 will cause a reset signal to be asserted to the chip to indicate a reset is requested. The bit is a write only bit and self-clears as part of the reset sequence.
[1]	**VECTCLRACTIVE**	**Exception Active Status Clear Bit** Reserved for debug use. When writing to the register, user must write 0 to this bit, otherwise behavior is unpredictable.
[0]	**Reserved**	Reserved.

System Control Register (SCR)

Register	Offset	R/W	Description	Reset Value
SCS_SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**SEVONPEND**	**Reserved**	**SLEEPDEEP**	**SLEEPONEXIT**	**Reserved**

Bits	Description	
[31:5]	**Reserved**	Reserved.
[4]	**SEVONPEND**	**Send Event on Pending Bit** 0 = Only enabled interrupts or events can wake-up the processor, disabled interrupts areexcluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake-up theprocessor. When an event or interrupt enters pending state, the event signal wakes up the processorfrom WFE. If the processor is not waiting for an event, the event is registered and affectsthe next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	**Reserved**	Reserved.
[2]	**SLEEPDEEP**	**Processor Deep Sleep and Sleep Mode Selection** Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = Sleep mode. 1 = Deep Sleep mode.
[1]	**SLEEPONEXIT**	**Sleep-on-exit Enable Bit** This bit indicates sleep-on-exit when returning from Handler mode to Thread mode. 0 = Do not sleep when returning to Thread mode. 1 = Enter Sleep or Deep Sleep when returning from ISR to Thread mode.Setting this bit to 1 enables an interrupt driven application to avoid returning to an emptymain application.
[0]	**Reserved**	Reserved.

System Handler Priority Register 2 (SHPR2)

Register	Offset	R/W	Description	Reset Value
SCS_SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_11**	**Priority of System Handler 11 – SVCall** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SCS_SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_15**	**Priority of System Handler 15 – SysTick** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of System Handler 14 – PendSV** "0" denotes the highest priority and "3" denotes the lowest priority.
[21:0]	**Reserved**	Reserved.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when the Cortex®-M0 core executes the WFI instruction only if the PDEN (CLK_PWRCTL[7]) bit set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-2 shows the clock generator and the overview of the clock source control.

The clock generator consists of 4 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Figure 6.3-1 Clock Generator Block Diagram

Figure 6.3-2 Clock Generator Global View Diagram

6.3.2 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 48MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL[0] trim frequency selection) to “1”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

6.3.3 System Clock and SysTick Clock

The system clock has three clock sources which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[1:0]). The block diagram is shown in Figure 6.3-3.

Figure 6.3-3 System Clock Block Diagram

The clock source of SysTick in the Cortex®-M0 core can use CPU clock or external clock CLKSRC(SYST_CTL[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[4:3]). The block diagram is shown in Figure 6.3-4.

Figure 6.3-4 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLK_CLKSEL1 and CLK_APBCLK register description in TRM. Please note that, while switching clock source from one to another, user must wait until both clock sources are running stabled.

Figure 6.3-5 Peripherals Bus Clock Source Selection for PCLK

	Peripheral Clock Selectable	Ext. CLK (HXT Or LXT)	HIRC	LIRC	HCLK
WDT	Yes	Yes	No	Yes	Yes
WWDT	Yes	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes	Yes
USCI0	Yes	Yes	Yes	Yes	Yes
USCI1	Yes	Yes	Yes	Yes	Yes
ADC	Yes	Yes	Yes	No	Yes
ACMP	No	No	No	No	Yes
ECAP	No	No	No	No	Yes
EBWM	No	No	No	No	Yes
BPWM	No	No	No	No	Yes
HDIV	No	No	No	No	Yes

Table 6.3-1 Peripheral Clock Source Selection Table

Note: For the peripherals those peripheral clock are not selectable, its clock source is fixed to PCLK.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one

multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIV1EN(CLK_CLKOCTL[5]) set to 1, the frequency divider clock will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

Figure 6.3-6 Clock Source of Frequency Divider

Figure 6.3-7 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NDA102 series is equipped with 29.5 Kbytes on chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NDA102 series also provides Data Flash Region, where the Data Flash is shared with original program memory and its start address is configurable and defined by user in Config1. The Data Flash size is defined by user depending on the application request. Security program memory (SPROM) provides user to protect any program code within SPROM.

6.4.2 Features

- Running up to 48 MHz with one wait state and 24 MHz without wait state for discontinuous address read access
- 29.5 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable Data Flash start address and memory size with 512 bytes page erase unit
- Three 512 bytes security program memory (SPROM)
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NDA102 series has up to 22 General Purpose I/O pins. These pins could be shared with other functions depending on the chip configuration. 22 pins are arranged in 4 ports named as PA, PB, PC, and PD. Each of the 22 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.0 V to 2.5 V.

Figure 6.5-1 I/O Pin Block Diagram

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting

- Supports High Drive and High Sink I/O mode
- Supports software selectable slew rate control
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOIN = 1, all GPIO pins in input mode after chip reset
- GPIOA supports the pull-up and pull-low resistor enabled in four I/O modes
- GPIOB to GPIOD internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.5.3 GPIO Interrupt and Wake-up Function

Each GPIO pin can be set as chip interrupt source by setting correlative RHIEN (Px_INTEN[n+16])/ FLIEN (Px_INTEN[n]) bit and TYPE (Px_INTTYPE[n]). There are five types of interrupt conditions to be selected: low level trigger, high level trigger, falling edge trigger, rising edge trigger and both rising and falling edge trigger. For edge trigger condition, user can enable input signal de-bounce function to prevent unexpected interrupt happened which caused by noise. The de-bounce clock source and sampling cycle period can be set through DBCLKSRC (GPIO_DBCTL[4]) and DBCLKSEL (GPIO_DBCTL[3:0]) register.

The GPIO can also be the chip wake-up source when chip enters Idle/Power-down mode. The setting of wake-up trigger condition is the same as GPIO interrupt trigger.

1. To ensure the I/O status before entering Idle/Power-down mode

When using toggle GPIO to wake-up system, user must make sure the I/O status before entering Idle/Power-down mode according to the relative wake-up settings.

For example, if configuring the wake-up event occurred by I/O rising edge/high level trigger, user must make sure the I/O status of specified pin is at low level before entering Idle/Power-down mode; and if configuring I/O falling edge/low level trigger to trigger a wake-up event, user must make sure the I/O status of specified pin is at high level before entering Power-down mode.

2. To disable the I/O de-bounce function before entering Idle/Power-down mode

If the specified wake-up I/O pin with enabling input signal de-bounce function, system will encounter two GPIO interrupt events while the system is woken up by this GPIO pin. One interrupt event is caused by wake-up function, the other is caused by I/O input de-bounce function. User should be disable the de-bounce function before entering Idle/Power-down mode to avoid the second interrupt event occurred after system woken up.

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Supports two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Supports independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Supports four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit CMPDAT)
- Supports maximum counting cycle time = (1 / T MHz) * (28) * (224); T is the period of timer clock
- 24-bit up counter value is readable through TIMERx_CNT (Timer Data Register)
- Supports event counting function to count the event from external pin (TM0, TM1)
- Supports internal capture triggered while internal ACMP output signal transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.7 Enhanced Input Capture Timer (ECAP)

6.7.1 Overview

This device provides an Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. This unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.7.2 Features

- 24-bit Input Capture up-counting timer/counter.
- 3 input channels thatl has its own capture counter hold register.
- Noise filter in front end of input ports.
- Edge detector with three options.
  - Rising edge detection.
  - Falling edge detection.
  - Both edge detection.
- Supports ADC compare output and ACMP output as input sources
- Captured events reset and/or reload capture counter.
- Supports compare-match function.
- Supports interrupt function.

6.8 Enhanced PWM Generator (EPWM)

6.8.1 Overview

The NDA102 series has built in one PWM unit which is specially designed for motor driving control applications. The PWM unit supports six PWM generators which can be configured as six independent PWM outputs, PWM0~PWM5, or as three complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with three programmable dead-zone generators.

Every complementary PWM pairs share one clock divider providing nine divided frequencies (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256) for each channel. Each PWM output shares one 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide fourteen independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period up counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit counter/comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. To control motor more precisely, some registers are provided to configure not only PWM but also Timer, ADC and ACMP. By doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.8.2 Features

- Supports one PWM clock timer and one 9 level Divider (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256).
- Supports six independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
  - Three synchronous PWM pairs, with each pin in a pair in-phase – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Supports group function.
- Supports one-shot (only edge alignment mode) or auto-reload mode PWM
- Supports 16-bit resolution PWM counter
- Supports Edge-aligned and Center-aligned mode
- Supports Programmable dead-zone insertion between complementary paired PWMs
- Supports hardware fault brake protections
  - Two Interrupt source types:
    - one type is brake directed, and one type can resume from brake.
    - fault brake source:

- BRK0: ACMP0, ACMP1, EADC and External pin (BRAKE).
- BRK1: ACMP0, ACMP1, EADC and External pin (BRAKE).

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- Supports independently falling CMPDAT matching, central matching (in Center-aligned mode), rising CMPDAT matching (in Center-aligned mode), period matching to trigger EADC conversion
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Supports interrupt accumulation function

6.9 Basic PWM Generator (BPWM)

6.9.1 Overview

The NDA102 series has one set of BPWM group supporting one set of PWM generator that can be configured as 2 independent PWM outputs, BPWM CH0~BPWM CH1, or as 1 complementary PWM pairs, (BPWM CH0, BPWM CH1) with programmable Dead-zone generators.

The PWM generator has one 8-bit pre-scalar, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generator provides two independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DTCNT01(BPWM_CTL[4]) is set, BPWM CH0 and BPWM CH1 perform complementary; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0.

To prevent PWM driving output pin from glitches, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with BPWM Counter Register(BPWM_PERIODx, x=0,1) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

6.9.2 Features

- One PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (24 ~ 218) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.11 USCI – Universal Serial Control Interface Controller

6.11.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

Note: For detailed USCI UART, I^2C and SPI information, please refer to section 6.12, 6.13 and 6.14.

6.11.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

To increase readability, the registers of USCI have different alias names that depending on the selected protocol. For example, register USCI_CTL has alias name UUART_CTL for protocol UART, has alias name USPI_CTL for protocol SPI, and has alias name UI2C_CTL for protocol I^2C.

6.12 USCI – UART Mode

6.12.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, frames can start at different points in time for transmission and reception.

The UART controller also provides the LIN function. There is incoming data to wake up the system.

6.12.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports programmable baud-rate generator
- Supports 9-Bit Data Transfer
- Supports LIN function
- Supports baud rate detection by built-in capture event of baud rate generator
- Supports Wake-up function

6.13 USCI – SPI Mode

6.13.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1.

The SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown as Figure 6.13-1 and Figure 6.13-2.

Figure 6.13-1 SPI Master Mode Application Block Diagram (x=0, 1)

Figure 6.13-2 SPI Slave Mode Application Block Diagram (x=0, 1)

6.13.2 Features

- Supports master or slave mode operation (the maximum frequency for Master = f_{PCLK} / 2, for Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode

6.14 USCI – I²C Mode

6.14.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.14-1 for more detailed I²C BUS Timing.

Figure 6.14-1 I²C Bus Timing

The device on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 0100B. When this port is enabled, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: A pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.14.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable

6.15 Hardware Divider (HDIV)

6.15.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.15.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.16 Analog to Digital Converter (ADC)

6.16.1 Overview

The NDA102 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 single-end external input channels. The A/D converters can be started by software, external pin (STADC/PC.1) or PWM trigger.

6.16.2 Features

- Analog input voltage range: 0~V_{DD}.
- 12-bit resolution and 10-bit accuracy guaranteed.
- Up to 8 single-end analog input channels.
- ADC clock frequency up to 16MHz.
- Configurable ADC internal sampling time.

6.17 Analog Comparator (ACMP)

6.17.1 Overview

The NDA102 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.17.2 Features

- Analog input voltage range: 0 ~ V_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input

6.18 Programmable Gain Amplifier (PGA)

6.18.1 Overview

The NDA102 series contains a programmable gain amplifier (PGA) which can be enabled through the PGAEN bit. User can measure the outputs of the programmable gain amplifier as the programmable gain amplifier output to the integrated A/D converter channel, where digital results can be taken. Furthermore, user can adjust gain to 1, 2, 3, 5, 7, 9, 11, and 13.

Note: The analog input port pins must be configured as input type before the PGA function is enabled.

6.18.2 Features

- Supports analog input voltage range: 0~ V_{DD}.
- Supports programmable gain: 1,2, 3,5,7,9.11,13
- Supports PGA output as input of ADC and ACMP

7 APPLICATION CIRCUIT

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.1 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.1	-	5.5	V	V_{DD} = 2.1V ~ 5.5V up to 48 MHz			
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage		1.2		V	V_{DD} = 3.0V ~ 5.5V, T_A = -40°C~105°C			
I_{DD5}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	9.7	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD6}		-	7.4	-	mA	5.5V	X	48 MHz	X
I_{DD7}		-	9.7	-	mA	3V	X	48 MHz	V
I_{DD8}		-	7.4	-	mA	3V	X	48 MHz	X
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD2}		-	4.4	-	mA	5.5V	24 MHz	X	X
I_{DD3}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD4}		-	4.4	-	mA	3V	24 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.7	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD10}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD11}		-	3.7	-	mA	3V	16 MHz	X	V
I_{DD12}		-	3.1	-	mA	3V	16 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz	-	2.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V

I_{DD10}	while(1){} Executed from Flash	-	2.3	-	mA	5.5V	12 MHz	X	X
I_{DD11}		-	2.8	-	mA	3V	12 MHz	X	V
I_{DD12}		-	2.3	-	mA	3V	12 MHz	X	X
I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.2	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD14}		-	1.0	-	mA	5.5V	4 MHz	X	X
I_{DD15}		-	1.2	-	mA	3V	4 MHz	X	V
I_{DD16}		-	1.0	-	mA	3V	4 MHz	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	291.7	-	μA	V_{DD}	LXT	LIRC	All Digital Modules
						5.5V	32 kHz	V	V[1]
I_{DD18}		-	290.7	-	μA	5.5V	32 kHz	V	X
I_{DD19}		-	280.8	-	μA	3V	32 kHz	V	V[1]
I_{DD20}		-	281.4	-	μA	3V	32 kHz	V	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	248.0	-	μA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	10 kHz	V[2]
I_{DD18}		-	247.7	-	μA	5.5V	X	10 kHz	X
I_{DD19}		-	237.9	-	μA	3V	X	10 kHz	V[2]
I_{DD20}		-	237.5	-	μA	3V	X	10 kHz	X
I_{IDLE5}	Operating Current Idle Mode HCLK= 48 MHz	-	4.9	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE6}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE7}		-	4.9	-	mA	3V	X	V	V
I_{IDLE8}		-	2.6	-	mA	3V	X	V	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 24 MHz	-	2.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V

I_{IDLE2}		-	1.9	-	mA	5.5V	24 MHz	X	X
I_{IDLE3}		-	2.8	-	mA	3V	24 MHz	X	V
I_{IDLE4}		-	1.9	-	mA	3V	24 MHz	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 16 MHz	-	2.0	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE11}		-	2.0	-	mA	3V	V	X	V
I_{IDLE12}		-	1.4	-	mA	3V	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 12 MHz	-	1.5	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.0	-	mA	5.5V	V	X	X
I_{IDLE11}		-	1.5	-	mA	3V	V	X	V
I_{IDLE12}		-	1.0	-	mA	3V	V	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	0.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE14}		-	0.6	-	mA	5.5V	V	X	X
I_{IDLE15}		-	0.7	-	mA	3V	V	X	V
I_{IDLE16}		-	0.6	-	mA	3V	V	X	X
I_{DD17}	Operating Current Idle Mode HCLK = 32 kHz	-	274.3	-	μA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{DD18}		-	273.0	-	μA	5.5V	X	V	X
I_{DD19}		-	265.0	-	μA	3V	X	V	V[1]
I_{DD20}		-	263.9	-	μA	3V	X	V	X
I_{DD17}	Operating Current Idle Mode HCLK = 10 kHz	-	232.6	-	μA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]

I_{DD18}		-	232.2	-	μA	5.5V	X	V	X
I_{DD19}		-	222.5	-	μA	3V	X	V	V[2]
I_{DD20}		-	222.1	-	μA	3V	X	V	X
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	1.9	-	μA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD2}		-	1.7	-	μA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current PA/PB/PC/PD	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			
V_{IL1}	Input Low Voltage PA/PB/PC/PD (TTL Input)	-0.3	1.33		V	V_{DD} = 5.5 V			
		-0.3	1			V_{DD} = 3.3 V			
V_{IH1}	Input High Voltage PA/PB/PC/PD (TTL Input)		1.47	V_{DD} + 0.3	V	V_{DD} = 5.5 V			
			1.08	V_{DD} + 0.3		V_{DD} = 3.3 V			
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	0.3V_{DD}	V	-			
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	0.7V_{DD}	-	-	V	-			
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.1 V ~ 5.5V			
V_{ILS}	Negative-going Threshold (Schmitt input), PA/PB/PC/PD	-	-	0.3V_{DD}	V	-			
V_{IHS}	Positive-going Threshold (Schmitt input), PA/PB/PC/PD	0.7V_{DD}	-	-	V	-			
I_{IL}	Logic 0 Input Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-63.65		μA	V_{DD} = 5.5 V, V_{IN} = 0V			
I_{TL}	Logic 1 to 0 Transition Current PA/PB/PC/PD	-	-566.7	-	μA	V_{DD} = 5.5 V			
I_{SR11}	Source Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-372	-	μA	V_{DD} = 4.5 V, V_{IN} = 2.4 V			
I_{SR12}		-	-76.8	-	μA	V_{DD} = 2.7 V, V_{IN} = 2.2 V			
I_{SR13}		-	-37.3	-	μA	V_{DD} = 2.1 V, V_{IN} = 1.8 V			
I_{SR21}	Source Current PA/PB/PC/PD (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V			
I_{SR22}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V			
I_{SR23}		-	-2	-	mA	V_{DD} = 2.1 V, V_{IN} = 1.8 V			
I_{SK11}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V			
I_{SK12}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V			

I_{SK13}	and Push-pull Mode)	-	6	-	mA	V_{DD} = 2.1 V, V_{IN} = 0.4 V

Notes:

1. Only enable modules which support 32 kHz LIRC clock source
2. Only enable modules which support 10 kHz LIRC clock source

8.3 AC Electrical Characteristics

8.3.1 External Input Clock

Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

8.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.1	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	414	-	uA	12 MHz, V_{DD} = 5.5V
		-	407	-	uA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

8.3.3 External 32.768 kHz XTAL Oscillator (LXT)

SYM.	PARAMETER	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
f_{LXTAL}	Oscillator frequency		32.768		kHz	
T_{LXTAL}	Temperature	-40		105	°C	
I_{LXTAL}	Operating current		17		μA	VDD=2.1V

8.3.4 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	20 pF	20 pF
32.768 kHz	20 pF	20 pF

Figure 8.3-1 NDA102 Typical Crystal Application Circuit

8.3.5 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
		-2		2	%	T_A = -40℃~105℃ V_{DD}=2.1 V~ 5.5 V
I_{HRC}	Operating Current	-	1.1	-	mA	T_A = 25 ℃,V_{DD} = 5 V

8.3.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-50[1]	-	+50[1]	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃
I_{LRC}	Operating Current	-	0.3	0.5	μA	T_A = 25 ℃,V_{DD} = 5 V

Note: These parameters are characterized but not tested.

8.4 Analog Characteristics

8.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0~5.5 V
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency		12	16	MHz	V_{DD} = 3.0 ~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})			700	kSPS	V_{DD} = 3.0~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time		1000	1050	ns	V_{DD} = 3.0~5.5 V
V_{DD}	Supply Voltage	3.0	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	1.6	-	pF	-
R_{IN}	Input Load	-	2.5	-	kΩ	-

Note: ADC voltage reference is same with V_{DD}

8.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.1	-	5.5	V	-
V_{LDO}	Output Voltage		1.5		V	-
TA	Temperature	-40	25	105	℃	

Note: It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	2.1	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-

I_{LVR}	Quiescent Current			1	μA	T_A=25℃
V_{LVR}	Threshold Voltage	1.8	1.9	2.0	V	TA = -40℃ ~ +105℃

8.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	100	-	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Hysteresis	4.33	4.3	4.39	V	BOV_VL [2:0] = 3
		4.03	4.0	4.10	V	BOV_VL [2:0] = 2
		3.73	3.7	3.79	V	BOV_VL [2:0] = 7
		3.02	3.0	3.09	V	BOV_VL [2:0] = 1
		2.72	2.7	2.79	V	BOV_VL [2:0] = 6
		2.42	2.4	2.49	V	BOV_VL [2:0] = 0
		2.22	2.2	2.30	V	BOV_VL [2:0] = 5
		2.02	2.0	2.09	V	BOV_VL [2:0] = 4
V_{BOD}	Brown-out Detector		4.3		V	BOV_VL [2:0] = 3
			4.0		V	BOV_VL [2:0] = 2
			3.7		V	BOV_VL [2:0] = 7
			3.0		V	BOV_VL [2:0] = 1
			2.7		V	BOV_VL [2:0] = 6
			2.4		V	BOV_VL [2:0] = 0
			2.2		V	BOV_VL [2:0] = 5
			2.0		V	BOV_VL [2:0] = 4

8.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage		1.75		V	V_{DD} = 5.0 V
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset		TBD		mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset		TBD		V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset		TBD		ms	

8.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	46		μA	V_{DD}=3.3V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	225	-	ns	
V_{HYS}	Hysteresis	-	10	-	mV	ACMPPHYSEN = 01
V_{HYS}	Hysteresis	-	90	-	mV	ACMPPHYSEN = 10
T_{STB}	Stable time	-	1.06	-	μs	

Note: Guaranteed by design, not test in production.

8.4.7 PGA

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
	Operation voltage range	2.5	3.3	5.5	V	
	Operating Current			5	mA	V_{DD}=5V, T=125℃
	Operating Temperature	-40	25	125	℃	
	Input Offset with calibration Type corner, temp=25,VCM=AVDD/2			+2	mV	
	Input Offset Average Drift			1	uV/℃	
	Output Swing	0.1		V_{DD} - 0.1	V	
	PGA gain accuracy	-1		+1	%	
	Input Common Mode Range	0		V_{DD} - 1.5	V	
	DC Gain	50	80		dB	
	Unity Gain Frequency	7		8.2	MHz	V_{DD} = 5V
	Phase Margin	50°			°	
	PSRR+	49	90		dB	V_{DD} = 5V
	CMRR	69	90		dB	V_{DD} = 5V

	Slew Rate+		6.0	7.5	V/us	V_{DD}=5V, RLoad=1.3K, CLoad=100p
	Wake Up Time			20	us	

Note: Guaranteed by design, not test in production.

8.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	100,000	-	-	cycles[1]	
T_{RET}	Data Retention	20	-	-	year	T_A =125℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	-	7.5	us	
I_{DD1}	Read Current	-	3	4.5	mA	@33 MHz
I_{DD2}	Program Current	-	-	4	mA	
I_{DD3}	Erase Current	-	-	2	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
   Guaranteed by design, not test in production.

9 PACKAGE DIMENSIONS

9.1 28-Pin TSSOP (4.4x9.7x1.0 mm)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

10 REVISION HISTORY

Date	Revision	Description
2018.03.06	1.00	Preliminary version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.