3 Phase PMSM/BLDC Motor Controller with Gate Driver

General Description

RT7075 series are two–in-one IC which consists of 3 phase motor controller and gate driver required for PMSM/BLDC motor applications.

RT7075 series integrate ARM 32-bit Cortex-M0 core and peripheral circuits to perform FOC and Sensor-less motor control. Many system level peripheral functions, such as ADC, DAC, communication interface, SVPWM, watchdog timer, current sensing, over current protection and thermal shutdown are integrated in order to reduce component count, board space and system cost. Furthermore, RT7075 series drive external power N-Channel MOSFETs or IGBTs in a half-bridge configuration with an external bootstrap network up to 600V. A dead time control prevents shoot-through of the external power N-channel MOSFETs or IGBTs. The RT7075 series are available in a LQFP-48L 7x7 package.

Ordering Information

RT7075 □□□

- Package Type
  PL : LQFP-48L 7x7 (L-Type)
- Operating Temperature Range
  G : Green (Halogen Free and Pb Free)
- RT7075 Version (Refer to Version Table)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

RT7075 Version Table

Version	RT7075A	RT7075B	RT7075C
Sourcing Current	290mA	125mA	70mA

Features

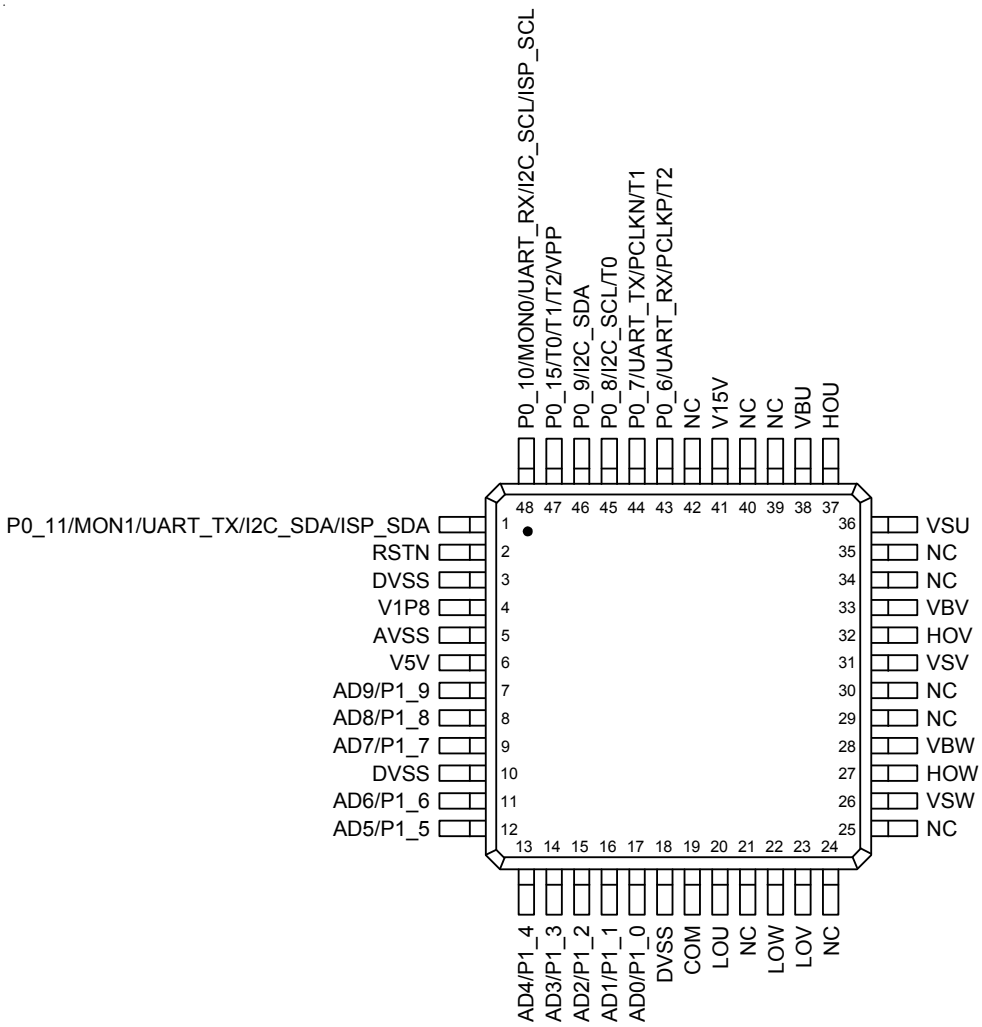
- **Integrated 3 Phase PMSM/BLDC Controller and Gate Driver**
- **Sensor-Less, Sine-Wave Field Oriented Control (FOC)**
- **Protections : Over Current , UVLO and Thermal Shutdown**
- **PMSM/BLDC Motor Controller :**
  - **ARM 32-bit Cortex-M0 CPU, Frequency up to 60MHz**
  - **Memories Size : 16KB MTP, Internal ROM with embedded motor control library and 4KB SRAM**
  - **Power Management : Normal Sleep and Deep Sleep**
  - **Programming Soft Start**
  - **Communication Interface : I^2C and UART**
  - **Programmable Clock for PFC control**
  - **10-Channel 10-bit ADC**
  - **1-Channel Current Type 6-bit DAC**
  - **1-Channel Voltage Type 8-bit DAC**
- **Gate Driver :**
  - **Floating Channel Designed for Bootstrap Operation up to 600V**
  - **Sourcing/Sinking Current :**
    RT7075A : 290mA/600mA
    RT7075B : 125mA/600mA
    RT7075C : 70mA/600mA
  - **Built in UVLO Functions for All Channels**
  - **Matched Propagation Delays for All Channels**
  - **V_{V15V} and $V_{VBU/V/W}$ Supply Range : 13V to 20V**
  - **Shoot Through Prevention**

Applications

- PMSM/BLDC motor
- Pedestal fan
- Ceiling fan
- Air conditioner indoor/outdoor fan
- Pump

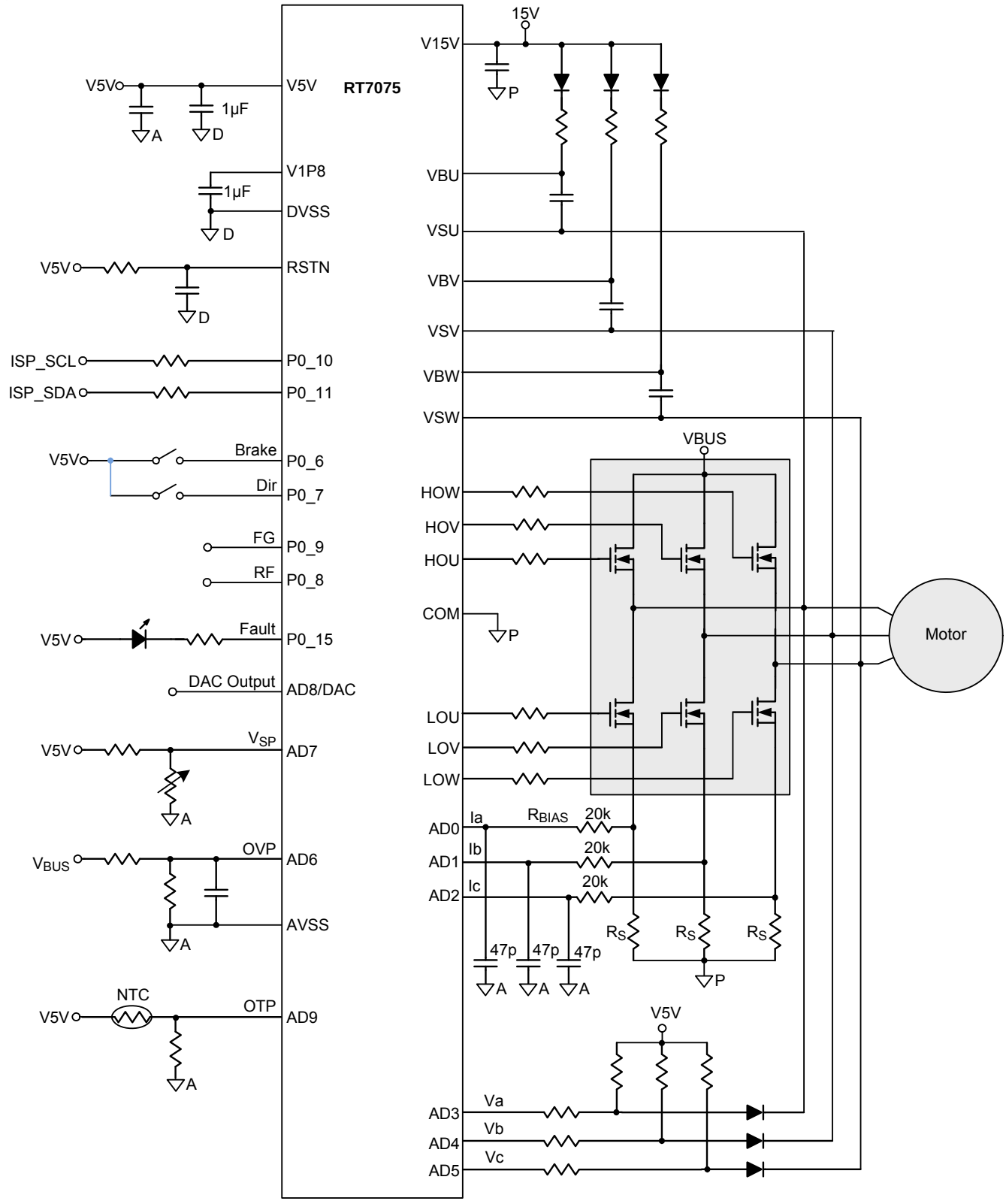
Pin Configurations

(TOP VIEW)



LQFP-48L 7x7

Typical Application Circuit



Functional Pin Description

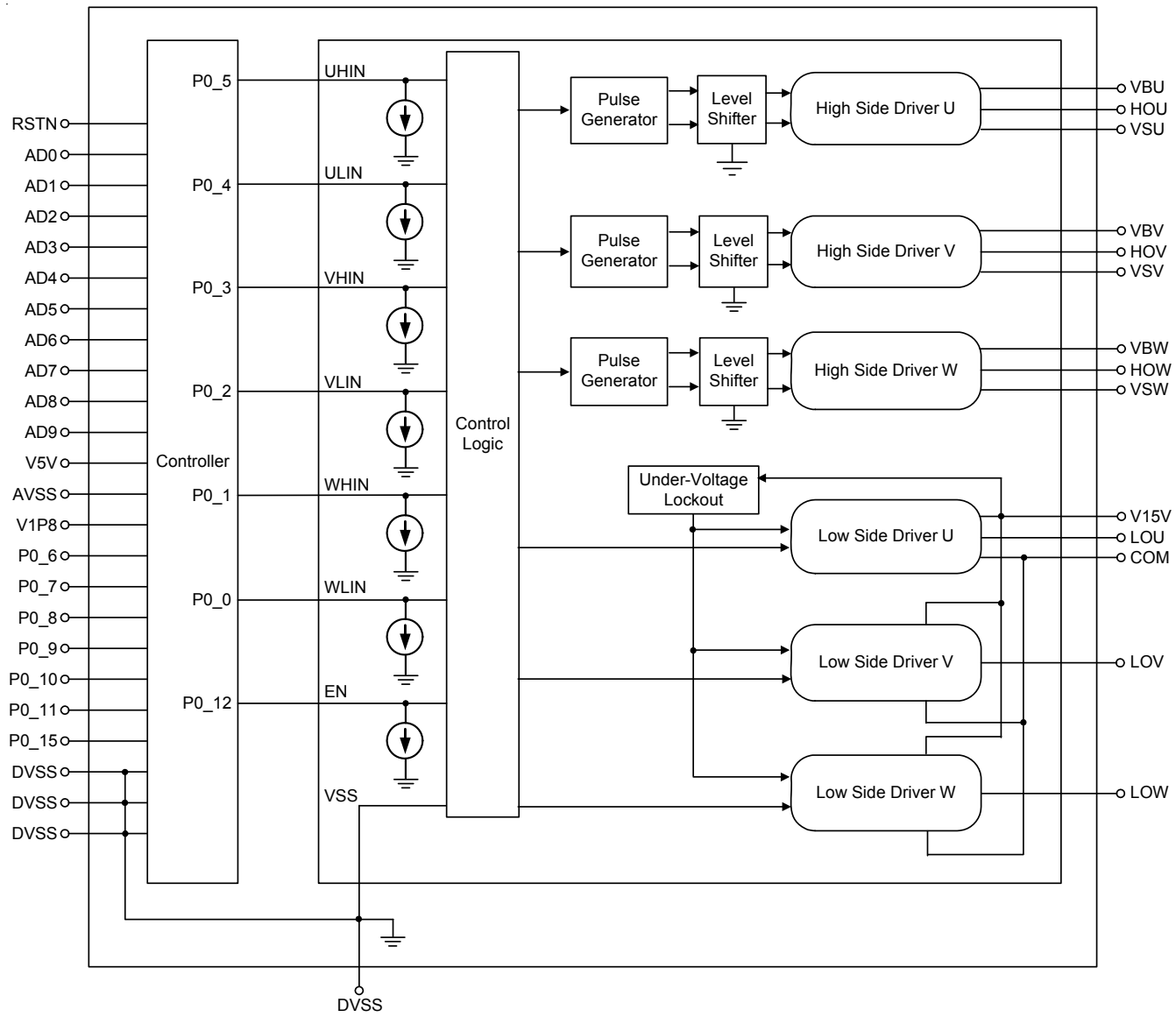
Pin No.	Pin Name	Type	Pin Function
1	P0_11	DIO	Pin 11 of GPIO Port 0.
	MON1	DO	Internal Digital Signal Monitoring Output Pin.
	UART_TX	DO	UART Transmitting Pin.
	I2C_SDA	DIO	I2C Data Pin.
	ISP_SDA	DIO	In System Programming Data Input Pin.
2	RSTN	DI	Pad Reset Pin.
3	DVSS	GND	Digital Ground.
4	V1P8	P	1.8V Power Pin.
5	AVSS	GND	Analog Ground.
6	V5V	P	5V Power Pin.
7	AD9	AIO	ADC Channel 9 Input Pin.
	AD9	AIO	Current Type DAC Input Pin. (Sink type)
	P1_9	DIO	Pin 9 of GPIO Port 1.
8	AD8	AIO	ADC Channel 8 Input Pin.
	AD8	AIO	Voltage Type DAC Output Pin.
	P1_8	DIO	Pin 8 of GPIO Port 1.
9	AD7	AIO	ADC Channel 7 Input Pin.
	P1_7	DIO	Pin 7 of GPIO Port 1.
10	DVSS	GND	Digital Ground.
11	AD6	AIO	ADC Channel 6 Input Pin.
	P1_6	DIO	Pin 6 of GPIO Port 1.
12	AD5	AIO	ADC Channel 5 Input Pin.
	P1_5	DIO	Pin 5 of GPIO Port 1.
13	AD4	AIO	ADC Channel 4 Input Pin.
	P1_4	DIO	Pin 4 of GPIO Port 1.
14	AD3	AIO	ADC Channel 3 Input Pin.
	P1_3	DIO	Pin 3 of GPIO Port 1.
15	AD2	AIO	ADC Channel 2 Input Pin.
	P1_2	DIO	Pin 2 of GPIO Port 1.
16	AD1	AIO	ADC Channel 1 Input Pin.
	P1_1	DIO	Pin 1 of GPIO Port 1.
17	AD0	AIO	ADC Channel 0 Input Pin.
	P1_0	DIO	Pin 0 of GPIO Port 1.
18	DVSS	GND	Digital Ground.
19	COM	PGND	Gate Driver Power Ground.

Pin No.	Pin Name	Type	Pin Function
20	LOU	HVO	Low-Side Gate Control Signal of Phase A.
21, 42	NC	--	No Internal Connection.
22	LOW	HVO	Low-Side Gate Control Signal of Phase C.
23	LOV	HVO	Low-Side Gate Control Signal of Phase B.
24, 25, 29, 30, 34, 35, 39, 40	NC	--	For H-V Rule.
26	VSW	HVI	High-Side Floating Supply Offset Voltage of Phase C.
27	HOW	HVO	High-Side Gate Control Signal of Phase C.
28	VBW	HVI	High-Side Floating Supply Voltage of Phase C.
31	VSV	HVI	High-Side Floating Supply Offset Voltage of Phase B.
32	HOV	HVO	High-Side Gate Control Signal of Phase B.
33	VBV	HVI	High-Side Floating Supply Voltage of Phase B.
36	VSU	HVI	High-Side Floating Supply Offset Voltage of Phase A.
37	HOU	HVO	High-Side Gate Control Signal of Phase A.
38	VBU	HVI	High-Side Floating Supply Voltage of Phase A.
41	V15V	P	15V Power Pin.
43	P0_6	DIO	Pin 6 of GPIO Port 0.
	UART_RX	DI	UART Receiving Pin.
	PCLKP	DO	Programmable Clock Positive Output Pin.
	T2	DI	T2 External Enable or external Clock Input Pin.
44	P0_7	DIO	Pin 7 of GPIO Port 0.
	UART_TX	DO	UART Transmitting Pin.
	PCLKN	DO	Programmable Clock Negative Output Pin.
	T1	DI	T1 External Enable or External Clock Input Pin.
45	P0_8	DIO	Pin 8 of GPIO Port 0.
	I2C_SCL	DIO	I2C Clock Pin.
	T0	DI	T0 External Enable or External Clock Input Pin.
46	P0_9	DIO	Pin 9 of GPIO Port 0.
	I2C_SDA	DIO	I2C Data Pin.
47	P0_15	DIO	Pin 15 of GPIO Port 0.
	T0	DI	T0 External Enable or External Clock Input Pin.
	T1	DI	T1 External Enable or External Clock Input Pin.
	T2	DI	T2 External Enable or External Clock Input Pin.
	VPP	P	8V Input Power for MTP Fast Programming.

Pin No.	Pin Name	Type	Pin Function
48	P0_10	DIO	Pin 10 of GPIO Port 0.
	MON0	DO	Internal Digital Signal Monitoring Output Pin.
	UART_RX	DI	UART Receiving Pin.
	I2C_SCL	DIO	I2C Clock Pin.
	ISP_SCL	DI	In System Programming Clock Input Pin.

IO Type Definition :
DIO : Digital input/output pin.
DI : Digital input pin.
DO : Digital output pin.
AIO : Analog input/output pin.
P : Power pin.
HVI : High voltage input pin.
HVO : High voltage output pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VV15V ---------- –0.3V to 25V
- Supply Input Voltage, VV5V ---------- –0.7V to 5.5V
- VSU/V/W to DVSS ---------- –0.3V to 625V
- VBU/V/W to VSU/V/W, VBU/V/W ---------- –0.3V to 25V
- HOU/V/W to VSU/V/W ---------- –0.3V to ($V_{VBU/V/W}$ + 0.3V)
- LOU/V/W to DVSS ---------- –0.3V to (V_{V15V} + 0.3V)
- Allowable VSU/V/W Voltage Slew Rate, dVSU/V/W /dt ---------- –50V/ns to 50V/ns
- Voltage of I/O Pin and RST Pin with Respect to GND, V_{VIH} ---------- –0.2V to V_{V5V} + 0.2V
- Analog Input Voltage, V_{AN} ---------- –0.2V to V_{V5V} + 0.2V
- Power Dissipation, P_D @ T_A = 25°C
  LQFP-48L 7x7 ---------- 1.49W
- Package Thermal Resistance (Note 2)
  LQFP-48L 7x7, θ_{JA} ---------- 67°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- V_{V15V} Supply Voltage, V_{V15V} ---------- 13V to 20V
- VBU/V/W to VSU/V/W, VBSx ---------- 13V to 20V
- VSU/V/W to DVSS ---------- 0 to 600V
- HOU/V/W to VSU/V/W ---------- 0 to VBSX
- LOU/V/W to DVSS ---------- 0 to V_{V15V}
- Supply Input Voltage, V_{V5V} ---------- 4.5V to 5.5V
- Supply Input Voltage, VPP ---------- 8V
- LDO capacitor on V1P8 ---------- 1µF
- Minimum time period of RSTN, T_{RSTN} ---------- 100µs
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{V15V} = $V_{VBU/V/W}$ = 15V, V_{V5V} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		--	50	--	MHz
Slow Clock for Sleep Mode	f_{LCLK}		--	80	--	kHz
Power Management Section						
Turn-On Voltage of V5V	V_{V_ON}		--	4.15	--	V
V_{5V} On-Off Hysteresis	V_{5_hys}	Turn-Off Voltage = V5V_ON - V5V_hys	--	0.3	--	V
LDO Output for Internal Operation Voltage	V_{1p8}	Full speed operation w/i external 20mA sink, CV1p8 > 1μF	--	1.8	--	V
1.8V Under Voltage to Reset MCU	V_{1p8_UV}		--	1.3	--	V
De-Bounce Time of 1.8V Under Voltage to Reset MCU	t_{1p8_UV}		--	50	--	μs
V_{5V} Current at Operation Mode	I_{5V_OPER}	20kHz PWM output, room temp, 25°C	--	15	--	mA
V_{5V} Current at Normal Sleep Mode	I_{5V_NSLP}	Room temp, 25°C	--	10	--	mA
V_{5V} Current at Deep Sleep Mode	I_{5V_DSLP}	Room temp, 25°C	--	320	--	μA
ADC Section (0~4V, 10-bit, single end mode, gain = 1)						
Minimum Conversion Voltage	V_{I_MIN}	Code 000h	--	0	--	V
Maximum Conversion Voltage	V_{I_MAX}	Code 3FFh	--	4	--	V
OCDAC Section (0V-4V, 8-Bit for short current and OC protect)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	4	--	V
DAC Offset	Voffset		--	0	--	mV
VDAC Section (0V-3V, 8-bit for other protect, output, and debug)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	3	--	V
DAC Offset	Voffset		--	0	--	mV
Output Resistance of DAC	Ro		--	1k	--	Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IDAC Section (0-100μA, 6-Bit for current sink)						
IDAC Output Bias Voltage Range	Vibias		0.2	--	5	V
Minimum Sink Current	I_{O_MIN}	Code 00h, Vibias = 2.5V	0	0	0.1	μA
Maximum Sink Current	I_{O_MAX}	Code FFh, Vibias = 2.5V	--	126	--	μA
Average Current Step	I_{LSB}	Test : (Ii_min-Ii_max)/(256-1)	--	2	--	μA
DAC Offset	Ioffset		--	0	--	μA
Current Limit Comparator Section (Short and OC)						
Comparator Offset	Voffset		−10	0	10	mV
Input Voltage Range of Comparator	Vin		1	--	4	V
General Purposed Comparator						
Comparator Offset	Voffset		−5	0	5	mV
Input Voltage Range of Comparator	Vin		0	--	3	V
IO of P0_6~P0_7 Section						
Positive Going Threshold Voltage	V_{IH}		--	3	--	V
Negative Going Threshold Voltage	V_{IL}		--	2	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.9	--	V
Pull-Down Resistor	R_{DOWN}		--	40	--	kΩ
High Level Output Current	I_{OH}	@ 0.8xV5V	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2xV5V	--	40	--	mA
IO of P0_8~P0_11 section						
Input High Voltage	V_{IH}		--	3	--	V
Input Low Voltage	V_{IL}		--	2	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	0.9	--	V
Pull-Up Resistor	R_{UP}		--	70	--	kΩ
High Level Output Current	I_{OH}	@ 0.8xV5V	--	8	--	mA
Low Level Output Current	I_{OL}	@ 0.2xV5V	--	20	--	mA
IO of AD0~AD9 section						
Positive Going Threshold Voltage	V_{IH}		--	2	--	V
Negative Going Threshold Voltage	V_{IL}		--	1	--	V
Hysteresis (V_{IH} – V_{IL})	V_H		--	1	--	V
Current Source for External Bias	I_{BIAS}		--	100	--	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
I²C Interface Section							
I²C Clock Cycle Time	t_{SCL}			t_{SYS} x 80	--	--	ns
I²C Start Bit Setup Time	t_{START}			--	t_{SCL} / 2	--	ns
I²C Stop Bit Setup Time	t_{STOP}			--	t_{SCL} / 2	--	ns
I²C Data Setup Time	t_{SETUP}			--	t_{SYS}	--	ns
I²C Data Hold Time	t_{HOLD}			--	t_{SYS}	--	ns
Low Side Power Supply Section							
V15V Under-Voltage Lockout Threshold (On)	V_{THON_V15V}			9	10.5	12	V
V15V Under-Voltage Lockout Threshold (Off)	V_{THOFF_V15V}			8	9.5	11	V
V15V Under-Voltage Lockout Hysteresis	V_{HYS_V15V}			--	1	--	V
V15V Quiescent Current	I_{Q_V15V}	Gate driver output low.		--	1000	--	μA
V15V Operating Current	I_{P_V15V}	f_{XLIN} = 20kHz, HOU/V/W & LOU/V/W = Open		--	1000	--	μA
Bootstrapped Power Supply Section							
VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (On)	V_{THON_VBSX}			9	10.5	12	V
VBU/V/W-VSU/V/W Under-Voltage Lockout Threshold (Off)	V_{THOFF_VBSX}			8	9.5	11	V
VBU/V/W-to-VSU/V/W Quiescent Current for Each Channel	I_{Q_VBSX}	Gate driver output low.		--	100	200	μA
VBU/V/W-VSU/V/W Under-Voltage Lockout Hysteresis	V_{HYS_VBSX}			--	1	--	V
VSU/V/W Leakage Current	I_{VSX}	$V_{BU/V/W}$ = $V_{SU/V/W}$ = 600V		--	--	50	μA
VBU/V/W-to-VSU/V/W Operating Current	I_{OP_VBSX}	f_{XHIN} = 20kHz, HOX, LOX = Open		--	--	600	μA
Gate Driver Output Section (HOU/V/W, LOU/V/W)							
High Side / Low Side Output Voltage	VOH	I_O = 0mA, $V_{VBU/V/W}$ - $V_{HOU/V/W}$, V15V - $V_{LOU/V/W}$		--	50	200	mV
	VOL	IO = 0mA, $V_{HOU/V/W}$-$V_{VSU/V/W}$, $V_{LOU/V/W}$-V_{COM}		--	20	100	mV
HOU/V/W and LOU/V/W Sourcing Current	IO+	Gate driver output high, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 0V, PW < 10μs	RT7075A	--	290	--	mA
			RT7075B	--	125	--	
			RT7075C	--	70	--	
HOU/V/W and LOU/V/W Sinking Current	IO-	Gate driver output low, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = V_{V15V}, PW < 10μs		--	600	--	mA

Dynamic Electrical Characteristics

(V_{V15V} = $V_{VBU/V/W}$ = 15V, V_{V5V} = 5V, $V_{VSU/V/W}$ = GND, C_L = 1000pF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Gate Driver Output Turn-On Rising Time	t_r	RT7075A	--	70	--	ns
		RT7075B	--	300	--	
		RT7075C	--	550	--	
Gate Driver Output Turn-Off Falling Time	t_f		--	35	--	ns
Gate Driver Output Dead Time	DT		--	500	--	ns

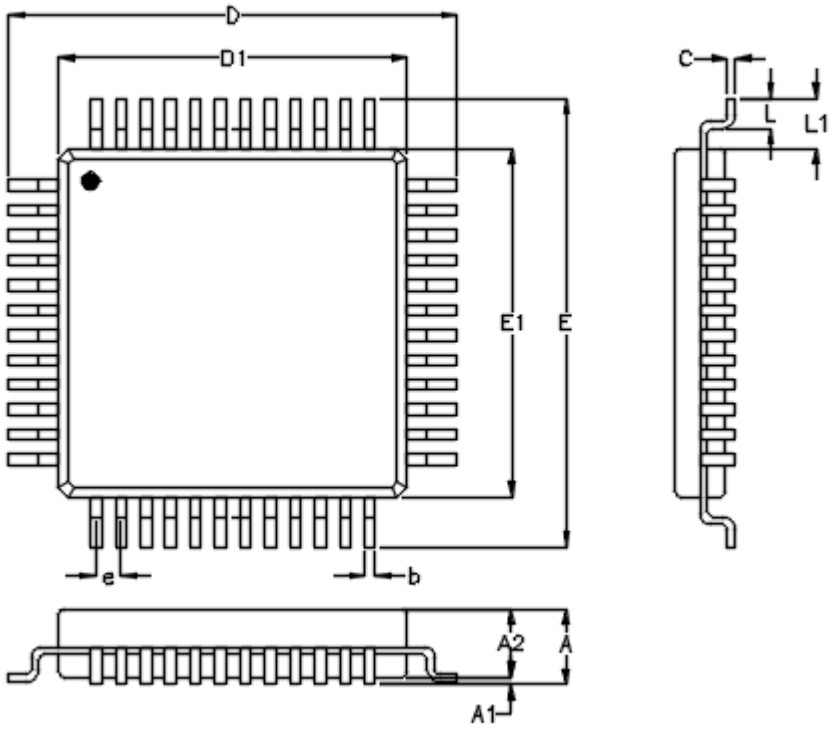
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.170	0.270	0.007	0.011
C	0.090	0.200	0.004	0.008
D	8.800	9.200	0.346	0.362
E	8.800	9.200	0.346	0.362
D1	6.900	7.100	0.272	0.280
E1	6.900	7.100	0.272	0.280
e	0.500		0.020	
L	0.450	0.750	0.018	0.030
L1	0.800	1.200	0.031	0.047

L-Type 48-Lead QFP 7x7 Plastic Package

Datasheet Revision History

Version	Date	Item	Description
P00	2015/6/2		First Edition
P01	2015/6/18	Features Pin Configurations Typical Application Circuit Functional Pin Description Recommended Operating Conditions Electrical Characteristics	Modify
P02	2015/9/3	General Description Features Ordering Information Absolute Maximum Ratings Version Table (Add) Electrical Characteristics	Modify

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