AN2388

Peak Current Controlled ZVS Full-Bridge Converter with Digital Slope Compensation

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ABSTRACT

This application note features a detailed discussion on plant modeling, control system design and firmware implementation of a 750W Peak Current Controlled Zero-Voltage Switching Full-Bridge (ZVS FB) Converter reference design with digital slope compensation. This ZVS FB Converter is designed to step down an input DC voltage of 400V to an output DC voltage of 12V. A unique feature of the reference design is the implementation of peak current control, using a fully software-based slope compensation algorithm, which eliminates the use of external analog components for slope compensation. This algorithm is topology independent and is easily implemented in Digital Signal Controllers (DSCs) with minimal latency, which is essential for achieving a near analog response.

INTRODUCTION

There is a growing need for higher efficiency, reliability and power density across the power electronics industry. These needs have driven the rapid growth of digital power solutions, especially in telecom and server power areas. The advantages and challenges of digitally controlled power supplies have been a topic of discussion and debate for several years. Integration of advanced peripherals for power supply control in microcontrollers, coupled with advanced high-speed devices in the power semiconductor industry, have led to an increased market penetration of digital power in the industry. Control techniques that were earlier the forte of analog solutions are now more feasible in the digital space. In this context, this reference design features the implementation of peak current control in a ZVS Full-Bridge topology (a high-level representation is shown in Figure 1), using a fully digital slope compensation technique with minimum software overhead.

In this application note, the proposed algorithm is a patented proprietary of Microchip Technology Inc., which offers minimum software latency in its computation of the slope compensated peak current reference on a cycle-by-cycle basis.

The ZVS FB Converter is one of the most commonly used topologies in server and telecom power supplies, battery chargers and renewable applications, mainly due to its high-efficiency operation and ease of control. In this topology, both Average Current mode control and Voltage mode control implementations typically require a capacitor in series with the transformer to prevent flux walking. The peak current control implementation eliminates the need for the series capacitor by virtue of dynamic flux balancing. In peak current control, however, to overcome the well-known subharmonic oscillations for duty cycles larger than 50%, a slope compensation ramp is either added to the inductor current or subtracted from the peak current reference generated by the voltage loop compensator. Peak current control is typically an analog technique, implemented using linear amplifiers, transistors, RC networks and analog comparators (Figure 2), or by using dedicated Application-Specific Integrated Circuits (ASICs).

Peak current control can also be accomplished digitally in three ways. The first method is popularly called predictive peak current control. In this technique, a leading-edge modulation of the PWM is used and the duty cycle is computed at the beginning of every cycle. This technique eliminates the need for slope compensation and an analog comparator. Here, the effective duty cycle is calculated based on the inductance, sensed input and output voltages, and the switching period. The disadvantage of this method is the dependence on the inductance value, which is susceptible to variation.

The second method is essentially a hybrid technique, involving a digital compensator, analog slope compensation (external), and an analog comparator (internal to the microcontroller).

The hybrid technique consists of removing the analog compensator in Figure 2 and replacing it with a digital compensator. The output of the compensator feeds a “digital peak current reference” to the Digital-to-Analog Converter (DAC) of a built-in high-speed analog comparator, as shown in Figure 3. The (internal) analog comparator then compares the DAC output to the slope compensated inductor current waveform and provides the truncation signal to the PWM module. The inductor/switch current waveform is added to a slope compensation ramp using an external analog circuitry. In addition to requiring additional components, the analog slope compensation could be suboptimal for a wide input voltage range.

The third method which is used in this reference design is a fully digital implementation, requiring no external components for implementing peak current control (a high-level representation is shown in Figure 3). The digital compensator, slope compensation and analog comparator are internal to the microcontroller. Here, the slope compensation is accomplished by an algorithm implemented in firmware.

This algorithm takes the input voltage, output voltage, inductor current and the digital peak current reference (from the digital compensator), and produces a slope compensated peak current reference, as shown in Figure 3.

The slope compensated peak current reference is then fed to the DAC of the internal high-speed comparator (inverting input). The inductor current feedback is fed directly to the non-inverting input of the comparator. The advantages of this method are better reliability due to reduced components and the ability to implement adaptive algorithms for better dynamic response. A detailed discussion on the implementation of the fully digital peak current control is provided in the following sections.

FIGURE 1: ZVS FULL-BRIDGE CONVERTER

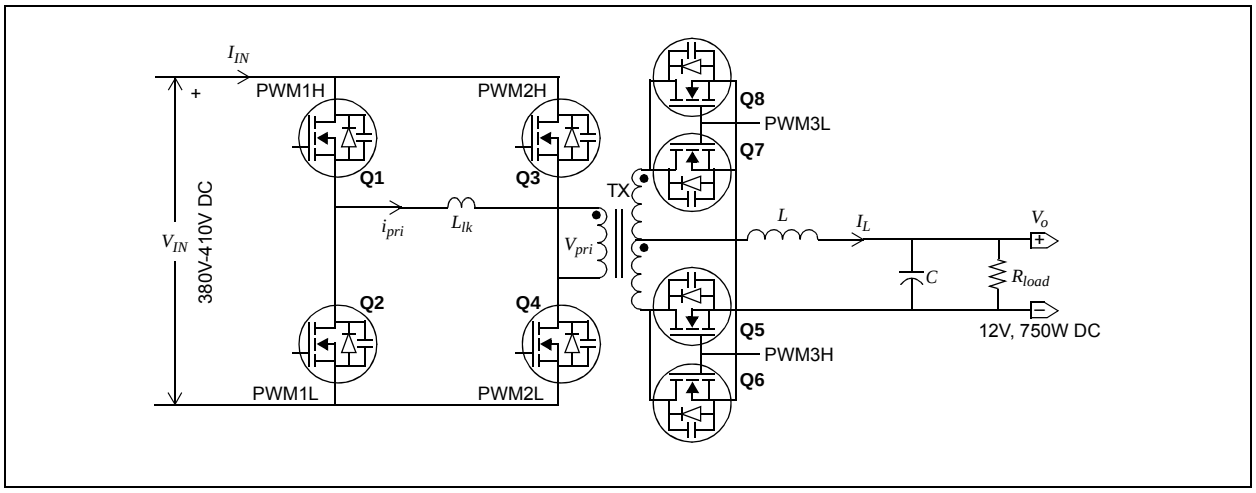


FIGURE 2: PEAK CURRENT CONTROL – ANALOG

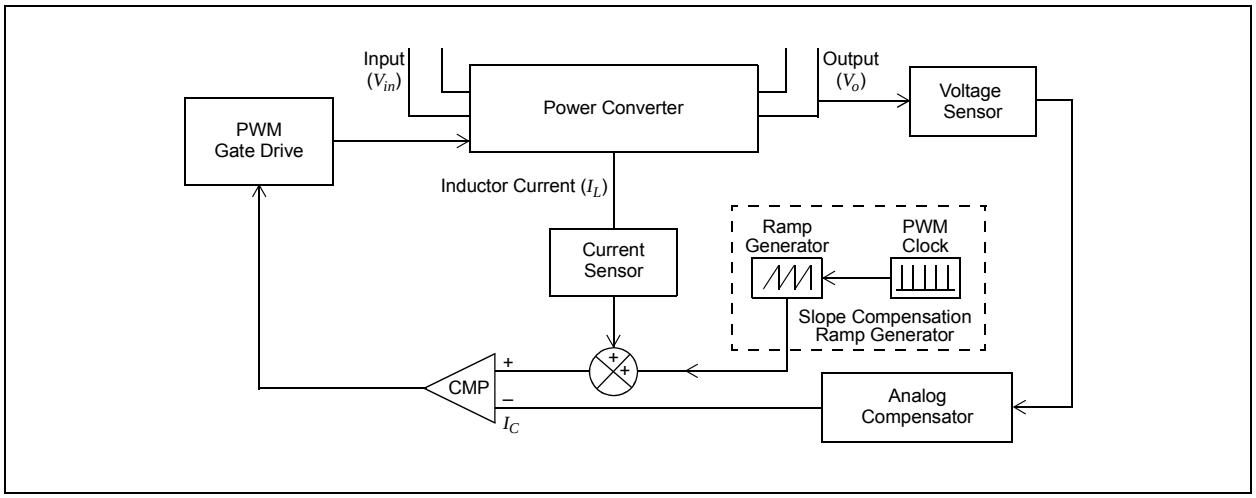
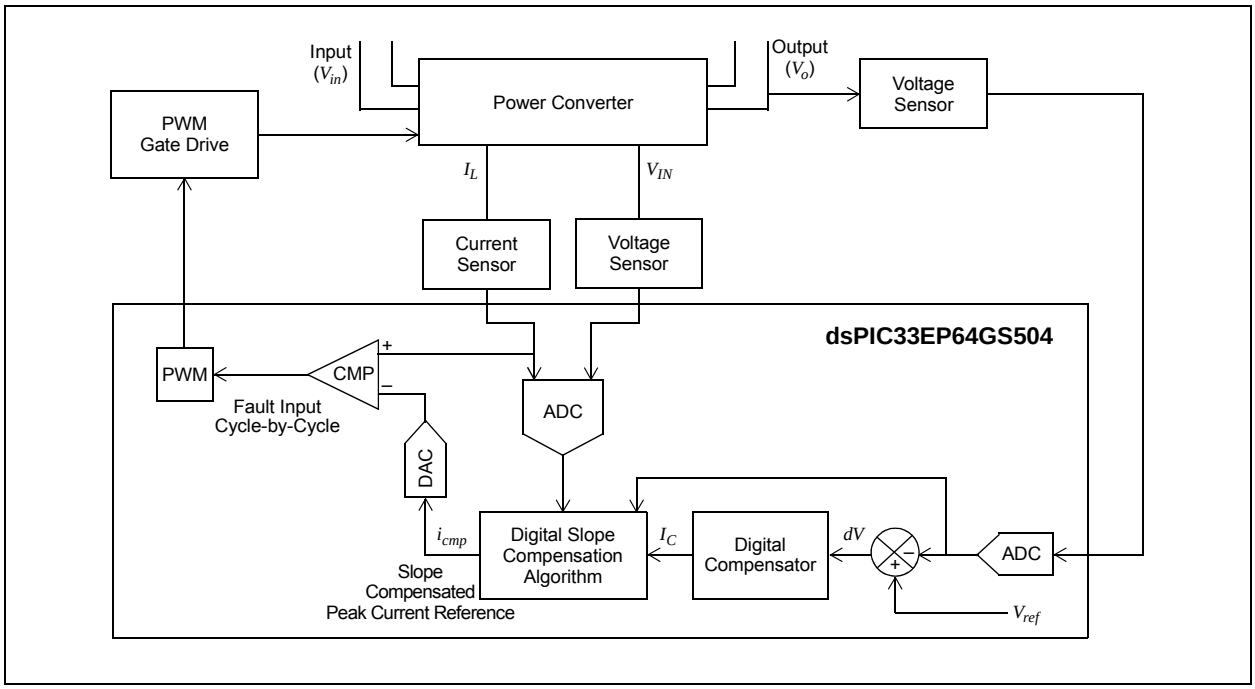


FIGURE 3: PEAK CURRENT CONTROL – DIGITAL



HARDWARE OVERVIEW

This section provides:

- A brief description of the topology and specifications
- A detailed discussion on the switching scheme
- A detailed description on the high-level control scheme and feedback networks

The ZVS FB Converter, shown in Figure 1, has a transformer with a center tapped secondary configuration with full wave synchronous rectification. Each leg of the full-bridge (Q1-Q2 and Q3-Q4) on the primary side of the transformer is driven by one PWM pair. In Figure 1, L_{lk} represents the summation of the transformer leakage inductance and the external inductance required for achieving the resonant transition of the leakage energy. The leakage energy depletes the charge in C_{oss} capacitance of each of the MOSFETs before turning them on (ZVS switching). On the secondary side, two MOSFETs are paralleled in each leg of the synchronous rectifiers (Q5-Q6 and Q7-Q8) and are driven by one PWM pair. This parallel configuration enables high-efficiency operation during high loads. L and C constitute the output filter stage, and the load is represented by R_{load}.

In a typical server/telecom application, the input to the ZVS FB Converter is provided by a front-end Power Factor Correction (PFC) Converter. The PFC stage typically takes the universal input voltage (90V-264V, 47 Hz-63 Hz AC) and provides a nominal output voltage of 400V. For this reference design, an input voltage range of 380V to 410V is considered. The specifications of the 750W ZVS FB Converter and a few key component values are shown in Table 1.

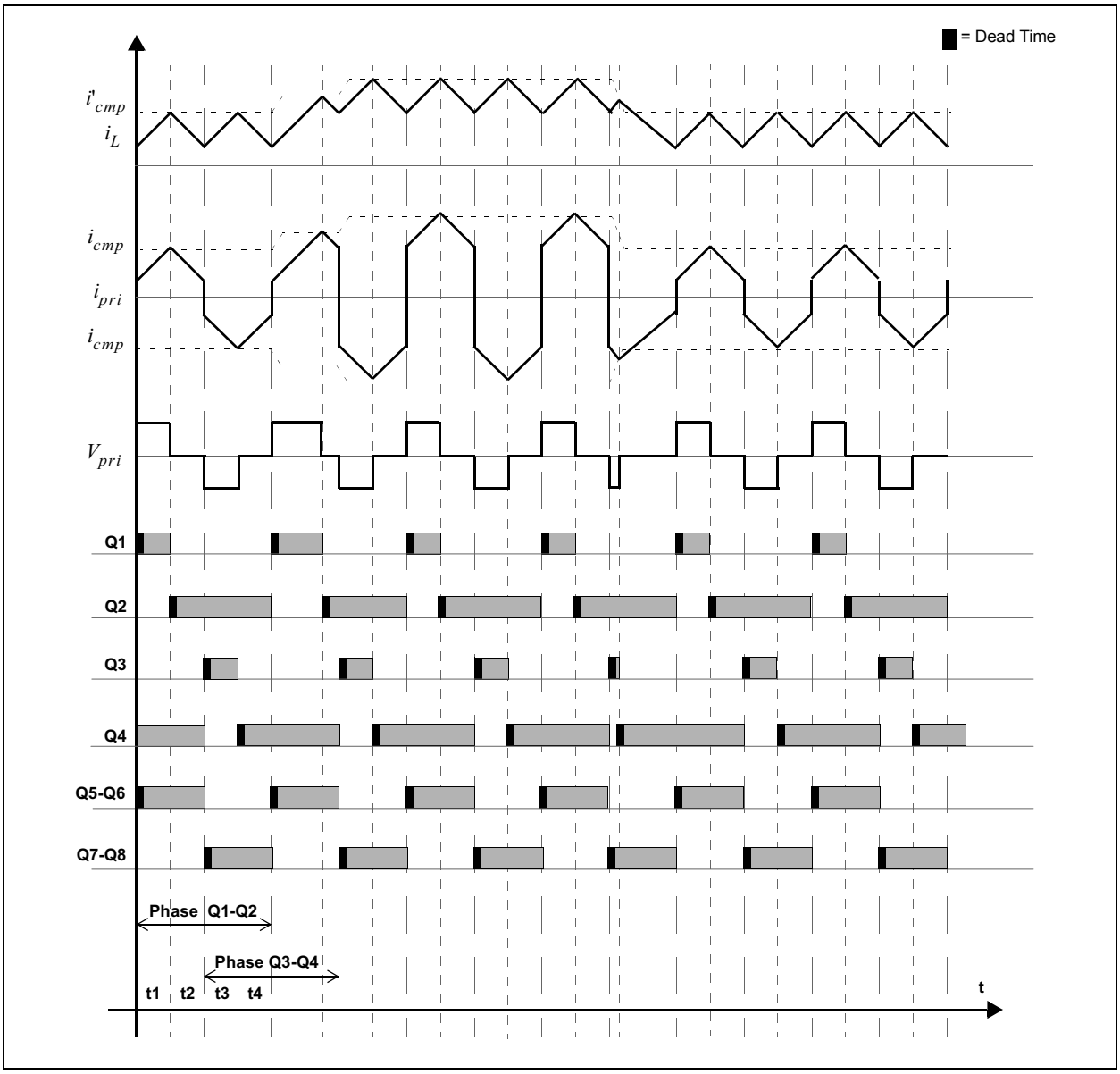
TABLE 1: CONVERTER SPECIFICATIONS AND KEY COMPONENT VALUES

Topology	ZVS Full-Bridge with Center Tapped Secondary and Synchronous Full Wave Rectification
Input Voltage	380V-410V DC
Output Voltage	12V, ±1%
Output Power	750W (62.5A @ 12V DC)
Control Method	Peak Current-Mode Control (PCMC) with Digital Slope Compensation
Transformer Turns	25:1:1
Filter Inductor (L)	2.78 µH
Output Filter Capacitor (C)	7.5 mF
Resonant Inductor (L_{lk})	38 µH
Peak Efficiency	96%
Form Factor	All Components Designed to Fit in 1U Form Factor (41 mm height)
Other Features	• Galvanic Isolation • Support for I^2C Communication • UART Communication with Front-End PFC

Switching Scheme

Figure 4 shows the switching waveforms of the ZVS FB Converter used in this reference design. Here, i_{cmp} is the peak current reference input to the comparator, i'_{cmp} is the peak current input referred to as the secondary side and I_L is the inductor current. The switching waveform for each of the MOSFETs, shown in Figure 1, is depicted in Figure 4.

FIGURE 4: SWITCHING WAVEFORMS OF ZVS FB CONVERTER



As shown in Figure 4, the leg comprising the Q1-Q2 MOSFETs is driven by a pair of PWMs (PWM1H and PWM1L, respectively) in Complementary mode. The leg comprising the Q3-Q4 MOSFETs is driven by a pair of PWMs (PWM2H and PWM2L, respectively) in Complementary mode. The MOSFETs Q1-Q2 are phase-shifted with respect to Q3-Q4 by 180°, as shown in Figure 4. This phase shift between the two legs of the full-bridge is kept fixed, unlike the traditional PSFB implementation, where the phase shift dynamically varies in closed-loop control. The portions of the PWM waveforms shown in black in Figure 4 indicate the resonant interval (dead time) between the complementary PWMs. The PWM Generator driving the synchronous secondary rectifiers (Q5-Q6 and Q7-Q8) is configured in Independent Time-Based mode. In Independent Time-Based mode, the phase and duty cycle of each PWM in a pair can be independently configured. In this case, PWM3L is configured to obtain a phase difference of 180° with respect to PWM3H. PWM3H drives Q5-Q6 and PWM3L drives Q7-Q8. The MOSFETs Q5-Q6 conduct during the first half of the PWM cycle. The MOSFETs Q6-Q7 conduct during the second half cycle of the PWM cycle. As shown in Figure 4, within one PWM cycle of the primary switches, there are two cycles of the inductor current (I_L). The intervals, t1, t2, t3 and t4, constitute one PWM cycle.

A brief description of the different intervals within a PWM cycle is provided in the following sections (where the terms, 'MOSFET' and 'switch', are interchangeably used).

POSITIVE CYCLE POWER DELIVERY INTERVAL (t1)

At the beginning of the PWM cycle, Q1 and Q4 diagonal switches conduct, resulting in a positive current in the transformer (i_{pri}). The interval begins with the ZVS turn-on of the switch, Q1. The inductor current starts increasing, and when it reaches the set peak current reference (i'_{cmp}), Q1 switch is turned off and the complementary Q2 switch turns on after a short resonant interval (dead time). During this resonant interval, the energy stored in the resonant inductor, L_{lk}, causes discharging of C_{oss} of the Q2 MOSFET and charging of C_{oss} of the Q1 MOSFET. The dead time is chosen, such that when the C_{oss} of Q2 is completely discharged, Q2 is turned on with ZVS. The Q4 MOSFET continues to remain on until the end of the Q3-Q4 phase, which also marks the end of the half-cycle of the PWM period.

During the interval, t1, on the secondary side, the current flows from the transformer terminals to the output filter and loads through the Q5-Q6 MOSFETs, which are turned on. The Q5-Q6 pair remains turned on during the complete positive current cycle (t1 and t2).

POSITIVE CYCLE FREEWHEELING INTERVAL (t2)

This interval begins with the ZVS turn-on of the Q2 switch and Q2 remains on until the end of the Q1-Q2 phase shown in Figure 4. The transformer current (i_{pri}) continues to freewheel in a positive direction. The transformer primary voltage is essentially zero during t2. On the secondary side, the inductor current (I_L) has a negative slope and freewheels through the inductor, Q5-Q6 and the transformer winding. At the end of the t2 interval, Q4 switch turns off as the period of the Q3-Q4 complementary pair reaches its end (since this pair is phase-shifted with respect to Q1-Q2 by 180°, as shown in Figure 4). The complementary Q3 switch turns on after a short resonant interval, during which, the energy stored in L_{lk} discharges C_{oss} of Q3 and charges C_{oss} of Q4. This results in the ZVS turn-on of Q3 at the beginning of the t3 interval.

At the end of the t2 interval, the Q5-Q6 pair turns off, and after a short dead time, the Q7-Q8 switches are turned on. During this dead time, the inductor current flows through the body diodes of both Q5-Q6 and Q7-Q8 until the Q7-Q8 pair is turned on.

NEGATIVE CYCLE POWER DELIVERY INTERVAL (t3)

This interval begins with ZVS turn-on of Q3 and turn-on of Q7-Q8 on the secondary rectifier. It should be noted that the Q2 switch is already switched on in the t2 interval. The transformer current (i_{pri}) increases in the negative direction, resulting in a negative power delivery cycle. The inductor current on the secondary side starts increasing (as shown in Figure 4). Once the current reaches the set peak current value (i_{cmp}), the Q3 MOSFET is turned off. After the resonant interval has elapsed, the complementary Q4 switch turns on. During the resonant interval, the leakage energy of L_{lk} charges C_{oss} of Q3 to rail voltage, while simultaneously discharging C_{oss} of Q4. Once the voltage across the drain to the source of the Q4 MOSFET reaches close to 0V, it is ready to be turned on, marking the beginning of the t4 interval. The Q7-Q8 switches remain on throughout the transformer negative current cycle (t3-t4).

NEGATIVE CYCLE FREEWHEELING INTERVAL (t4)

This interval begins with the ZVS turn-on of the Q4 switch and Q4 remains on until the end of the Q3-Q4 phase (shown in Figure 4). The transformer current (i_{pri}) continues to freewheel in a negative direction, circulating between Q2 and Q4. The transformer primary voltage is essentially zero during t4. On the secondary side, the inductor current (I_L) has a negative slope and freewheels through the inductor, Q7-Q8 and the transformer winding. At the end of t4, the Q2 switch turns off as the period of the Q1-Q2 complementary pair comes to an end (as shown in Figure 4). The complementary Q1 switch turns on after a short resonant interval, during which, the energy stored in L_{lk} discharges C_{oss} of Q1 and charges C_{oss} of Q2. This results in a ZVS turn-on of Q1 at the beginning of the next positive power delivery interval (t1). At the end of t4, the Q7-Q8 switches also turn off, and after a short dead time, the Q5-Q6 switches are turned on. During this dead time, the inductor current flows through the body diodes of both the Q7-Q8 and Q5-Q6 pairs until the Q5-Q6 pair is turned on, marking the beginning of the next positive power delivery cycle.

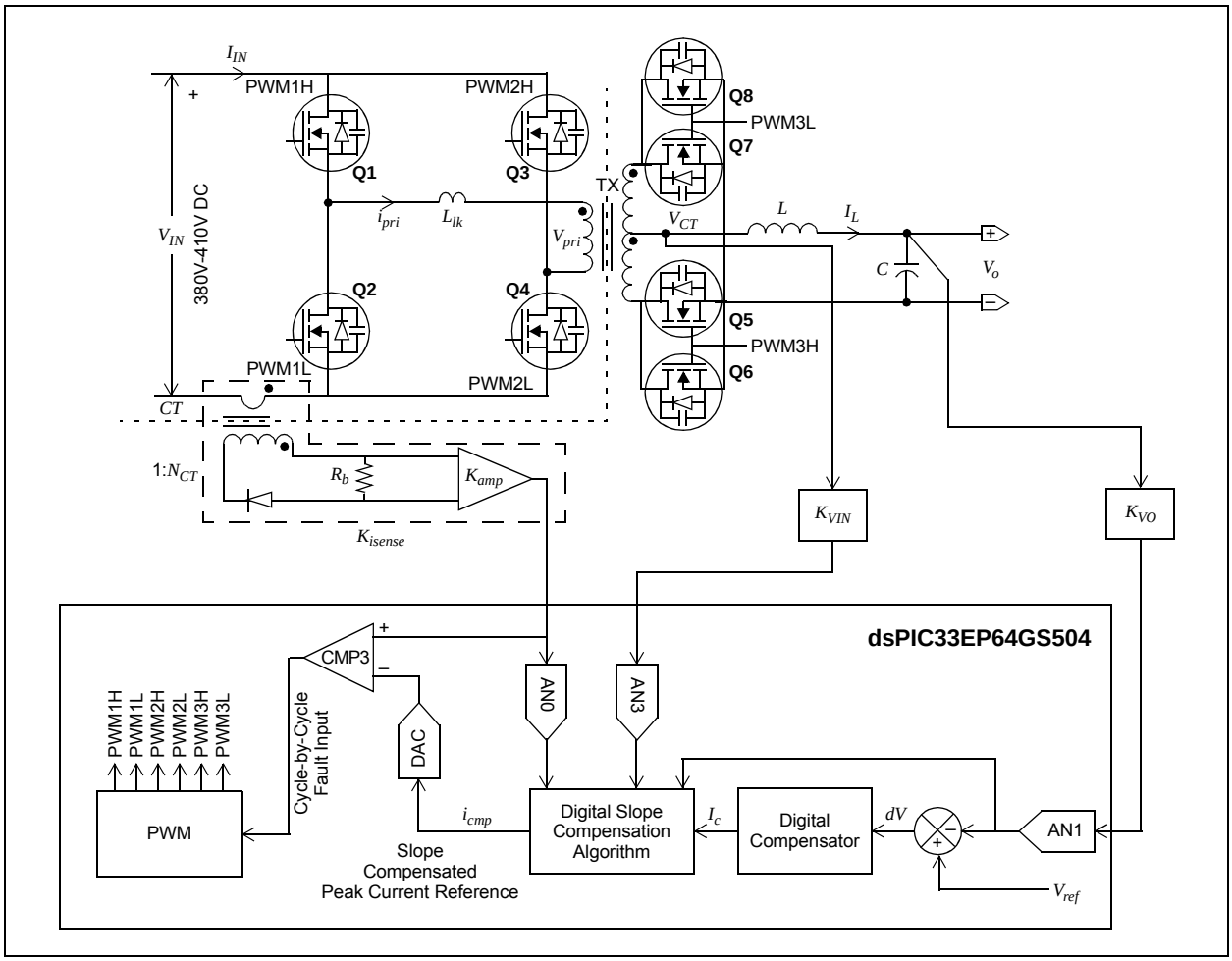
Digital Control of ZVS FB Converter with Digital Slope Compensation

A high-level control block diagram with the dsPIC® DSC is shown in Figure 5. Three key feedback signals are required for closed-loop control of the ZVS FB Converter with digital slope compensation. They are:

- Output Voltage (V_o)
- Inductor Current (I_L)
- Input Voltage (V_{in})

The output voltage is sensed by a resistor divider network (of gain, K_{VO}) and is fed to the dedicated ADC Core 1 channel, AN1. The digitized output voltage is then subtracted from a digital reference voltage, V_{ref}, and the error, dV, is fed to the digital voltage loop compensator. The output of the digital compensator is the uncompensated peak current reference, I_c.

FIGURE 5: ZVS FULL-BRIDGE CONVERTER WITH DIGITAL SLOPE COMPENSATION



Feedback of the reflected inductor current (i_{IN}) on the converter input terminals is sensed by a Current Transformer (CT), the output of which is amplified and fed to the dedicated ADC Core 0 channel, AN0. The total gain of the current sense network is K_{isense}, as shown in Figure 5. The AN0 channel is triggered to sample the reflected inductor current at the beginning of every half PWM cycle (valley current). A feedback of the reflected input voltage (on the transformer secondary, as shown in Figure 5) is sensed by a resistor divider network (of gain, K_{VIN}) and fed to the dedicated ADC Core 3 channel, AN3. The input voltage is reflected across the center tap of the secondary winding only during the power delivery intervals, t1 and t3 (Figure 4). Hence, the trigger for sampling the reflected input voltage sensed at AN3 has to be set to occur within t1 or t3. The digital peak current reference, input voltage feedback, output voltage feedback and the sensed valley current are processed by a digital slope compensation algorithm, which is executed at the beginning of every half-cycle of the full-bridge drive. The output of the digital slope compensation algorithm is the slope compensated peak current reference, i_{cmp}. The slope compensated peak current reference is scaled and fed to the 12-bit DAC. The DAC output is the input to the inverting terminal of the internal high-speed analog comparator. The non-inverting terminal of the analog comparator is fed with sensed (reflected) inductor current, which is the output of the current sense network. When the sensed inductor current reaches the programmed i_{cmp} value, the analog comparator output goes high. The output of the analog comparator is configured as a cycle-by-cycle Fault source for the high-speed PWM module, which turns off PWM1H or PWM2H, as shown in Figure 4.

As mentioned earlier, three key feedback signals are required for implementation of peak current control with digital slope compensation and are discussed in the following sections.

INDUCTOR CURRENT

For peak current control, it is essential to have an accurate feedback of the inductor current. A switching frequency of FSW on the full-bridge MOSFETs results in an inductor current frequency of 2 FSW. Typically, for an accurate replication of the inductor current, the sensor bandwidth must be at least 15-20 times the inductor current frequency. Thus, for an FSW of 75 kHz, the bandwidth of the current sense circuitry must be ~2 MHz for a desired replication of the current. Although it is possible to measure the inductor current directly by either using a shunt or a Hall effect sensor, there are disadvantages in both approaches. In the shunt measurement approach, expensive circuitry with large Common-mode voltages and high bandwidth are required to process the voltage across the shunt before feeding to the ADC pin. Also, the shunt is typically placed in the series path of the inductor current, resulting in I^2R loss, and therefore, is an inefficient solution. The disadvantage of a Hall effect sensor is the high cost of high bandwidth sensors; hence, this solution is not considered.

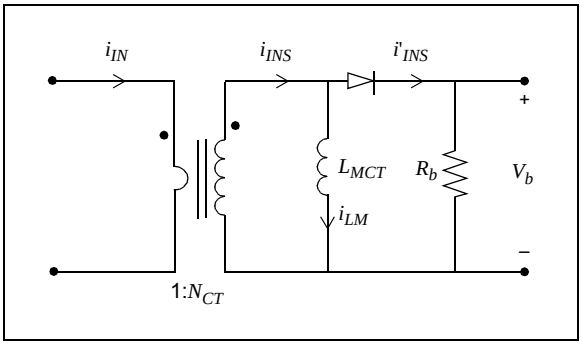
The disadvantages of shunt and Hall effect measurements are addressed by a Current Transformer (CT), which is both a low-cost and high bandwidth solution. The inductor current is essentially a DC current and cannot be directly measured using a CT. However, a feedback of the reflected inductor current can be obtained by placing a CT (of N_{CT} turns) in the path of the input current, I_{IN}, as shown in Figure 5. In this design, the CT terminals are connected to a burden resistor (R_b), followed by a low-pass filter and a high bandwidth amplifier. The inductor current is reflected to the primary side only during the power delivery intervals (t1 and t3 in Figure 4). The time intervals available for reset of the Current Transformer core are the freewheeling intervals (t2 and t4) at every half PWM cycle (or each inductor current cycle).

A reflection of the current flowing through the primary terminals of the CT, in the form of voltage across R_b, is most accurate when it is kept to a minimum value (by keeping a lower value of R_b). In a CT, the current flowing through the burden resistor is the sum of the magnetizing current and stepped down input current, as shown in Figure 6 (here, the core loss current is assumed to be negligible). An expression for the current flowing through the burden resistor, R_b, for the CT shown in Figure 6 is given by Equation 1.

EQUATION 1:

$$i'_{INS} = i_{INS} + i_{LM}$$

FIGURE 6: CURRENT TRANSFORMER



The aim is to minimize the magnetizing current, i_{LM}, to obtain a true reflection of the primary current ($i'_{INS} \approx i_{INS}$). The magnetizing current is directly proportional to the voltage across the secondary terminals and inversely proportional to the square of the secondary side turns of the CT($i_{LM} \alpha \frac{V_b}{N_{CT}^2}$).

To minimize i_{LM}, it is recommended to increase the turns of the CT secondary winding while keeping burden resistance at a low value. This implies that the inherent gain of the CT has to be kept to a minimum value for a desired replication of the current through the primary winding. This gain reduction has a disadvantage of having poor Signal-to-Noise Ratio (SNR) at low currents in the primary winding of the CT. To overcome this shortcoming, a linear amplifier is chosen to amplify the voltage across R_b while N_{CT} is increased. Figure 7 shows the schematic of the CT network.

FIGURE 7: SCHEMATIC OF CURRENT SENSE NETWORK

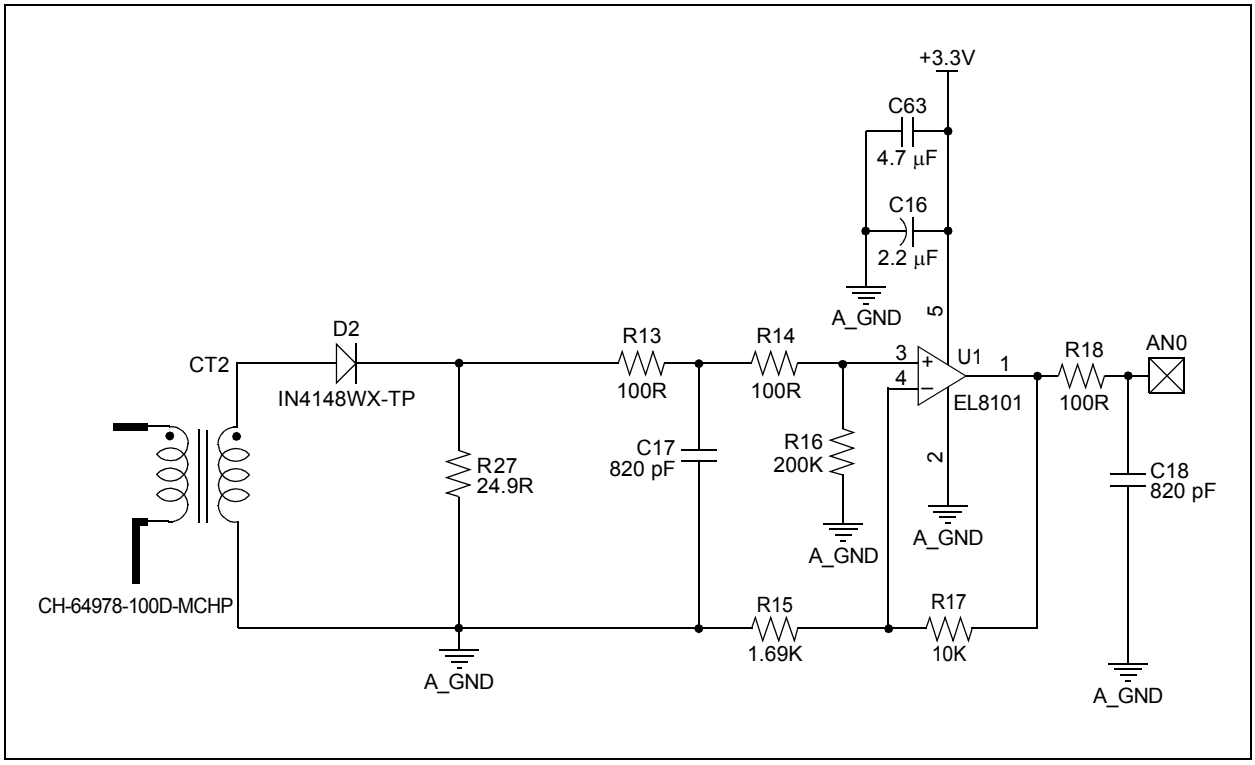


Figure 7 shows two low-pass filters: one at the input of the amplifier and another at the output of the amplifier. The corner frequency of the resulting second order filter has been chosen, such that it eliminates the high-frequency switching noise present in the current waveform. The filter stage transfer function is given by Equation 2.

EQUATION 2:

$$G_{i\_filter}(s) = \frac{1}{(1 + R13 \times C17 \times s)(1 + R18 \times C18 \times s)}$$

Here, C17 = C18 = 820 pF and R13 = R18 = 100Ω, resulting in a corner frequency of 1.24 MHz. This is sufficient to eliminate all the switching frequency noise components without inducing a phase lag to the sensed current.

The gain of the CT is given by Equation 3.

EQUATION 3:

$$K_{CT} = \frac{R27}{N_{CT}}$$

Where, R27 = R_b = 24.9Ω and N_{CT} = 200, resulting in a K_{CT} value of 0.1245Ω.

To amplify the current sense network gain, a high bandwidth non-inverting amplifier is connected to the burden resistor, R27 (U1 in Figure 6). An expression for the non-inverting amplifier gain is given by Equation 4.

EQUATION 4:

$$K_{amp} = \frac{R16}{R14 + R16}\left(1 + \frac{R17}{R15}\right)$$

Here, R14 = 100Ω, R16 = 200 kΩ, R17 = 10 kΩ and R15 = 1.69 kΩ, resulting in a K_{amp} of 6.91.

Thus, the total gain of the current sensing network, K_{isense}, is given by Equation 5.

EQUATION 5:

$$K_{isense} = K_{CT} \times G_{i\_filter} \times K_{amp}$$

Substituting the values for K_{CT} and K_{amp} gives K_{isense} = 0.86 $G_{i\_filter}(s)$.

For an inductor current frequency of 2 Fsw, the gain offered by the filtered stage $G_{i\_filter}(s)$ can be considered unity. Thus, the nominal gain of the current sense network is 0.86Ω.

Considering the reference voltage of the ADC (ADC_REF) as 3.3V, the base current of the system corresponding to a current sensor gain of K_{isense} is given by the expression, ADC_REF/K_{isense}, resulting in a value of 3.83A ($I_{basepri}$) on the primary side and 95.8A ($I_{basesec}$) when reflected on the secondary side.

OUTPUT VOLTAGE

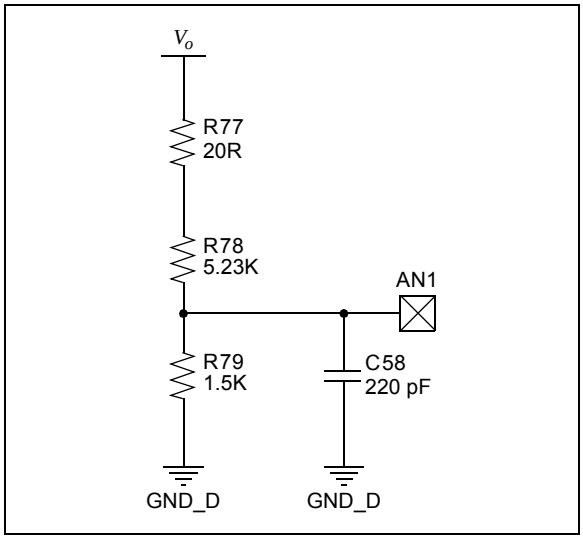
The output voltage is sensed using a resistor divider network, as shown in Figure 8. The expression for the gain of the output voltage sense network is given as seen in Equation 6.

EQUATION 6:

$$K_{VO} = \frac{R79}{(R77 + R78 + R79)}\left(\frac{1}{1 + \frac{R79(R77 + R78)}{(R77 + R78 + R79)} \times C58 \times s}\right)$$

The resistance, R77 (20Ω), is basically used as an injection resistor to be used in conjunction with the injection transformer of a network analyzer to measure the loop gain. The values, R79 and R78, were chosen to result in a base voltage (V_{base}) value of 14.8V for achieving a good dynamic range of the output voltage over the nominal value of 12V. In other words, the gain of the voltage sense network, K_{VO}, is ADC_REF/V_{base}. From Figure 8, R78 = 5.23 kΩ and R79 = 1.5 kΩ, resulting in a K_{VO} of 0.222.

FIGURE 8: OUTPUT VOLTAGE FEEDBACK NETWORK



It is also important to choose an appropriate filter capacitor, C_f (C58 in Figure 8), for filtering out high-frequency noise from the feedback signal. For the output voltage feedback, it is essential to retain the switching frequency components while eliminating only the high-frequency components and minimizing the phase lag at the switching frequency. Hence, the corner frequency was placed approximately a decade above the switching frequency. The value of C58 was chosen to be 220 pF for obtaining a corner frequency of ~600 kHz.

INPUT VOLTAGE

A real-time measurement of the input voltage is essential for the implementation of digital slope compensation. As shown in Figure 5, the Digital Signal Controller is essentially referenced to the same ground as the output voltage for the following reasons:

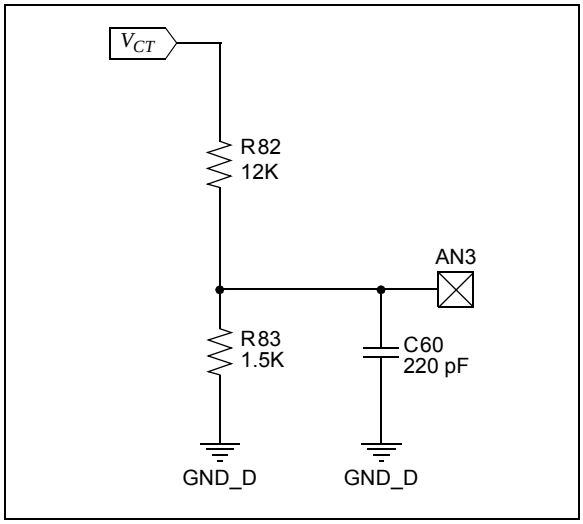
- The output voltage feedback can be non-isolated
- No isolation is needed for communication networks as they are referenced to the low-voltage side

As the input voltage has to be measured across the isolation barrier, an expensive linear opto amplifier is required, and therefore, not a preferred solution. An alternate approach is to sense the voltage at the center tap point of the transformer secondary winding, with respect to the output ground, during the power delivery cycles (t1 and t3 in Figure 4). During the power delivery intervals, the applied input voltage is reflected across the secondary winding. This measurement can be accomplished using a resistor divider network, as shown in Figure 9. The expression for the gain of the input voltage sense network is given by Equation 7.

EQUATION 7:

$$K_{VIN} = \frac{R83}{(R82 + R83)}\left(\frac{1}{1 + \frac{R82 \times R83}{(R82 + R83)} \times C60 \times s}\right)$$

FIGURE 9: INPUT VOLTAGE FEEDBACK NETWORK



The gain of the input voltage sensor has to be chosen to cover input voltages up to 450V for a greater dynamic range. For a transformer (TX) turns ratio of 25:1:1 (K_{VIN}), the gain for a full-scale voltage of the ADC pin is given by the expression, $ADC\_REF/VIN\_MAX/N$, which translates to a value of 0.1833.

Thus, the resulting base value for the input voltage sensor ($V_{baseinput}$) is 18V (ADC_REF/K_{VIN}).

Since the base voltage of the system (V_{base}) is chosen to be 14.8V, a change of base for the measured input voltage is required. This implies that the sensed digital input voltage has to be scaled by a factor, $V_{baseinput}/V_{base}$, which translates to a value of 1.26. Implementing this scale factor in the microcontroller will consist of a multiplication and shift factor applied to the sampled input voltage. A better method is to choose the sensor gain for the input voltage to be half of the sensor gain of the output voltage, so that the change of base scaling translates to a value of 2, while the dynamic range is satisfied. Thus, choosing a sensor gain, K_{VIN}, of 0.111 gives the change of base scaling of 2 for the input voltage measurement. This is achieved easily by a left shift of the measured digital input voltage by 1 bit. Substituting R82 = 12 kΩ and R83 = 1.5 kΩ gives a gain of 0.111. For the filter capacitor, C60, the same value of 220 pF was chosen, resulting in a corner frequency of ~542 kHz, which is sufficient for filtering the high-frequency noise with minimal phase lag.

DIGITAL SLOPE COMPENSATION

The key feature of this reference design is the implementation of peak current control with a Microchip patented, software-based slope compensation algorithm [1]. Peak Current-Mode Control (PCMC) and its applications in control of power converters are well researched topics in literature. This control technique has many advantages when compared to Voltage mode control.

A few key advantages are:

- Excellent dynamic response
- Dynamic flux balancing, precluding the use of series blocking capacitors in transformer-based converters
- Inherent line feed-forward

The well-known phenomenon of subharmonic oscillations for duty cycles greater than 50% is typically overcome by hardware-based slope compensation circuits. The slope compensation ramp, shown in Figure 2, is typically achieved using an RC network, along with a transistor for resetting the capacitor at the end of every inductor current cycle.

The proposed software-based slope compensation technique eliminates the usage of external components for slope compensation, hence, it improves the reliability of the overall system. Further, since the technique is software-based, it is possible to implement an adaptive slope compensation where the slope can be adjusted relative to the variation of the input voltage and output voltage. This helps in achieving an optimal slope compensation (deadbeat) across line and load conditions. This section provides a mathematical derivation of the expression for digital slope compensation.

Consider the inductor current for one cycle, shown in Figure 10. Here, i_c is the control reference obtained from the digital voltage compensator, i_{cmp} is the slope compensated peak current reference and i_L is the inductor current. The rising slope (power delivery) of the inductor current is m_1 and the falling slope (freewheeling) is m_2. The switching period is given by T_s, the inductor current rise time is given by dT_s and the fall time is given by $d'T_s$, where $d' = 1 - d$.

FIGURE 10: INDUCTOR CURRENT WAVEFORM WITH COMPENSATION SLOPE

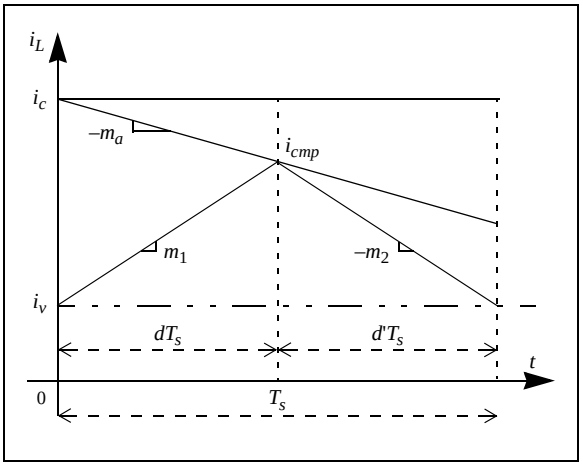


Figure 10 shows that:

EQUATION 8:

$$i_c - m_a dT_s = i_{cmp}$$

EQUATION 9:

$$i_v + m_1 dT_s = i_{cmp}$$

From Equation 8:

EQUATION 10:

$$d = (i_c - i_{cmp})\frac{1}{m_a T_s}$$

Substituting Equation 10 in Equation 9 and rearranging the terms gives Equation 11.

EQUATION 11:

$$i_{cmp} = \frac{m_a i_v}{(m_1 + m_a)} + \frac{m_1 i_c}{(m_1 + m_a)}$$

Equation 11 can be written in a general form as Equation 12.

EQUATION 12:

$$i_{cmp} = Ai_v + Bi_c$$

Where:

$$A = \frac{m_a}{(m_1 + m_a)}$$

$$B = \frac{m_1}{(m_1 + m_a)}$$

It can be seen that $A + B = 1$. Therefore, if A is determined, then B can be determined by using Equation 13.

EQUATION 13:

$$B = 1 - A$$

It is known that the slope of the compensation ramp must satisfy $m_a > \frac{1}{2}(m_1 + m_2)$ and an optimum value is achieved when $m_a = m_2$.

EQUATION 14:

$$\frac{1}{2}(m_1 + m_2) < m_a \leq m_2$$

Therefore, m_a has a range given by Equation 14. Dividing Equation 14 by m_2 yields Equation 15.

EQUATION 15:

$$\frac{1}{2}\left(\frac{m_1}{m_2} + 1\right) < \frac{m_a}{m_2} \leq 1$$

If m_a is varied proportional to m_2, then:

EQUATION 16:

$$m_a = km_2$$

Where: $k \leq 1$

Substituting Equation 16 in Equation 15 yields Equation 17.

EQUATION 17:

$$\frac{1}{2}\left(\frac{m_1}{m_2} + 1\right) < k \leq 1$$

From Equation 17, k has the range $\left(\left(0.5 + 0.5\frac{m_1}{m_2}\right), 1\right)$.

Substituting Equation 16 in expression for A gives Equation 18.

EQUATION 18:

$$A = \frac{km_2}{(m_1 + km_2)}$$

The ZVS FB Converter is essentially a buck derived topology. For the ZVS FB Converter, the slopes, m_1 and m_2 are essentially the same as that of a Buck Converter and are given by:

$m_1 = \frac{v_{in} - v_o}{L}$ and $m_2 = \frac{v_o}{L}$

Here, v_{in} is the input voltage on the primary side (v_{inpri}), referred to the secondary side ($\frac{v_{inpri}}{N}$), where N is the turns ratio of the transformer.

Substituting the expressions of m_1 and m_2 for a ZVS FB Converter in Equation 18 yields Equation 19.

EQUATION 19:

$$A = \frac{k\frac{v_o}{L}}{\left(\frac{v_{in} - v_o}{L} + k\frac{v_o}{L}\right)} = \frac{kv_o}{v_{in} - v_o + kv_o}$$

EQUATION 20:

$$B = \frac{(v_{in} - v_o)}{v_{in} - v_o + kv_o}$$

For achieving an optimal slope compensation, $k = 1$ can be substituted (for deadbeat response) in Equation 19 and Equation 20, and the expression for the slope compensated peak current reference is obtained in Equation 21.

EQUATION 21:

$$i_{cmp} = di_v + d'i_c$$

Where:

$d = \frac{v_o}{v_{in}}$ and $d' = 1 - d$ and i_v is the valley current at the beginning of every inductor current cycle, as shown in Figure 4.

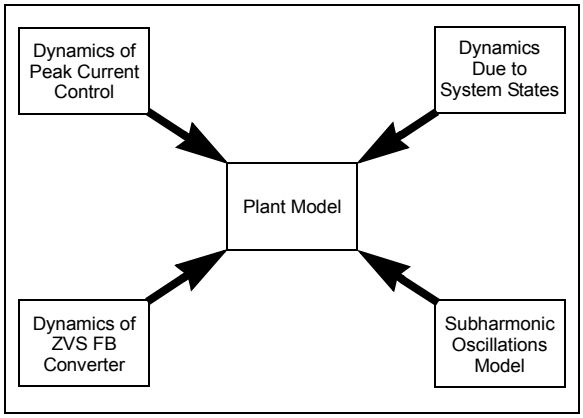
The slope compensation algorithm is given by Equation 21. This equation has to be implemented in software with the least possible latency at the beginning of every inductor current cycle, after measurement of the valley current, i_v. It can be seen from Equation 21 that d and d' are dependent on the input and output voltages, and i_c is the output of the digital voltage compensator. These three signals (d, d' and i_c) can be computed at a slower rate (with respect to the inductor current frequency) since the voltages change at a much slower rate. Also, the compensator output changes at a slower rate. The valley current, however, could change dynamically on a cycle-by-cycle basis. It should be noted that for a ZVS FB Converter, the peak current reference generated by the voltage compensator has to be held constant over even numbers of inductor current cycles (two inductor current cycles constitute one PWM period, and hence, one transformer current cycle) for flux balancing of the transformer. In other words, the uncompensated peak current reference (i_c) from the voltage compensator can be updated once in every two (or its multiples) inductor current cycles to achieve flux balancing. In the software implementation for a given PWM cycle, the quantities, d, d' and i_c, are computed and made available at the end of the previous PWM cycle. The valley current is measured and updated in Equation 21 at the beginning of every half PWM cycle (one inductor current cycle).

PLANT MODELING

In this section, a complete mathematical model of the plant for the peak current controlled ZVS FB Converter with digital slope compensation is derived.

The four components that constitute the plant model are shown in Figure 11.

FIGURE 11: COMPONENTS OF PLANT MODEL



In the following sections, each component is separately derived and then integrated to obtain the overall plant model that can be used to design a suitable compensator. In a peak current controlled system, the output variable to be controlled is the output voltage, v_o, and the control variable is the peak current reference, i_c. Therefore, the target plant model is to obtain the s-domain transfer function relating to the output voltage and the peak current reference.

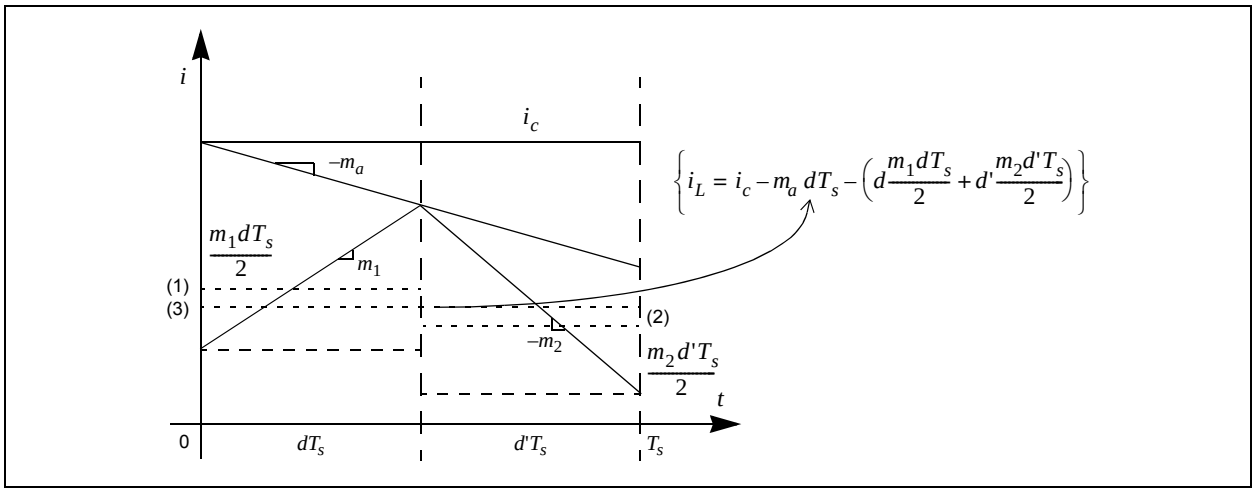
EQUATION 22:

$$G_{vic} = \frac{v_o(s)}{i_c(s)}$$

Dynamics of Peak Current Control

Consider the waveform of inductor current, as shown in Figure 12. From the figure, it can be seen that the waveform depicts a generic case where the valley current at the beginning and the end of the cycle are not equal.

FIGURE 12: INDUCTOR CURRENT WAVEFORM DEPICTING DERIVATION OF AVERAGE VALUE



From Figure 12, the average of the first triangular portion of the inductor current (corresponding to the slope, m_1, and the interval dT_s) is given by: $\frac{m_1 dT_s}{2}$

and is depicted by the dotted line (1). The average of the second triangular portion of the inductor current (corresponding to the slope, m_2, and the interval, $d'T_s$, is given by: $\frac{m_2 d'T_s}{2}$)

is depicted by the dotted line (2). The average of the two triangular portions of the inductor current over the switching period, T_s, is given by the expression:

$(d\ \frac{m_1 dT_s}{2} + d'\frac{m_2 d'T_s}{2})$.

Hence, the average inductor current over the switching period, T_s, can be obtained by subtracting the contribution of the compensation slope waveform and the average of the triangular portions of the current waveforms from the control current, i_c; this is given by Equation 23 (as shown by the dotted line (3) in Figure 12).

EQUATION 23:

$$i_L = i_c - m_a dT_s - \left(d\frac{m_1 dT_s}{2} + d'\frac{m_2 d'T_s}{2} \right)$$

Equation 23 is nonlinear and can be perturbed and linearized about an operating point comprising the nominal values of all quantities in the equation, which can be expressed as Equation 24.

EQUATION 24:

$$\begin{aligned} i_L &= I_L + \tilde{i_L} \\ i_c &= I_c + \tilde{i_c} \\ v_{in} &= V_{in} + \tilde{v_{in}} \\ m_1 &= M_1 + \tilde{m_1} \\ m_2 &= M_2 + \tilde{m_2} \\ m_a &= M_a + \tilde{m_a} \\ d &= D + \tilde{d} \\ d' &= D' - \tilde{d} \end{aligned}$$

All the terms in Equation 24, depicted by capital letters, constitute the quiescent quantities and their perturbations are appended with a '~' sign. Substituting Equation 24 in Equation 23 and eliminating all the DC terms (the terms consisting of products of the quiescent quantities), and also eliminating smaller terms (the terms consisting of products of two or more perturbations), gives the expression of a linearized average inductor current, as shown in Equation 25 [2].

EQUATION 25:

$$i_c = i_L + M_a T_s d + D T_s m_a + \frac{D^2 T_s}{2} m_1 + \frac{D'^2 T_s}{2} m_2$$

It should be noted that all time varying quantities in Equation 25 are small signal perturbations; hence, in the following mathematical expressions, the '~' sign is dropped for the sake of clarity.

For the ZVS FB Converter, the slopes, m_1 and m_2 in Figure 12, are given by Equation 26.

EQUATION 26:

$$m_1 = \frac{v_{in} - v_o}{L} \quad \text{and} \quad m_2 = \frac{v_o}{L}$$

Here, v_{in} is the input voltage on the primary side (v_{inpri}), referred to the secondary side

($\frac{v_{inpri}}{N}$ where N is the turns ratio of the transformer).

Substituting Equation 26 in Equation 25 and rearranging the terms gives Equation 27.

EQUATION 27:

$$d = F_m(i_c - i_L - F_g v_{in} - F_v v_o)$$

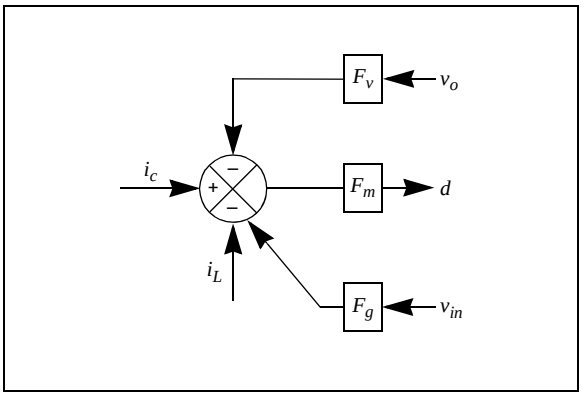
Where: $F_m = \frac{1}{M_a T_s}$

$$F_g = \frac{D^2 T_s}{2L}$$

$$F_v = \frac{(1-2D)T_s}{2L}$$

A block diagram model of Equation 27 is depicted in Figure 13.

FIGURE 13: DYNAMICS DUE TO PEAK CURRENT CONTROL AND COMPENSATION RAMP



Dynamics Due to System States

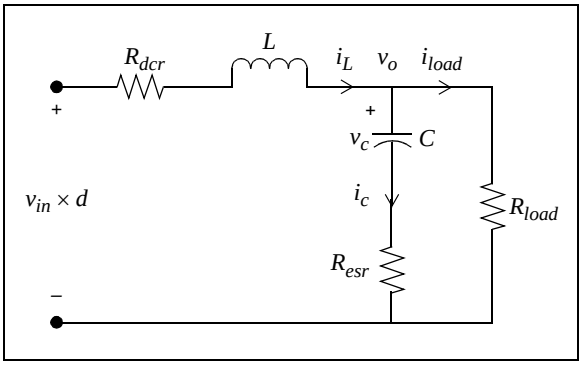
The generalized linearized, small signal model (Equation 25) relating to the control current, duty cycle and average inductor current was derived and discussed in the previous section. This model is typical for all three common converter types (Buck, Boost and Buck Boost). The specific expression related to each of the topologies can be obtained by substituting the expressions for slopes unique to each of them. As mentioned earlier, the ZVS FB is a buck derived topology. This can be readily seen by looking at the output stage (on the secondary side of transformer), which is essentially an LC low-pass filter, as shown in Figure 14. The switching network of a Buck Converter is effectively replaced by the full-bridge, the transformer and the center tapped rectifier network. The output of this switching network (comprised of the full-bridge, transformer and rectifiers) is actually the input DC voltage to the full-bridge V_{DC}, referred to the secondary side and multiplied by the effective duty cycle, d.

In Figure 14:

$$v_{in} = \frac{v_{dc}}{N}$$

is multiplied by the duty cycle ($v_{in} \times d$) and translates as an input to the LC filter.

FIGURE 14: ZVS FB OUTPUT STAGE



A small signal model of a buck derived converter can be represented in the state-space form and is shown in Equation 28.

EQUATION 28:

$$\overbrace{\begin{pmatrix} \dot{i}_L \\ \dot{v}_c \end{pmatrix}}^{\dot{x}} = \overbrace{\begin{pmatrix} \frac{-(R_{dcr}+R)}{L} & \frac{-R_1}{L} \\ \frac{R_1}{C} & \frac{-R_1}{R_{load}\,C} \end{pmatrix}}^{A} \overbrace{\begin{pmatrix} i_L \\ v_c \end{pmatrix}}^{x} + \overbrace{\begin{pmatrix} \frac{V_{IN}}{L} \\ 0 \end{pmatrix}}^{B_1} \overbrace{\tilde{d}}^{u_C} + \overbrace{\begin{pmatrix} \frac{D}{L} \\ 0 \end{pmatrix}}^{B_2} \overbrace{v_{in}}^{u_d}$$

$$\overbrace{(v_o)}^{y} = \overbrace{(R\,R_1)}^{C_v} \overbrace{\begin{pmatrix} i_L \\ v_c \end{pmatrix}}^{x}$$

In the state-space model of Equation 28:

- x is the state vector comprised of the state variables (inductor current, i_L, and capacitor voltage, v_c)
- x is the first differential of the state vector
- A is the state matrix which mainly comprises the circuit parameters, such as the filter inductance, filter capacitance, capacitor ESR, inductor DCR and load
- B_1 is the control vector that relates the states to the control input, d (duty cycle)
- B_2 is the input vector which relates the states to the input voltage
- y is the output (in Equation 28, this output is chosen to be the output voltage)
- C is the output matrix (and could be different depending on the output chosen)

The two output matrices corresponding to the output voltage (C_v) and inductor current (C_i) are shown in Equation 29.

EQUATION 29:

$$C_v = (R\,R_1)$$

$$C_i = (1\ 0)$$

Where: $R = \dfrac{R_{esr} \bullet R_{load}}{(R_{esr} + R_{load})}$

$$R_1 = \frac{R_{load}}{(R_{esr} + R_{load})}$$

The target plant model is to obtain an expression between the output voltage and the peak current reference, as shown in Equation 22. In peak current control, the peak current reference dictates the effective duty cycle. This is different from a Voltage mode control or an Average Current mode control scheme, where the duty cycle is the control variable. Hence, there is a need to eliminate the intermediate control variable, duty cycle (d), from Equation 25. To eliminate the duty cycle variable, the requirement is to obtain a small signal transfer function, relating the duty cycle to the output voltage, and the small signal transfer function, relating the duty cycle to the inductor current. To obtain the transfer functions, the time domain state-space model (Equation 28) is converted to s-domain, as shown in Equation 30.

EQUATION 30:

$$\overbrace{\begin{pmatrix} i_L \\ v_c \end{pmatrix}}^{x} = \overbrace{\begin{pmatrix} \frac{-(R_{dcr}+R)}{sL} & \frac{-R_1}{sL} \\ \frac{R_1}{sC} & \frac{-R_1}{sR_{load}C} \end{pmatrix}}^{A} \overbrace{\begin{pmatrix} i_L \\ v_c \end{pmatrix}}^{x} + \overbrace{\begin{pmatrix} \frac{V_{IN}}{sL} \\ 0 \end{pmatrix}}^{B_1} \underbrace{u_C}_{\tilde{d}} + \overbrace{\begin{pmatrix} \frac{D}{sL} \\ 0 \end{pmatrix}}^{B_2} \underbrace{u_d}_{v_{in}}$$

$$\underbrace{y}_{(v_o)} = \underbrace{C_v}_{(R\,R_1)} \overbrace{\begin{pmatrix} i_L \\ v_c \end{pmatrix}}^{x}$$

From the s-domain state-space model of Equation 30, a small signal expression relating the states and the duty cycle, or the input voltage, can be obtained. It should be noted that the model in Equation 30 is incomplete without incorporation of the dynamics of the resonant inductor, which is unique to the ZVS FB topology. In the next section, the model in Equation 30 is modified to incorporate the ZVS FB dynamics.

Dynamics of ZVS FB Model

As mentioned earlier, by observing the output stage of the ZVS FB Converter (in Figure 14), it is evident that the converter is essentially a buck derived topology. Similar to a Buck Converter, the voltage at the switching node is essentially the input voltage multiplied by duty ratio ($v_{in} \times d$), followed by a low-pass filter stage. However, the difference arises in the way in which the switching node voltage is produced. In the case of the ZVS FB Converter, this is achieved by the full-bridge MOSFETs, followed by the transformer and the center tapped full wave rectifier, as shown in Figure 1. The input node in Figure 14 is actually the center tap point on the secondary side of the transformer, where the filter inductor connects to the transformer, as shown in Figure 5. One major difference that eliminates the usage of the state-space equations of the Buck Converter for the ZVS FB Converter is the presence of the resonant inductor on the primary side of the transformer. This inductor causes significant alteration to the state equations and the Buck Converter model has to be suitably modified to incorporate the dynamics due to the resonant inductor. The effect of the dynamics, due to the overall system model, is derived in this section [3].

In most of the ZVS FB applications, the resonant inductor is built-in as the leakage inductance of the transformer (L_{lk}). The resonant inductor essentially erodes the effective duty cycle seen by the converter [3]. The amount of duty cycle erosion due to the resonant inductance is affected by both the input voltage to the full-bridge (V_{IN}) and the load current (i_L), as shown in Figure 15. The effective duty cycle is given in Equation 31.

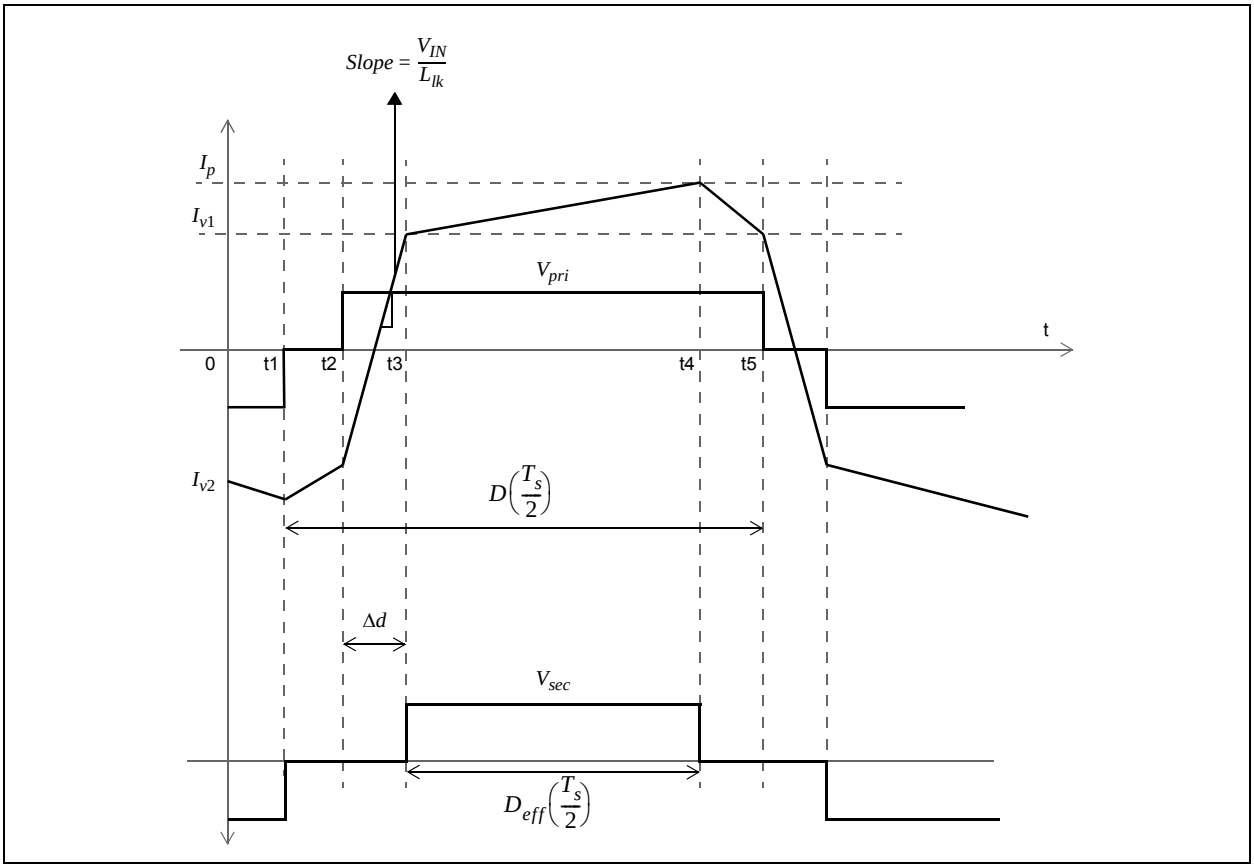
EQUATION 31:

$$d_{eff} = d_c + d_i + d_v$$

Where:

- d_c is the programmed duty cycle due to controller action (in this case, effective duty cycle due to peak current control)
- d_i is the duty cycle due to load current
- d_v is the duty cycle due to input voltage

FIGURE 15: TRANSFORMER CURRENT AND EFFECTIVE DUTY CYCLE



In Figure 15, it is observed that the duty cycle seen in the secondary side of the transformer is lower than the duty cycle seen in the primary side. When the diagonal switches turn on, starting the power delivery cycle, the transformer current (i_{pri}), reverses direction with a slope defined by Equation 32.

EQUATION 32:

$$L_{lk}\frac{\Delta i}{\Delta t} = v_{in}$$

At steady state, the valley point of the inductor current is reflected in the transformer primary current as i_{v1} and i_{v2}, as shown in Figure 15. Here, it is assumed that the magnetizing current of the transformer is negligible and $i_{v1} = i_{v2}$. Rearranging Equation 32 gives Equation 33.

EQUATION 33:

$$\Delta t = \Delta d\left(\frac{T_s}{2}\right) = \frac{L_{lk}}{v_{in}}(\Delta i) = \frac{L_{lk}}{v_{in}}(i_{v1} + i_{v2})$$

Equation 34 can be derived from Equation 33.

EQUATION 34:

$$\Delta d = \frac{L_{lk}}{v_{in}\left(\frac{T_s}{2}\right)}(i_{v1} + i_{v2})$$

In the steady state, the valley currents in the inductor are nothing but average inductor current adjusted for the ripple value, as shown in Equation 35.

EQUATION 35:

$$i_{v1} = i_{v2} = \frac{\left(i_L - \frac{\Delta i_L}{2}\right)}{N}$$

For the ZVS FB Converter, inductor ripple current ($\frac{\Delta i_L}{2}$) is given by Equation 36.

EQUATION 36:

$$\frac{\Delta i_L}{2} = v_o D' T_s / 2L$$

Substituting Equation 36 in Equation 35 gives Equation 37.

EQUATION 37:

$$\Delta d = \frac{NL_{lk}(4\, i_L - V_o D' T_s / L)}{v_{in} T_s}$$

As seen from Equation 37, the duty cycle correction factor is a function of the input voltage, output voltage, inductor current and the switching frequency, and also, the resonant inductance.

EQUATION 38:

$$\Delta d = f(v_{in}, i_L, L_{lk}, T_s, v_o)$$

Since the T_s, L_{lk} and the output voltage are fixed, the duty cycle correction factor can be considered as a function of the input voltage and load current.

EQUATION 39:

$$\Delta d = f(v_{in}, i_L)$$

EQUATION 40:

$$\Delta d = \Delta d_i + \Delta d_v$$

The differentiation of Δd in Equation 37, with respect to i_L keeping the input voltage fixed, yields the sensitivity of the of duty cycle due to load current, as given in Equation 41.

EQUATION 41:

$$\Delta d_i = \tilde{d}_i = \frac{-R_d}{NV_{IN}}\tilde{i_L}$$

Similarly, differentiation of Δd in Equation 53, with respect to v_{IN}, keeping the load current fixed yields the sensitivity of the duty cycle due to input voltage, as seen in Equation 42.

EQUATION 42:

$$\Delta d_v = \tilde{d}_v = \frac{-R_d}{NV_{IN}^2}\left(I_L - \frac{V_o D' T_s}{4L}\right)\tilde{v_{in}}$$

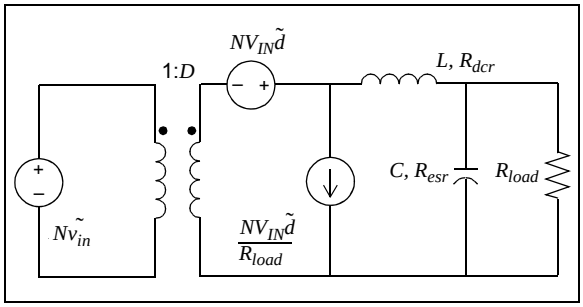
Where:

EQUATION 43:

$$R_d = 4N^2\frac{L_{lk}}{T_s}$$

It should be noted that the term, R_d in Equation 43, has the unit of resistance. Deriving Equation 41 and Equation 42 ensures that all the components for obtaining the effective duty cycle in Equation 31 are available. The small signal model of the secondary side of the ZVS FB Converter, without considering the resonant inductor as derived in Equation 30, is shown in Figure 16.

FIGURE 16: SMALL SIGNAL MODEL OF SECONDARY STAGE OF ZVS FB CONVERTER WITHOUT RESONANT INDUCTOR DYNAMICS



Replacing $\tilde{d}$ with $(\tilde{d}_{eff})$ in Figure 16 results in showing the small signal model of the ZVS FB Converter and the dynamics consideration due to the resonant inductor, as shown in Figure 17. The small signal model for the ZVS FB Converter is shown in Equation 44.

EQUATION 44:

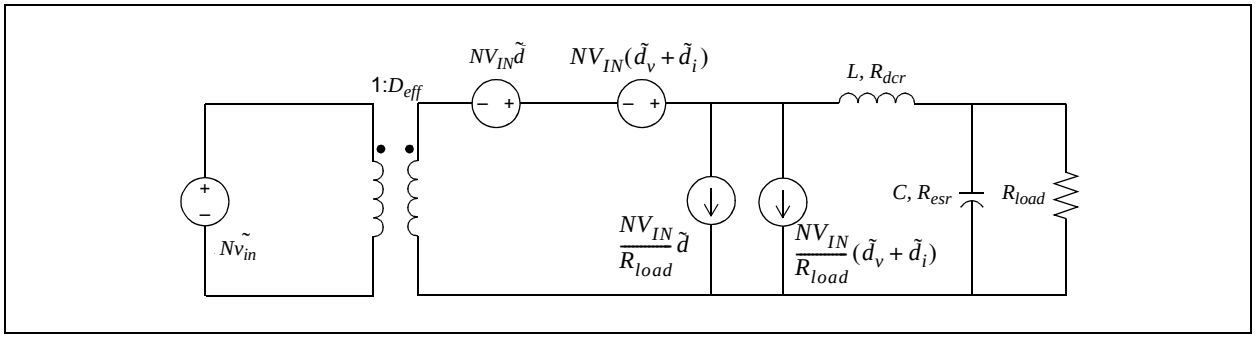
$$\overbrace{\begin{pmatrix}\dot{i}_L\\ \dot{v}_c\end{pmatrix}}^{\dot{x}} = \overbrace{\begin{pmatrix}\frac{-(R_{dcr}+R+R_d)}{L} & \frac{-R_1}{L}\\ \frac{R_1}{C} & \frac{-R_1}{R_{load}C}\end{pmatrix}}^{A}\overbrace{\begin{pmatrix}i_L\\ v_c\end{pmatrix}}^{x} + \overbrace{\begin{pmatrix}\frac{V_{INS}}{L}\\ 0\end{pmatrix}}^{B_1}\underbrace{u_C}_{\tilde{d}} + \overbrace{\begin{pmatrix}\frac{\left(ND+\frac{R_d k}{V_{INP}}\right)}{L}\\ 0\end{pmatrix}}^{B_2}\underbrace{u_d}_{v_{in}}$$

$$\underbrace{(v_o)}_{y} = \overbrace{(R\ R_1)}^{C_v}\overbrace{\begin{pmatrix}i_L\\ v_c\end{pmatrix}}^{x}$$

Where $k = I_{load} - \frac{V_o D' 2T_s}{4L}$, and R and $R1$ are as defined in Equation 29.

As seen in Equation 44, the term, R_d, which is dependent on the resonant inductance, increases the overall damping of the system as it adds with the inductor DCR. From Equation 44, all transfer functions for the ZVS FB can be derived. Figure 17 shows the modified small signal model achieved after including the duty cycle terms due to load current variation and input voltage variation.

FIGURE 17: SMALL SIGNAL MODEL OF ZVS FB CONVERTER WITH RESONANT INDUCTOR DYNAMICS



The output voltage to duty cycle transfer function, $G_{vd}(s)$, is given by Equation 45.

EQUATION 45:

$$G_{vd}(s) = \frac{v_o(s)}{d(s)}$$

$$G_{vd}(s) = C_v(SI - A)^{-1}B$$

$$G_{vd}(s) = \frac{\frac{V_g}{L}\left(R\left(s + \frac{R}{CR_{load}R_{esr}}\right) + \frac{R^2}{CR_{esr}}\right)}{den}$$

Where:

$$den = S^2 + \left(\frac{R}{CR_{load}R_{esr}} + \frac{(R_{dcr} + R_d + R)}{L}\right)S + \left(\frac{(R_{dcr} + R_d + R)R}{LCR_{load}R_{esr}} + \frac{R^2}{LCR_{esr}^2}\right)$$

The inductor current to duty cycle transfer function, $G_{id}(s)$, is given by Equation 46.

EQUATION 46:

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = C_i(SI - A)^{-1}B$$

$$G_{id}(s) = \frac{\frac{v_g}{L}\left(s + \frac{R}{CR_{load}R_{esr}}\right)}{den}$$

The output voltage to disturbance (v_{in}) transfer function, $G_{vg}(s)$, is given by Equation 47.

EQUATION 47:

$$G_{vg}(s) = \frac{v_o(s)}{v_{in}(s)} = C_v(SI - A)^{-1}B_1$$

The inductor current to disturbance (v_{in}) transfer function, $G_{vd}(s)$, is given by Equation 48.

EQUATION 48:

$$G_{ig}(s) = \frac{i_L(s)}{v_{in}(s)} = C_i(SI - A)^{-1}B_1$$

In the range, Equation 45 to Equation 48, the matrix, I, that is used is a second order identity matrix:

$$I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

By using Equation 45 through Equation 48, the linearized small signal expressions, relating system states to the control and disturbance inputs can be derived, as shown in Equation 49 and Equation 50.

EQUATION 49:

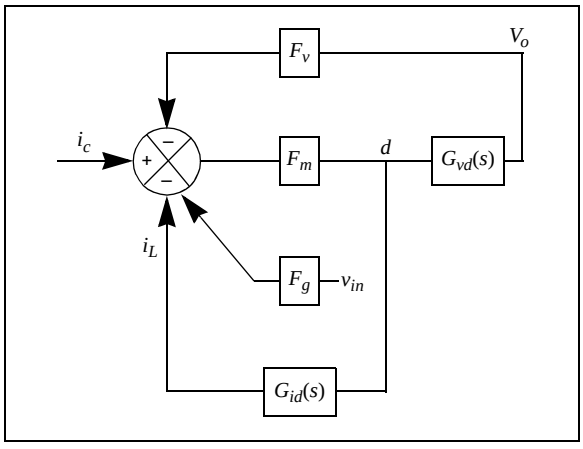
$$v_o(s) = G_{vd}(s)\big|_{v_{in}=0}d(s) + G_{vg}(s)\big|_{d=0}v_{in}(s)$$

EQUATION 50:

$$i_L(s) = G_{id}(s)\big|_{v_{in}=0}d(s) + G_{ig}(s)\big|_{d=0}v_{in}(s)$$

Combining Equation 45 and Equation 46 with Equation 27, and eliminating d, gives the small signal model shown in Figure 18. From Figure 18, a relationship between the output voltage and the peak current reference can be obtained, as shown in Equation 51.

FIGURE 18: SMALL SIGNAL MODEL



EQUATION 51:

$$G_{vc}(s) = \frac{v_o(s)}{i_c(s)} = \frac{F_m G_{vd}(s)}{(1 + F_m(G_{id}(s) + F_v G_{vd}(s)))}$$

Subharmonic Oscillation Model

A well-known artifact in peak current controlled converters is the subharmonic oscillations, seen in the inductor current, for duty ratios larger than 50% (shown in Figure B-3). The subharmonic oscillations in the inductor current occur at multiples of the PWM switching frequency. The plant model for peak current control (Equation 51) is incomplete without incorporation of a suitable model to mathematically describe these subharmonic oscillations.

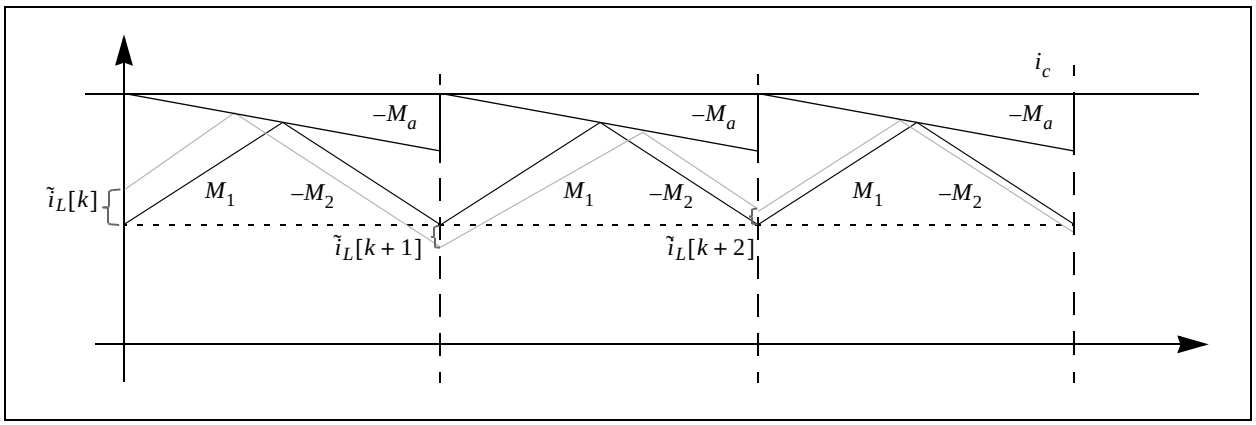
Considering the waveform in Figure 19, and assuming that the system voltages, control reference current (i_c) and the compensation slope are constant, the effect of a perturbation in the inductor current at the beginning of k^{th} cycle given by $\tilde{i}_L[k]$ at any of the subsequent cycles can be computed. From Figure 19 it can be seen that the inductor current perturbation at any k^{th} cycle can be described by Equation 52.

EQUATION 52:

$$\tilde{i}_L[k] = -\alpha\tilde{i}_L[k-1] + (1+\alpha)\tilde{i}_c[k]$$

Where: $$\alpha = \frac{M_2 - M_a}{M_1 + M_a}$$

FIGURE 19: WAVEFORM SHOWING THE PERTURBATION IN INDUCTOR CURRENT



A z-transform of Equation 52 yields:

EQUATION 53:

$$\frac{\tilde{i}_L[z]}{\tilde{i}_c[z]} = (1+\alpha)\frac{z}{(z+\alpha)}$$

To obtain a continuous time relationship between the inductor current perturbation and the control current, substitute $z = e^{sT_s}$ in Equation 53 and convolve with the ZOH transfer function (Equation 54) to obtain Equation 55 [2] [4].

EQUATION 54:

$$ZOH = \frac{(1 - e^{-sT_s})}{sT_s}$$

EQUATION 55:

$$\frac{\tilde{i}_L[s]}{\tilde{i}_c[s]} = (1+\alpha)\frac{e^{sT_s}}{(e^{sT_s}+\alpha)}\frac{(1-e^{-sT_s})}{sT_s}$$

Applying a second order Padé approximation for e^{-sT_s}, as shown in Equation 56.

EQUATION 56:

$$e^{-sT_s} = \frac{\left(1 - \frac{\pi}{2}\left(\frac{s}{\frac{\omega_s}{2}}\right) + \left(\frac{s}{\frac{\omega_s}{2}}\right)^2\right)}{\left(1 + \frac{\pi}{2}\left(\frac{s}{\frac{\omega_s}{2}}\right) + \left(\frac{s}{\frac{\omega_s}{2}}\right)^2\right)}$$

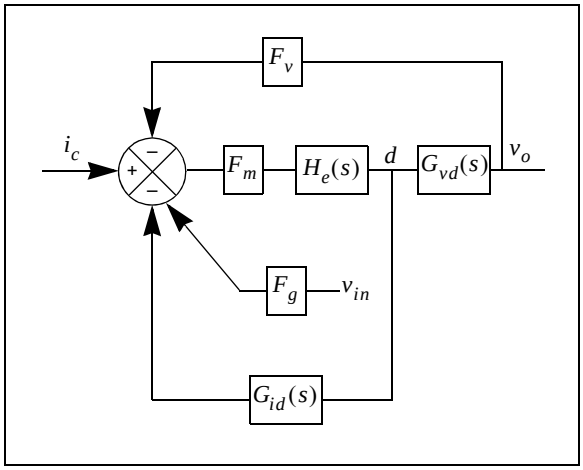
Substituting Equation 56 in Equation 55 and simplification yields Equation 57.

EQUATION 57:

$$\frac{\tilde{i}_L[s]}{\tilde{i}_c[s]} = \frac{1}{1 + \frac{\pi}{2}\left(\frac{2}{1+\alpha} - 1\right)\frac{s}{\frac{\omega_s}{2}} + \left(\frac{s}{\frac{\omega_s}{2}}\right)^2}$$

The model in Equation 57 can be incorporated to the small signal model (Equation 51) by matching both at high frequencies. The model with the incorporated high-frequency effects is shown in Figure 20.

FIGURE 20: PLANT MODEL WITH HIGH-FREQUENCY DYNAMICS INCLUDED



In Figure 20, the high-frequency model term, $H_e(s)$, is given by Equation 58.

EQUATION 58:

$$H_e(s) = \frac{1}{\left(1+\frac{s}{\omega_P}\right)}$$

Where:

$$\omega_P = 2\pi f_s \frac{\pi}{4}\left(\frac{2}{1+\alpha}-1\right)$$

$$\alpha = \frac{M_2 - M_a}{M_1 + M_a}$$

The final small signal relationship between the output voltage and the control current corresponding to Figure 20 is given by Equation 59.

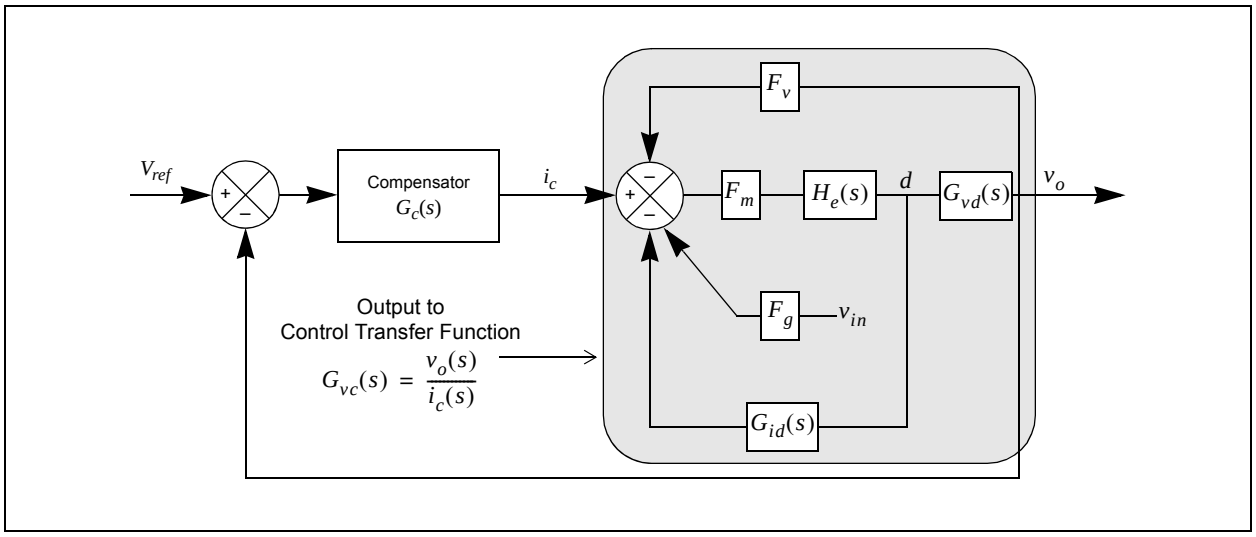
EQUATION 59:

$$G_{vc}(s) = \frac{v_o(s)}{i_c(s)} = \frac{F_m G_{vd}(s)}{(1 + F_m H_e(s)(G_{id}(s) + F_m G_{vd}(s)))}$$

CONTROL SYSTEM DESIGN

In this section, the plant model derived in the previous section is used to design a suitable control system. The control block diagram for a peak current controlled ZVS FB Converter is shown in Figure 21. The output voltage to control the input transfer function can be derived by block diagram reduction of the highlighted portion in Figure 21. The expressions for F_v, F_m and F_g are obtained in the **"Dynamics of Peak Current Control"** section. The expression for $H_e(s)$ is obtained in the **"Subharmonic Oscillation Model"** section. The expressions for $G_{vd}(s)$ and $G_{id}(s)$ for the ZVS FB are obtained in the **"Dynamics of ZVS FB Model"** section, from Equation 45 and Equation 46.

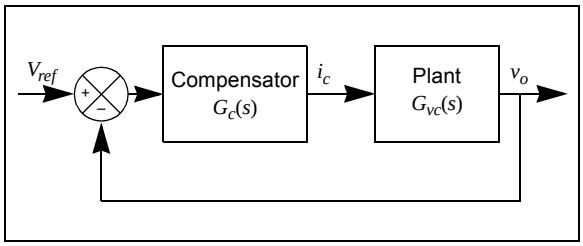
FIGURE 21: CONTROL BLOCK DIAGRAM



The expression for output voltage to control input, $G_{vc}(s)$, is obtained in Equation 59.

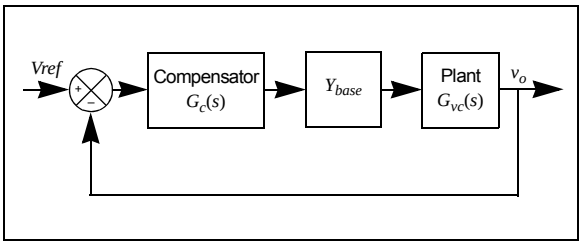
Equation 59 gives the plant transfer function for a peak current controlled system. Substituting the expressions in Equation 45 and Equation 46 for $G_{vd}(s)$ and $G_{id}(s)$ in Equation 59 gives the plant transfer function for the ZVS FB Converter. A simplified control block diagram is shown in Figure 22. A suitable compensator is designed considering this plant transfer function, $G_{vc}(s)$.

FIGURE 22: SIMPLIFIED CONTROL BLOCK DIAGRAM



In Figure 22, the effect of feedback sensing networks is not considered. However, in real-time systems, sensing networks are required to measure voltages and currents. For closed-loop control of the peak current controlled ZVS FB, the inductor current, input voltage and output voltages are sensed, as discussed in the **"Digital Control of ZVS FB Converter with Digital Slope Compensation"** section. In real-time control, the feedback of the output voltage is per-unitized with respect to V_{base} and the inductor current feedback is per-unitized with respect to I_{base}, as discussed earlier. Therefore, the open-loop transfer function of the model has to be multiplied by a factor of Y_{base} (I_{base}/V_{base}), referred to the secondary side of the transformer to match the loop gain response obtained from the hardware, as shown in Figure 23.

FIGURE 23: CLOSED-LOOP CONSIDERING SENSOR GAIN SCALING



The nominal values of the components of the plant are given in Table 2. By substituting these component values in Equation 45 and Equation 46, the plant transfer function with Y_{base} (Equation 60) is obtained.

EQUATION 60:

$$G_{vc}(s)Y_{base} = \frac{0.5041\left(\frac{s}{4.44\times10^{6}}+1\right)}{\left(\frac{s}{202.3\times10^{3}}+1\right)\left(\frac{s}{1643}+1\right)}$$

Equation 60 shows that the plant model effectively has a pole and a zero at very high frequencies, and there is only one pole which is at low frequency (1643 rad/sec). This is a typical characteristic of a peak current controlled system, where the pole corresponding to the inductor state is pushed to a very high frequency so its effects are practically none.

TABLE 2: NOMINAL VALUES OF PLANT COMPONENTS

Parameter	Value	Parameter	Value
R_{load}	0.1920Ω	V_g	400V
R_{esr}	0.03 mΩ	V_o	12V
Y_{der}	5 mΩ	C	7500 µF
N	25	Fsw	72.8 kHz
L	2.7 µH	M_1	$\frac{\left(\frac{V_g}{N}-V_o\right)}{L}$
L_{lk}	38 µH	M_2 (= M_a)	$\frac{(V_o)}{L}$

A PI compensator shown in Equation 61 is chosen to control the plant.

EQUATION 61:

$$G_c = k_p + \frac{k_i}{s}$$

The following are the key considerations to design the compensator:

- To achieve a phase margin > 45°
- To achieve a gain margin > 10 dB
- To achieve a crossover of 3.5 kHz
- Switching frequency attenuation ≤ 40 dB
- Open-loop: $TF = G_c(s)G_{vc}(s)G_{fb}(s)Y_{base}$
- $G_{fb}(s)$ is the transfer function of the output voltage sensor LP filter
- Choose k_p and k_i to attain the above targets

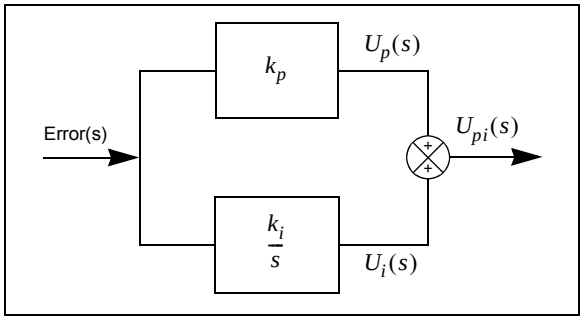
The values chosen for k_p and k_i are 18.5k and 302.5k, respectively. Thus, the PI compensator in s-domain is given by Equation 62.

EQUATION 62:

$$G_c = 18.5 + \frac{302.5k}{s}$$

The PI compensator is essentially implemented considering the proportional U_p separately and the integral output U_i separately, as shown in Figure 24.

FIGURE 24: PI COMPENSATOR BLOCK DIAGRAM



Therefore,

$$U_p(s) = k_p error(s)$$

Converting the above expression to z-domain gives:

$$U_p(z) = k_p error(z)$$

Taking an inverse z-transform of the above expression results in Equation 63.

EQUATION 63:

$$U_p[k] = k_p error[k]$$

Similarly,

$$U_i(s) = \frac{k_i}{s} error(s)$$

Converting the above expression to z-domain by applying the bilinear transformation,

$s = \frac{2}{T_s}\frac{(1-z^{-1})}{(1+z^{-1})}$, gives the following expression.

$$U_i(z) = \frac{k_i T_s}{2}\frac{(1+z^{-1})}{(1-z^{-1})} error(z)$$

Here, the sampling period (in the expression for s in bilinear transform) is the same as the switching period, T_s. Rearranging the terms in the previous expression gives:

$$U_i(z) - U_i(z)z^{-1} = \frac{k_i T_s}{2} error(z) + \frac{k_i T_s}{2} error(z)z^{-1}$$

Taking an inverse z-transform of the above equation gives Equation 64.

EQUATION 64:

$$U_i[k] = U_i[k-1] + \frac{k_i T_s}{2} error[k] + \frac{k_i T_s}{2} error[k-1]$$

Thus, the output of the digital PI compensator is given by the summation of Equation 63 and Equation 64 as Equation 65.

EQUATION 65:

$$U_{PI}[k] = k_p error[k] + U_i[k-1] + \frac{k_i T_s}{2} error[k] + \frac{k_i T_s}{2} error[k-1]$$

The difference equation in Equation 65 is implemented in the dsPIC® DSC using one multiply instruction (for U_p calculation), two MAC instructions and one summation for adding the components. From Equation 62, it is observed that the value of k_p is 18.5. To digitally implement this value in a fixed point processor, a number format of Q6.10 is chosen, since this format has a range of ±32. For the integral controller, the effective value implemented is $k_i T_s/2$, as given by Equation 64, and this translates to a value of 2.074. The Q3.13 fixed-point number format is chosen to represent $k_i T_s/2$, as this format has a dynamic range of ±4. The frequency response plot of the open-loop transfer function of the system, given by Equation 66, is shown Figure 25.

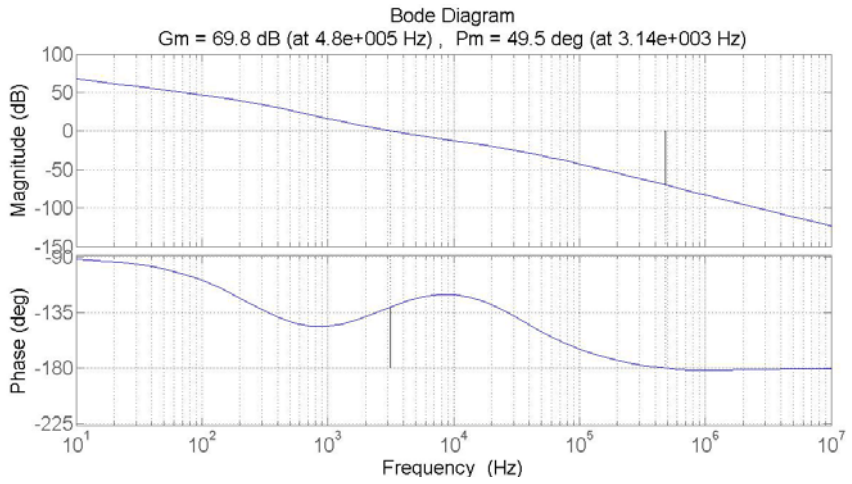
EQUATION 66:

$$G_{OLTF} = G_c G_{vc} G_{filter} Y_{base}$$

In Equation 66, G_{filter} is the same as the frequency component of the output voltage sense filter, as shown in Equation 6.

From the Bode plot of the loop gain or the open-loop transfer function ($G_{OLTF}(s)$) in Figure 25, it can be observed that all the design objectives are met.

FIGURE 25: BODE PLOT OF $G_{OLTF}(s)$



FIRMWARE IMPLEMENTATION

In this section, all the aspects related to firmware design and implementation are discussed, which include the following key features:

- dsPIC DSC used for real-time control
- Description of the key Interrupt Service Routines (ISRs)
- dsPIC DSC resources for implementing digital control
- A few techniques for efficiency improvement

Key Features of dsPIC33EP "GS" Family of Devices

In this reference design, the real-time implementation of A peak current controlled ZVS FB Converter is achieved using the dsPIC33EP64GS504 Digital Signal Controller from the dsPIC33EP "GS" family of dsPIC DSCs. This family of Digital Signal Controllers is ideal for digital power conversion applications and features high-resolution PWMs, along with high-speed 12-bit ADCs and a high-speed 12-bit DAC to use with the analog comparators. The key requirement for achieving optimal performance for digital slope compensation is fast execution time, coupled with fast and high-resolution ADCs and analog comparators. The dsPIC33EP "GS" family of devices satisfies all of the above requirements.

The following features enable implementation of digital slope compensation:

- Lower Software Execution Time
  - 70 MIPS with DSP Engine
  - Alternate Working Register Sets
- Lower ADC Conversion Latency
  - 12-Bit, 3.25 Msps (~300 ns conversion time)
  - Early Interrupt Generation
  - 4 Dedicated SAR ADC Cores and One Shared SAR ADC Core
- Fast Analog Comparator
  - Response Time of 15 ns and 12-Bit DAC

Apart from the high clock frequency of the device (70 MIPS) and low ADC conversion latency, the two key features that enable performance acceleration are the Alternate Working registers and early interrupt generation of the ADC. These two features are discussed in the following sections.

ALTERNATE WORKING REGISTERS

The dsPIC33EPXXGS50X family of devices has two additional sets of Alternate Working registers or contexts apart from the default set. These two additional Alternate Working register sets, named Context 1 (CTXT1) and Context 2 (CTXT2), can be configured to be tied to any particular Interrupt Priority Level (IPL).

For example, IPL7 can be tied to CTXT1 and IPL5 can be tied to CTXT2 using the appropriate Configuration bit settings. This will allow an ISR of IPL 7 and an ISR of IPL 5 to eliminate saving and restoring of context before and after the execution of the ISR software. When the ISR with IPL7 is invoked, the device hardware automatically switches to the Alternate Working register set corresponding to CTXT1. Similarly, when the ISR with IPL5 is invoked, the device hardware automatically switches to the Alternate Working register set corresponding to CTXT2.

For more information, refer to **"dsPIC33E Enhanced CPU"** (DS70005158) in the "*dsPIC33/PIC24 Family Reference Manual*".

EARLY INTERRUPT GENERATION

The ADC core takes a finite amount of time from the trigger for starting the conversion to the ending of the conversion. Typically, at the end of conversion, the respective ADC ISR is called and a finite amount of time (~13 T_{CY}) has elapsed before entering into the ISR. In the dsPIC33EPXXGS50X family, it is possible that the control enters the ADC ISR even while the ADC is converting, thereby masking the interrupt entry latency almost completely. This feature is specifically useful for performing tasks that are not dependent on the sampled value during the conversion process.

Device Resources and Software Architecture

Table 3 captures all the resources used for the dsPIC33EP64GS504 family of devices.

TABLE 3: DEVICE RESOURCES

Description	Device Resource
Program Memory (without compiler optimizations)	4716 bytes (11%)
Data Memory	208 bytes (3%)
MIPS Usage	20 MIPS (28.5%) [Communication ISRs are not included]
PWM Module (3 pairs)	PWM1H/1L – Full-Bridge Q1-Q2 MOSFETs PWM2H/2L – Full-Bridge Q3-Q4 MOSFETs PWM3H/3L – Synchronous Rectifiers Q5-Q6 and Q7-Q8
ADC Module	AN0 – Line Current Feedback AN1 – Output Voltage Feedback AN3 – Center Tap Voltage Feedback AN4 – Remote Voltage Feedback(1) AN10 – Load Share Reference(1) AN11 – Load Share Feedback(1)
Analog Comparator	CMP3C – Line Current for Peak Current Control CMP2D – Output Voltage Fault
GPIO	RC5, RC6 – For Enabling and Disabling of Parallel Synchronous MOSFETs RC3 – Fan Control RB3 – DACOUT for Debugging RC8 – I/O for Fault LED RC7 – Temperature Fault Input
UART1	Communication with PFC Stage: RC11 – U1TX RC12 – U1RX
UART2	External Communication: RC0 – U2RX RC13 – U2TX
I^2C	External Communication:(1) RB6 – SCL RB7 – SDA RC4 and RB5
Programming/Debugging	PGEC3/PGED3

Note 1: Not implemented in the software.

A high level overview of the software implementation is shown in Figure 26. It can be seen that there are a total of five key ISRs to control the converter. The UART ISRs for PFC communication and external communication are not shown in Figure 26. The descriptions of key ISRs are captured in Figure 26 and their priority levels are given in Table 4. A software execution timing diagram for all the ISRs is shown in Figure 27.

FIGURE 26: HIGH-LEVEL SOFTWARE OVERVIEW

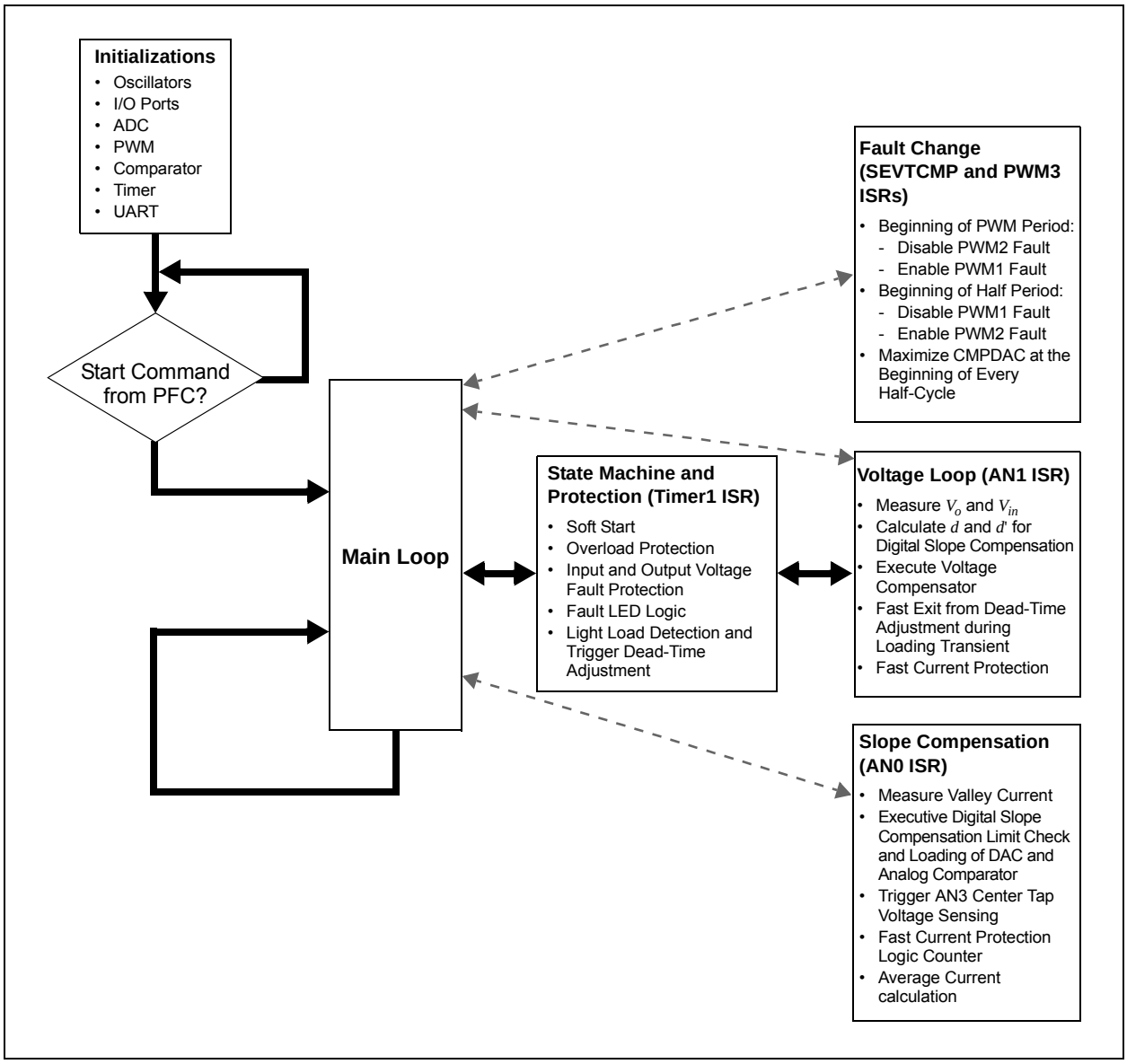


TABLE 4: KEY ISRs AND THEIR PRIORITY LEVELS

ISR Name	Priority Level	Execution Rate	Description
`_ADCAN0Interrupt()`	7	146 kHz	Slope Compensation and CMPDAC Loading
`_PWM3Interrupt()`	6	73 kHz	Enable PWM1 Fault and Disable PWM2 Fault
`_PWMSpEventMatchInterrupt()`	6	73 kHz	Enable PWM2 Fault and Disable PWM1 Fault
`_ADCAN1Interrupt()`	5	73 kHz	Slope Compensation Parameters Calculation, Voltage Compensator and Dead-Time Adjustment Software
`_T1Interrupt()`	4	20 kHz	State Machine and Fault Protection Software

_ADCAN0Interrupt()

The slope compensation loop (ADCAN0 ISR) has to be executed at the beginning of every inductor current cycle. In other words, the ADCAN0 ISR has to be implemented at the beginning of every half-cycle of the PWM signal. This loop implements Equation 21 and updates the comparator DAC for cycle-by-cycle peak current control. The AN0 ISR is triggered after the End-of-Conversion (EOC) of the AN0 channel. The trigger for conversion of the AN0 channel is obtained by ORing the triggers set by both the TRIG1 and STRIG1 registers of the PWM1 Generator. The ORing is accomplished by setting the Dual Trigger Mode bit (DTM) for the PWM1 Generator. The accelerated slope compensation calculations (with Alternate Working registers) take ~300 ns from entry into the ISR until the instant of update of the comparator DAC. The same calculations, without Alternate Working registers, take ~425 ns to execute (30% improvement in speed with Alternate Working registers).

_PWM3Interrupt() and
_PWMSpEventMatchInterrupt()

A single comparator is used for detecting the peak current in both the positive half and the negative half of the transformer current cycle. This means that the same Fault source is used for both positive and negative peak current detection. Therefore, the PWM2 Fault is masked during the positive half-cycle (PWM3 ISR) and the PWM1 Fault is masked during the negative half-cycle (SEVTCMP ISR). The Fault masking ISRs have to precede the slope compensation ISR at every half PWM cycle. The PWM3 ISR is triggered by the value configured in the TRIG3 register and the Special Event Trigger ISR is triggered by the value configured in the SEVTCMP register. Apart from Fault remapping, these interrupts also perform the task of releasing the DAC (DAC set to maximum value) of the peak current comparator at the beginning of every inductor current cycle. This is desirable to avoid peak current detection, due to previous peak current reference, while the peak current value for the present cycle is still being computed. The Fault and DAC management ISRs each take ~280 ns to execute.

_ADCAN1Interrupt()

The calculations for the slope parameters (d and d'), which are dependent on the measured input and output voltages along with the voltage compensator execution, are performed in the AN1 ISR. The output of the voltage compensator is the uncompensated peak current reference. The AN1 ISR is triggered to execute during the negative cycle after both the SEVTCMP ISR and the AN0 ISR complete their execution. This way, all five high-priority ISRs (Priority 5 and higher) are executed without any overlap. The slope parameters and the peak current reference calculated in the AN1 ISR are used for executing the slope compensation algorithm for the next PWM cycle. In other words, the slope parameters and the peak current reference are used for slope compensation in both the positive and negative current cycles in the next PWM cycle. The trigger for conversion of the AN1 channel is set by the TRIG2 register of the PWM2 Generator.

The AN1 ISR also implements:

- Fast Current Protection: Determines whether the sensed current exceeds the absolute maximum value for two inductor current cycles and turns off all the MOSFETs when the current exceeds the maximum value.
- Exit Dead-Time Adjustment: At light loads, the dead time between the complementary MOSFETs in each leg of the full-bridge is increased for higher efficiency (see **"Dead-Time Adjustment"**). However, during sudden loading transients, it is advisable to exit from dead-time adjustment and revert to normal dead time as quickly as possible for maximizing the effective duty cycle. This fast exit from dead-time adjustment software is executed in AN1 ISR.

The hardware accelerated (with Alternate Working registers) AN1 ISR takes 1.7 μs to execute. An implementation without Alternate Working registers takes around 2.2 μs to execute.

_T1Interrupt()

The Timer1 ISR implements the soft start, state machine and Fault management software.

The Fault management software provides protection against overload, input undervoltage, input overvoltage, output undervoltage and output overvoltage. This ISR also implements a LED Fault indication logic. The Fault indication logic toggles an indication LED (connected to the RC8 pin) to a predetermined number of blinks to indicate a particular Fault type (summarized in Table 5). Each LED on time lasts for a duration of 250 ms.

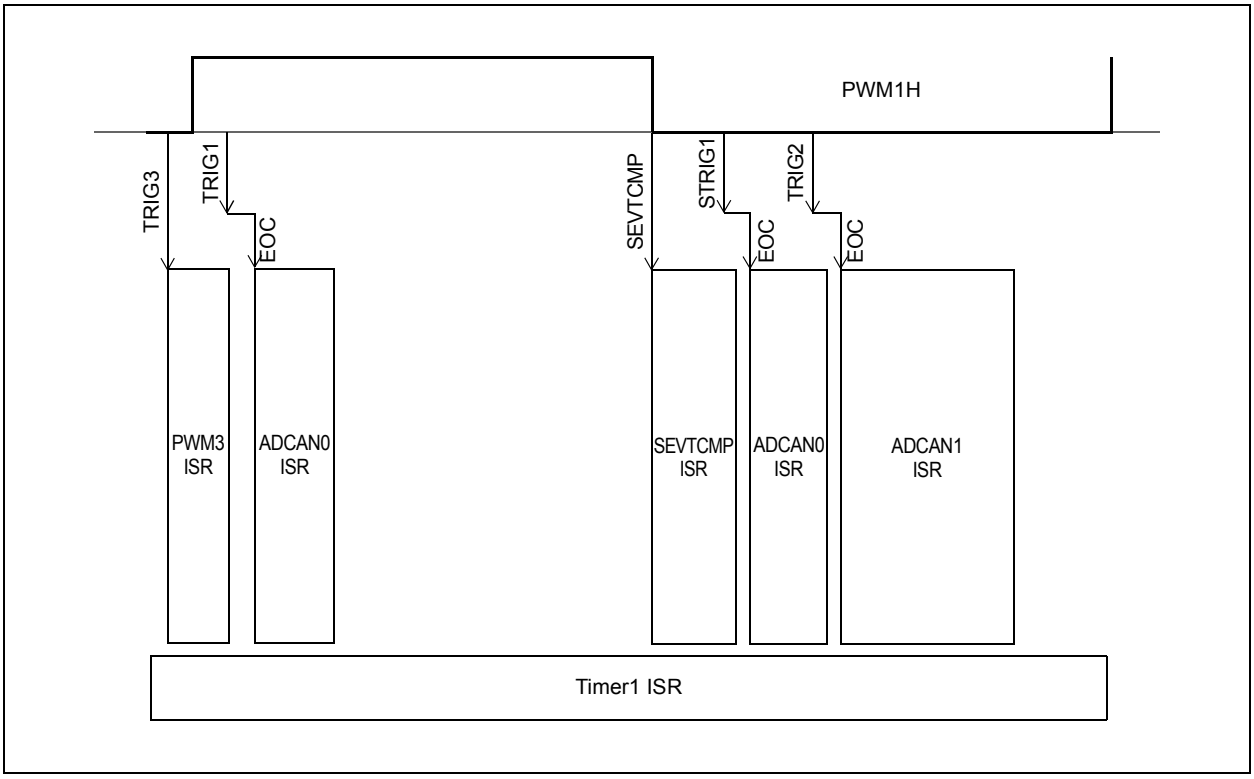
TABLE 5: SYSTEM FAULTS

Fault Indication	No. of LED Blink(s)
Overload Fault	1
Input Overvoltage Fault	2
Input Undervoltage Fault	3
Output Overvoltage Fault	4
Output Undervoltage Fault	5
High-Current Fault	Latched to ON State

The Timer1 ISR also implements the detection of light load and enters a dead-time adjustment for reducing the dead time. The entry to dead-time adjustment is implemented in the Timer1 ISR, since it is not time-critical to enter into this mode at light loads.

The timing diagram, indicating the relative instants of execution of the critical ISRs, is shown in Figure 27. From the figure, it can be deduced that the execution times for the slope compensation loop, Fault management and the voltage compensator loop have to be as minimal as possible. To achieve the best performance, all the critical ISRs are written in assembly language. The Timer1 ISR, being non-critical, is written using C language.

FIGURE 27: SOFTWARE EXECUTION TIMING DIAGRAM FOR CRITICAL ISRs



Efficiency Improvement Techniques

In this section, a few key techniques that can be implemented in software to improve efficiency of the converter are discussed. Dead-time adjustment and Burst mode can be used to improve efficiency at light loads, while the synchronous rectifier overlap technique can improve efficiency at medium and high loads.

DEAD-TIME ADJUSTMENT

In a ZVS FB Converter, at low load currents, the amount of energy stored in the resonant inductance (L_{lk}) is reduced. It is therefore recommended to increase the dead time (resonant interval) between the top switch and the bottom switch of the legs of the full-bridge as the load current decreases. This allows more time for the resonant transition. A typical implementation of dead-time adjustment for the primary side MOSFETs is shown in Figure 28. Although the typical implementation is possible in the software, for the sake of brevity, the actual implementation of dead-time adjustment is done by toggling between two fixed values, as shown in Figure 29. In the software, the dead time between the MOSFETs in a leg (Leg1 → Q1-Q2 and Leg2 → Q3-Q4) are toggled between 520 ns and 1250 ns, depending on the sensed CT current. The nominal value of dead time is 520 ns. When the load current is reduced below 10%, the dead time is toggled to 1250 ns. A hysteresis band of 10% is provided to exit from the Dead-Time Adjustment mode, as seen in Figure 29.

FIGURE 28: DEAD-TIME ADJUSTMENT TYPICAL IMPLEMENTATION

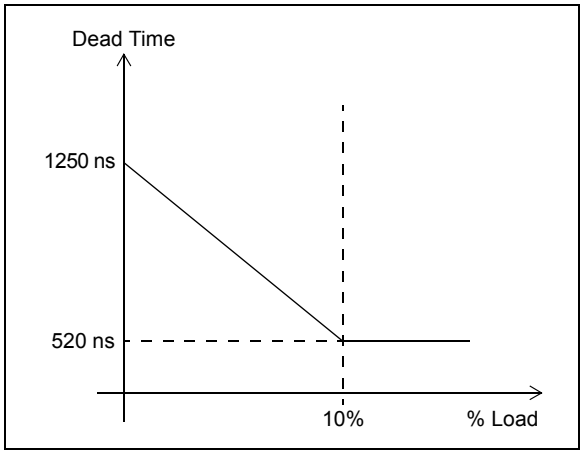
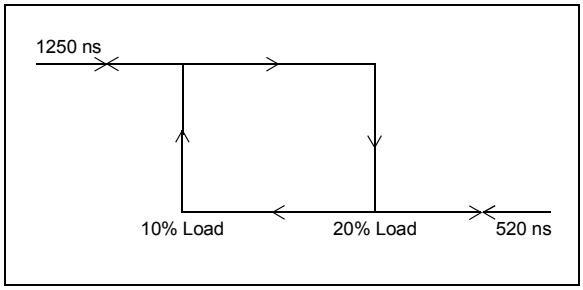
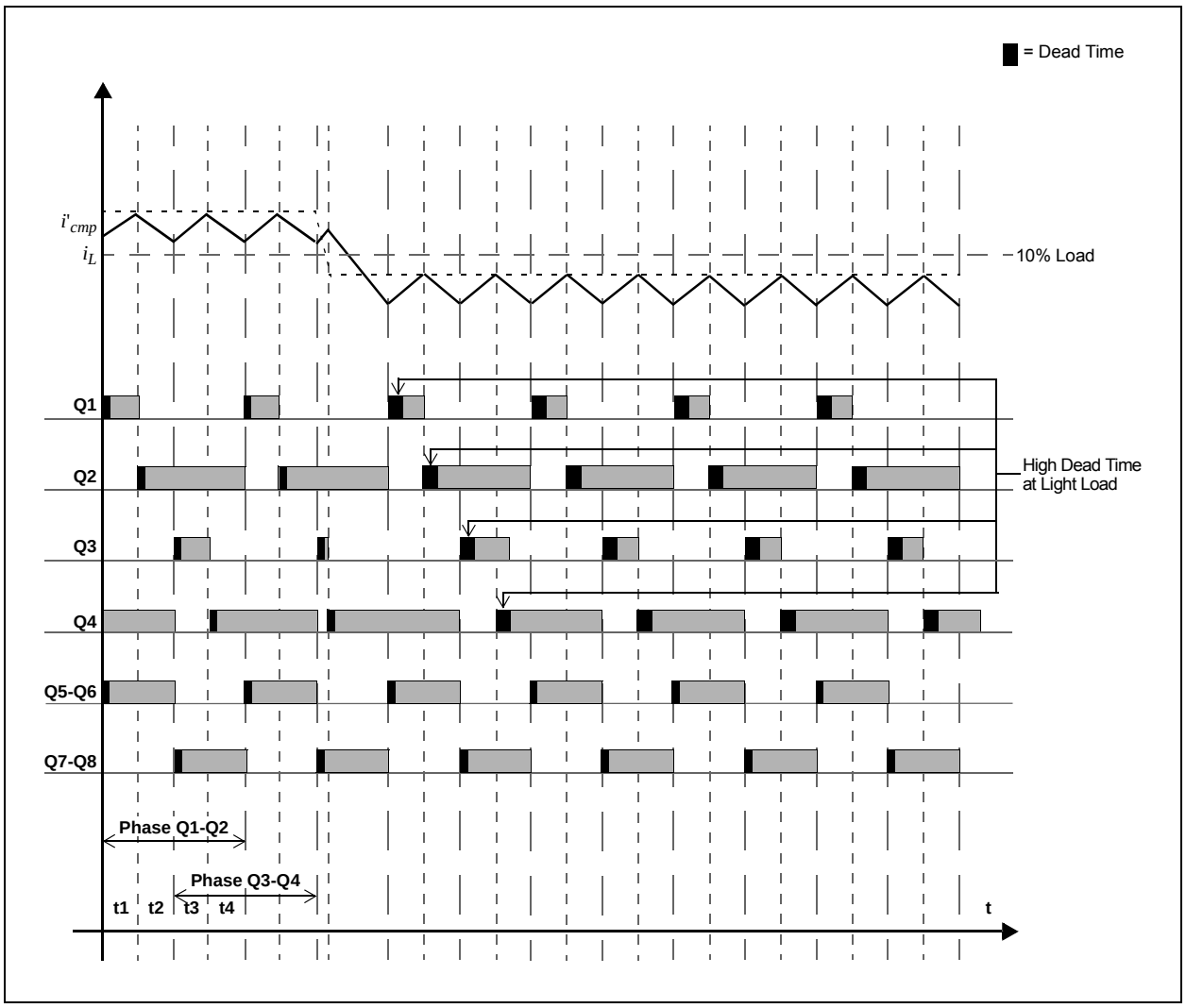


FIGURE 29: DEAD-TIME ADJUSTMENT ACTUAL IMPLEMENTATION



It should be noted that when at a light load condition (dead time is 1250 ns), if the converter experiences a sudden heavy loading transient, the software should support a quick exit from Dead-Time Adjustment mode to allow the maximum duty cycle to be realized. To achieve this, the software to exit from dead-time adjustment has been incorporated into the ADCAN1 ISR, which gets executed once every PWM cycle. The entry to Dead-Time Adjustment mode (from heavy load to light load) being less time-critical, can be executed at a much slower rate and has been implemented in the Timer1 ISR. The switching waveforms for dead-time adjustment implementation are shown in Figure 30. From the figure, it can be observed that as the load current reduces below 10%, the dead-time adjustment software increases the dead time between Q1 and Q2, and also Q3 and Q4 to a larger value.

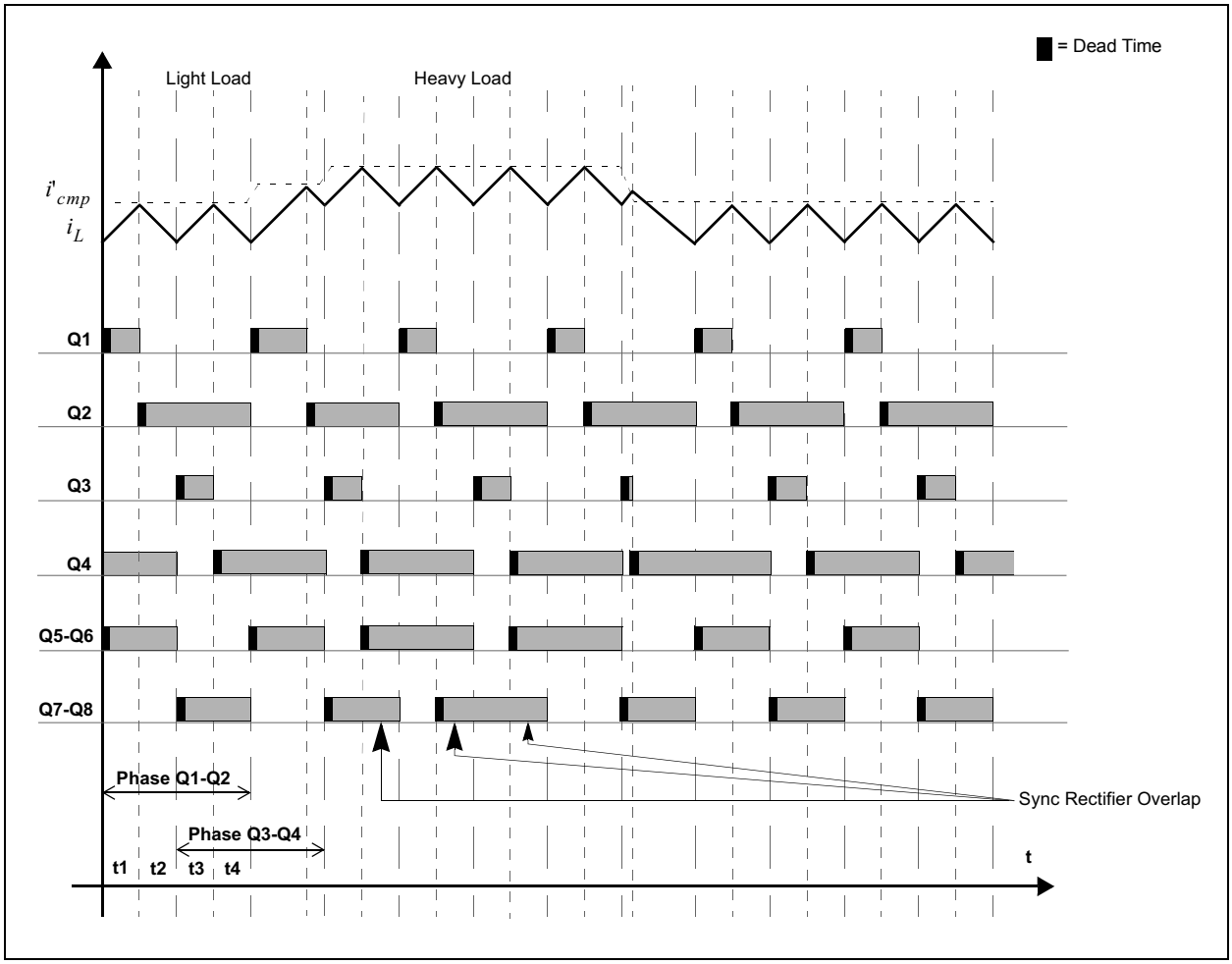
FIGURE 30: DEAD-TIME ADJUSTMENT AT LIGHT LOADS



SYNCHRONOUS RECTIFIER OVERLAP

A commonly applied technique to achieve a higher efficiency at medium and high loads is to overlap the conduction time of the synchronous rectifiers during the freewheeling intervals, t2 and t4 in Figure 4. In this reference design, each leg of the center tapped synchronous rectifier has two paralleled MOSFETs for higher efficiency. Therefore, an overlap of the two legs would result in paralleling of four MOSFETs under medium and high loads. The paralleled MOSFETs would result in a much lower R_{dsON}, thereby improving efficiency significantly. The switching waveforms, during the overlap, are shown in Figure 31. From the figure, it is observed that as the load current increases, i_{cmp} also increases and the synchronous rectifiers overlap during the freewheeling intervals.

FIGURE 31: SYNCHRONOUS FET OVERLAP AT HEAVY LOADS



For achieving synchronous overlap, the following settings are needed for configuring the PWM Generator, which provides the drive signals for the synchronous MOSFETs:

1. Configure PWMx in True Independent mode. In this mode, PWMxH and PWMxL duty cycles are independently controlled by the DTRx and ALTDTRx registers. Also, the PWMxH and PWMxL phases can be independently controlled by the PHASEx and SPHASEx registers.
2. Set SPHASEx to obtain a 180° phase difference from PHASEx.
3. Set the Independent Fault mode bit in the FCLCONx register. This will hand over the Fault control of PWMxH to the CLTSRC<4:0> bits in FCLCONx and PWMxL to the FLTSRC<4:0> bits in FCLCONx. Also, the PWMxH state during a Fault is governed by the value of the FLTDAT1 bit (IOCONx<5>) and the PWMxL state during a Fault is governed by the value of the FLTDAT0 bit (IOCONx<4>)
4. Set the FLTDAT<1:0> bits (IOCON<5:4>) to '0b11'. This setting will cause both PWMxH and PWMxL to go high in the event of a Fault.
5. As seen in Figure 31, the Q5-Q6 MOSFETs must turn on along with the rising edge of Q4 (PWM2L) and the Q7-Q8 MOSFETs must turn on along with the rising edge of Q2 (PWM1L). In other words, the rising edge of Q2 and Q4 have to be configured as Fault sources for Q6 and Q5, respectively.
6. Q2 is driven by PWM1L and Q4 is driven by PWM2L. Since PWM2L is multiplexed with a Remappable Pin (RP), the pin can be configured as an input pin and mapped as a Fault source for PWMxH. However, in the dsPIC33EP64GS504 device, since PWM1L is not multiplexed by a remappable pin, there are two options for choosing this PWM as the Fault source for PWMxL:
   a) Configure PWM4 to be the same as the PWM1 configurations (including Faults). PWM4 pins can be remapped to any of the remappable pins of the device. Therefore, PWM4L can be assigned to any (unused) remappable pin (configured as an output port), and this remappable pin can be externally connected to another remappable pin (configured as an input port), which can be configured as a Fault source for PWMxL.
   b) Choose the PWM4 Generator for Q1-Q2 and choose pins that are multiplexed with remappable pins for PWM4H and PWM4L.

BURST MODE

During very light load scenarios, the converter enters Discontinuous Conduction mode. During this mode, the synchronous MOSFETs can be completely turned off, leaving only the body diode of the MOSFETs for conduction (Diode Emulation mode). This results in minimization of circulating currents in the secondary side of the transformer and improves efficiency. At very light loads, the switching losses of the MOSFETs become comparable to power demanded by the load. Under such conditions, it is recommended to completely turn off the MOSFETs of the full-bridge (and synchronous rectifiers) for several cycles, during which, the output capacitor bank supports the load. After a few PWM cycles, the MOSFETs can be turned on again to charge the output capacitor bank. This technique is also called Burst mode, since the input power is applied only in short bursts and the converter is essentially turned off for most of the time. In this technique, it should be ensured that the transformer flux balance is maintained by allowing an even number of inductor current cycles to elapse before restarting the MOSFETs.

Both Diode mode and Burst mode techniques are easy to implement if the controller has an accurate feedback of the load current. This is possible by connecting a shunt to the load current. Voltage across the shunt can be filtered and amplified, and fed back to the dsPIC DSC.

In this reference design, the following techniques are implemented to improve efficiency during light loads:

1. Dead-time adjustment, as shown in Figure 29 and Figure 30, in the **"Dead-Time Adjustment"** section.
2. Paralleling of two synchronous MOSFETs at each leg for efficiency improvement at high loads.
3. Turn off of one MOSFET in each pair of synchronous MOSFETs for < 10% load.

APPENDIX A: DESIGN PACKAGE

A complete design package for this reference design is available as a zipped folder. This design package can be downloaded from the Microchip corporate web site at: www.microchip.com.

A.1 Design Package Contents

The design package contains the following items:

- Reference Design Schematics
- Bill of Materials
- Hardware Design Gerber Files
- Source Code
- Hardware Design Layout Files
- Demonstration Instructions
- MATLAB® Models

APPENDIX B: ELECTRICAL SPECIFICATIONS AND OPERATIONAL WAVEFORMS

This section provides information on the electrical specifications for the 750W DC/DC Converter and also showcases a few key waveforms captured from the hardware.

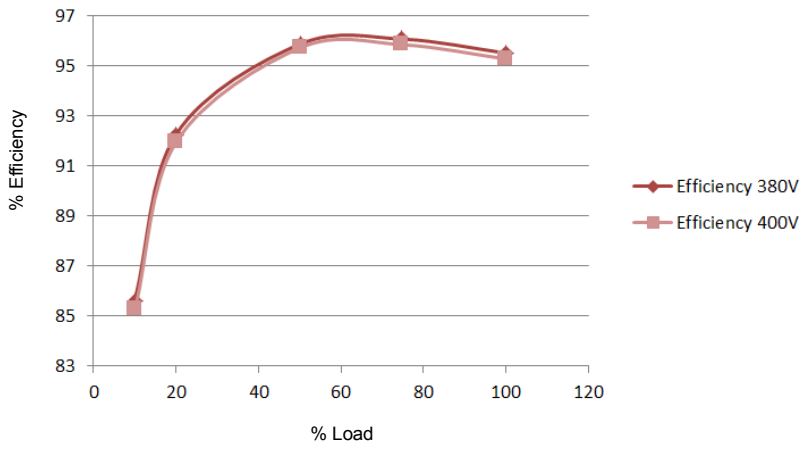
B.1 Electrical Specifications

Table B-1 shows the key electrical specifications for the DC/DC Converter.

TABLE B-1: DC/DC CONVERTER ELECTRICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Unit	Comments
V_{IN}	DC Input Voltage	380	400	410	V	
V_o	DC Output Voltage	11.88	12	12.12	V	±1%
P_o	Output Power	—	750	—	W	
I_o	Output Current	—	62.5	71	A	
η	Converter Efficiency	—	95.4	96	%	Peak Efficiency
Fsw	Switching Frequency	—	72.84	—	kHz	

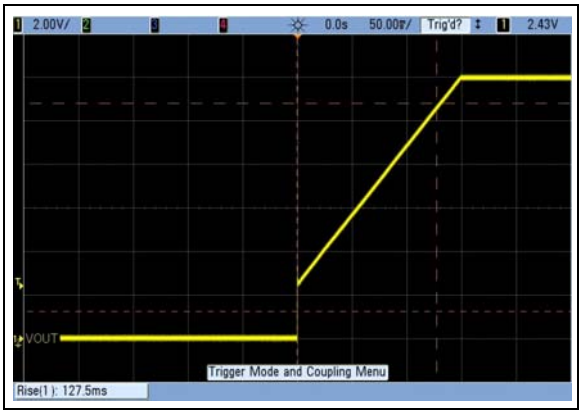
FIGURE B-1: 750W DC/DC CONVERTER EFFICIENCY vs. % LOAD CHART



B.2 Operational Waveforms

Figure B-2 shows the output voltage waveform during start-up with an applied input voltage of 400V and a load of 750W connected at the output. From the waveform, it can be seen that the soft start routine ensures a smooth ramp-up of the voltage reference and the output voltage follows the voltage reference.

FIGURE B-2: START-UP WAVEFORM



From Figure B-2, it can be seen that there is no undershoot or overshoot in the output voltage during and after the completion of a soft start. At start-up (Figure B-2), it can be observed that the output voltage rises to a minimum value before ramping up during the soft start. That is because the converter is essentially run in an open loop with a fixed peak current reference. During this time, the input voltage is applied across the transformer primary winding, instantaneously charging the output capacitors. As a result, the output voltage increases even before the soft start routine with closed-loop control is enabled.

Figure B-3 shows the (sensed) current waveform without the application of digital slope compensation. Here, the output of the voltage compensator is directly scaled and provided to the 12-bit DAC of the analog comparator. From the figure, the subharmonic oscillations can be clearly observed, resulting in a non-uniform steady-state current waveform.

FIGURE B-3: SENSED CURRENT (INDUCTOR CURRENT DURING t1 AND t3) WITHOUT SLOPE COMPENSATION

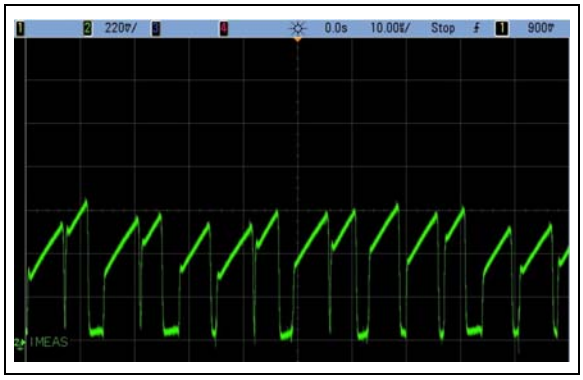


Figure B-4 shows the sensed current waveform with the application of a digital slope compensation algorithm to the voltage compensator output. From the waveform in Figure B-4, it should be noted that the effective duty cycle is ~80%. It can be concluded that the digital slope compensation algorithm is effective in eliminating the subharmonic oscillations due to duty cycles > 50%, resulting in a smooth steady-state current.

FIGURE B-4: SENSED CURRENT (INDUCTOR CURRENT AT t1 AND t3) WITH DIGITAL SLOPE COMPENSATION

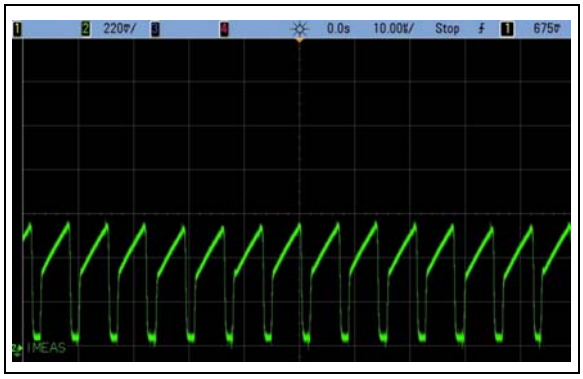


Figure B-5 shows the transient response of the converter output voltage for a dynamic load setting of 15%-75%-15% with a slew rate of 1A/µs at a rate of 100 Hz. The sensed current and the load current are also shown.

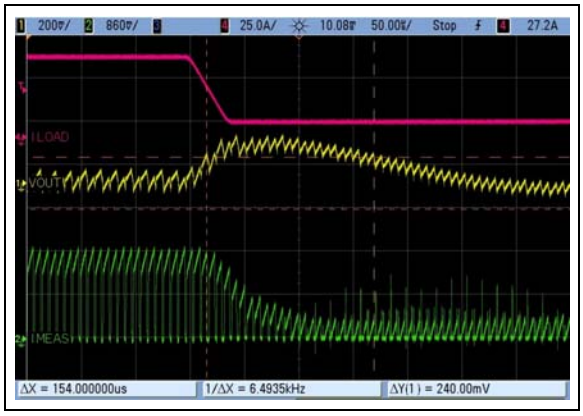
FIGURE B-5: TRANSIENT RESPONSE (15%-75%-15%, 1A/µS, 100 Hz)

Figure B-6 shows a magnified version of the loading transient of 15%-75% load. The figure also shows the settling time and the peak undershoot during the loading transient.

FIGURE B-6: LOADING TRANSIENT (15%-75%) DEPICTING SETTLING TIME WITHIN 1% BAND

Figure B-7 shows a magnified version of the load throw-off transient of 75%-15% load. The figure also shows the settling time and the peak undershoot during the load throw-off transient.

FIGURE B-7: LOAD THROW-OFF TRANSIENT (75%-15%) DEPICTING SETTLING TIME WITHIN 1% BAND



From Figure B-6 and Figure B-7, it can be observed that the subharmonic oscillations are eliminated from the current waveform, even during load transients.

Figure B-8 shows a transient response for 10%-75%-10% loading with 1A/µs slew rate at a 100 Hz rate.

FIGURE B-8: TRANSIENT RESPONSE (10%-75%-10%, 1A/µS, 100 Hz)

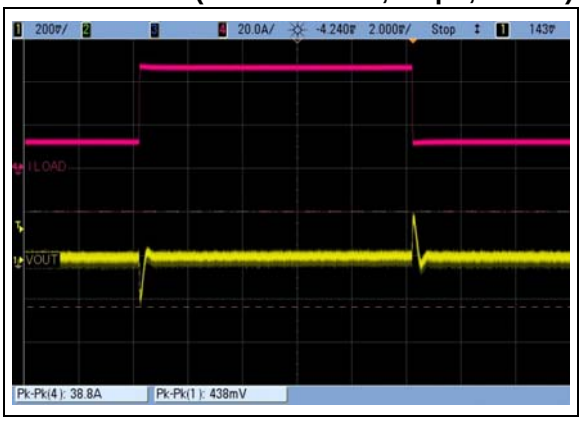


Figure B-9 shows the drain to source voltage (VDS) and the gate to source (VGS) voltage of a Q1 MOSFET at a 50% load. This figure also depicts the ZVS turn-on at the beginning of the t1 interval, as shown in Figure 4.

FIGURE B-9: ZVS TURN-ON OF Q1 MOSFET AT 50% LOAD

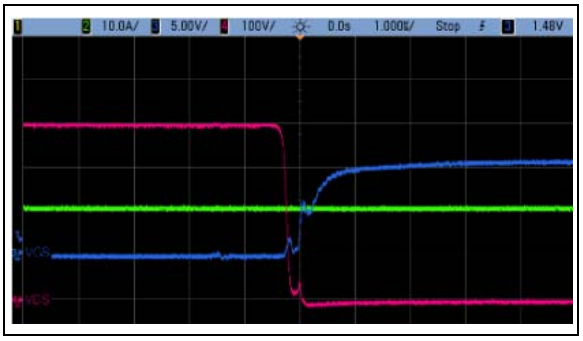
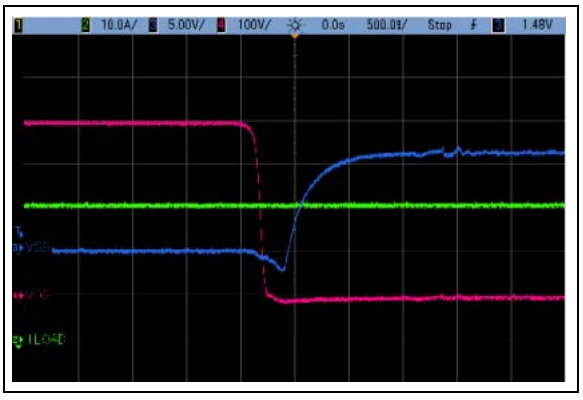


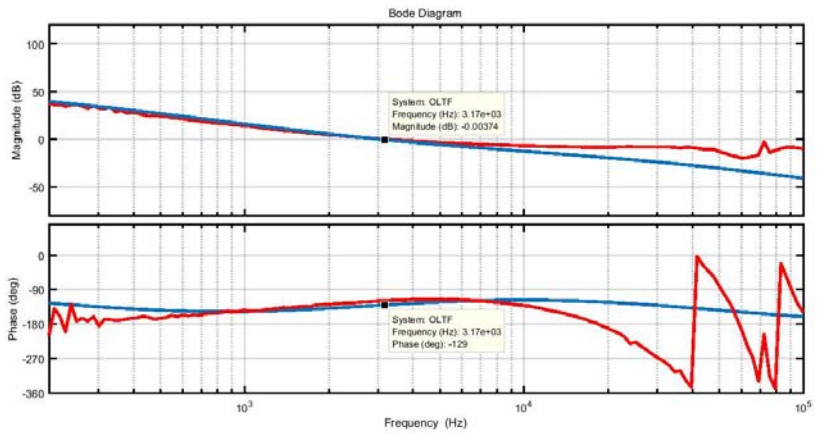
Figure B-10 shows the drain to source voltage (VDS) and the gate to source (VGS) voltage of a Q2 MOSFET at a 50% load. This figure also depicts the ZVS turn-on at the beginning of the t2 interval, as shown in Figure 4.

FIGURE B-10: ZVS TURN-ON OF Q2 MOSFET AT 50% LOAD



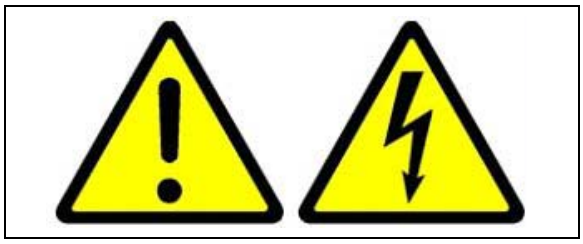
A comparison of the frequency response plot predicted by the mathematical model (Equation 66) and the results captured in the hardware using a frequency response analyzer are shown in Figure B-11. As shown in the figure, the hardware response closely matches the model prediction.

FIGURE B-11: FREQUENCY RESPONSE – $G_{OLTF}(s)$



Red: Hardware
Blue: Model Prediction

APPENDIX C: SAFETY NOTICES



The following safety notices and operating instructions should be observed to avoid a safety hazard. If in any doubt, consult your supplier.

WARNING – This reference design must be earthed (grounded) at all times.

WARNING – This reference design should not be installed, operated, serviced or modified except by qualified personnel who understand the danger of electric shock hazards, and have read and understood the user instructions. Any service or modification performed by the user is done at the user's own risk and voids all warranties.

WARNING – It is possible for the output terminals to be connected to the incoming AC mains supply and may be up to 410V with respect to ground, regardless of the input mains supply voltage applied. These terminals are live during operation and for some time after disconnection from the supply. Do not attempt to access the terminals or remove the cover during this time.

C.1 General Notices

- This reference design is intended for evaluation and development purposes, and should only be operated in a normal laboratory environment as defined by IEC 61010-1:2001
- Clean with a dry cloth only
- Operate flat on a bench and do not move the reference design during operation
- This reference design should not be operated without all of the supplied covers fully secured in place
- This reference design should not be connected or operated if there is any apparent damage to the unit

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4. F.J. Azcondo, Ch. Branas, R. Casanueva, and Dragan Maksimovic, *"Approaches to Modeling Converters with Current Programmed Control"*, *"IEEE Transactions on Power Electronics Education"*, June 2005, pp. 98-104

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