Richtek DDR5 PMIC 解決方案

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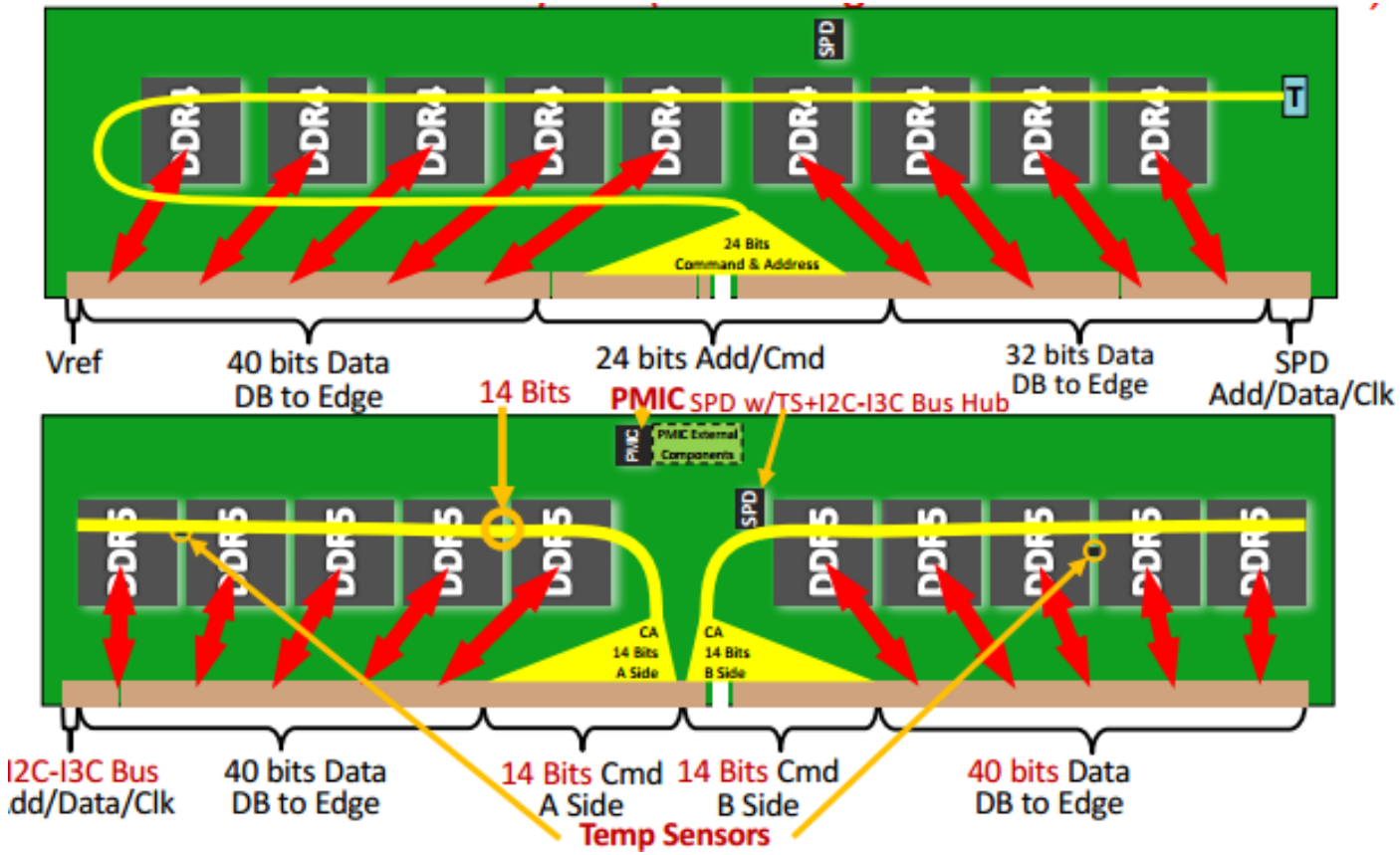
your power partner.

DDR5電源方案 – PMIC在DIMM上

- Sever : JEDEC PMIC5000 & PMIC5010 規範, 用於 RDIMM & LRDIMM
- Client : JEDEC PMIC5100 規範, 用於 UDIMM & SO-DIMM



DDR4 DIMM :
- DDR4 SDRAMs
- SPD

DDR5 DIMM :
- DDR5 SDRAMs
- SPD
- PMIC
- Temp. Sensor (optional)

Diagram Source : JEDEC

為什麼要把PMIC電源方案移到DDR5 DIMM上

- **受限於DIMM板形及可使用線數不足**
  - DDR5 需要提供更多線數給資料匯流排
  - 連接埠上的線距無法再減小
- **要求輸出電壓準確度提高**
  - 針對更高速的操作穩定性, 要求小於±3% 的電壓誤差
  - 原始DDR4架構, 會有電壓降在主機板及連接埠上
- **降低成本**
  - 主機板上的電源設計預算不再以DIMM插槽數來考量而導致過度設計
  - 可透過微調DIMM上供應給DRAM的電壓來提高DRAM的批次良率
- **加值考量**
  - 電源異常發生可儲存原因於暫存器, 當重新啟動時可讀取暫存器資料還偵錯
  - 可以跟主控溝通, 並報告相關電壓, 電流, 溫度...的資訊

更多的資料傳輸線數

更好的電壓準確度

更低的材料成本

更易偵錯及資訊取得

DDR5 UDIMM & SO-DIMM的電源腳位

DDR5 Client DIMM應用 : UDIMM用於桌機電腦, SO-DIMM用於筆記本電腦

DDR4-288pins → DDR5-288pins

UDIMM

(133.35mm x 31.25mm)

Pin #1 : VIN_BULK(+5Vin)
Pin #145 : VIN_BULK(+5Vin)
Pin #146 : VIN_BULK(+5Vin)
Pin #147 : PWR_GOOD
Pin #151 : PWR_EN
KEY : Pin75/219~Pin76/220

DDR4-260pins → DDR5-262pins

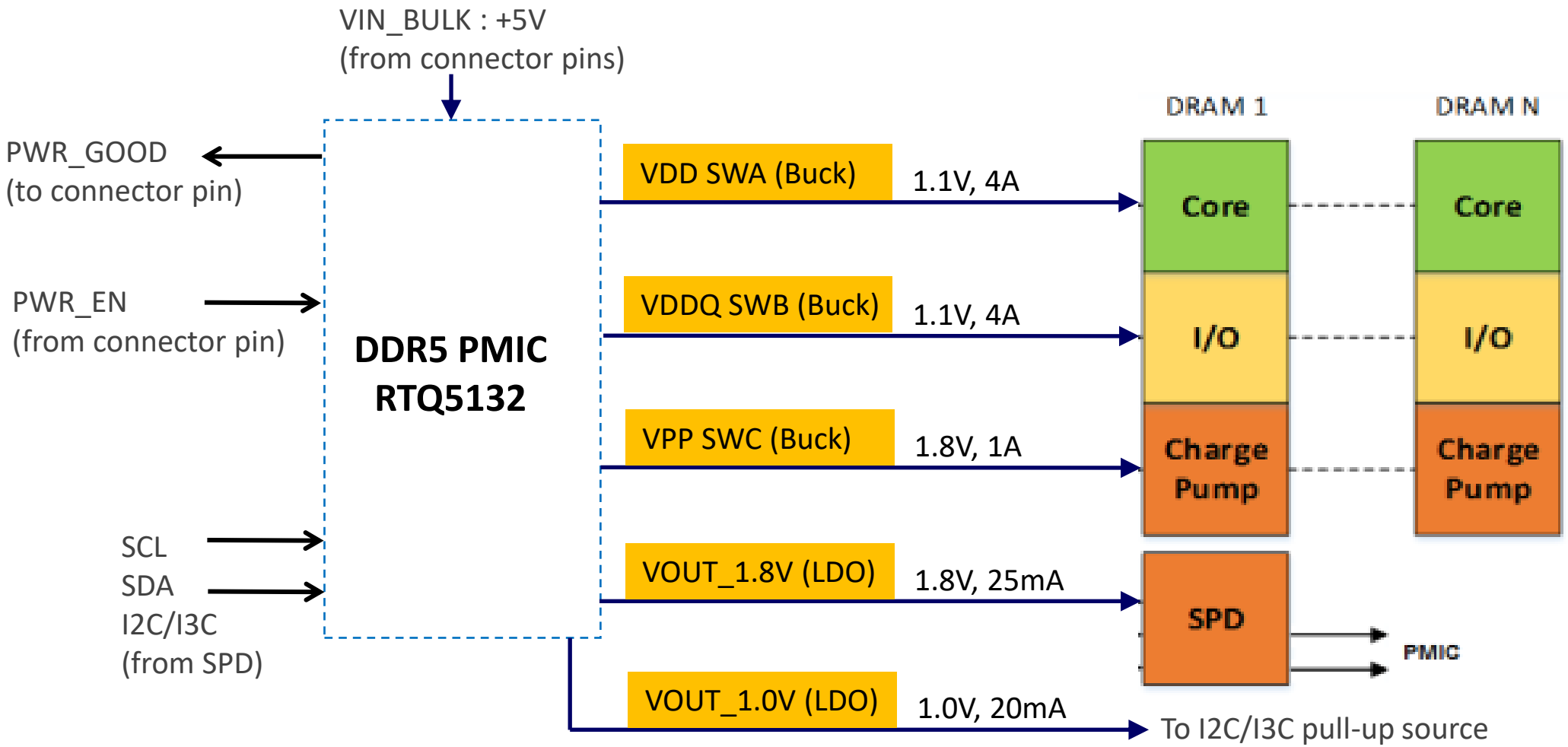
SO-DIMM

(69.6mm x 30mm)

Pin #1 : VIN_BULK(+5Vin)
Pin #3 : VIN_BULK(+5Vin)
Pin #7 : PWR_GOOD
Pin #8 : PWR_EN
KEY : Pin125/126~Pin127/128

DDR5 UDIMM & SO-DIMM上的電源架構

DDR5 UDIMM & SO-DIMM 電源配置



DDR5 UDIMM & SO-DIMM PMIC規格 – Richtek RTQ5132

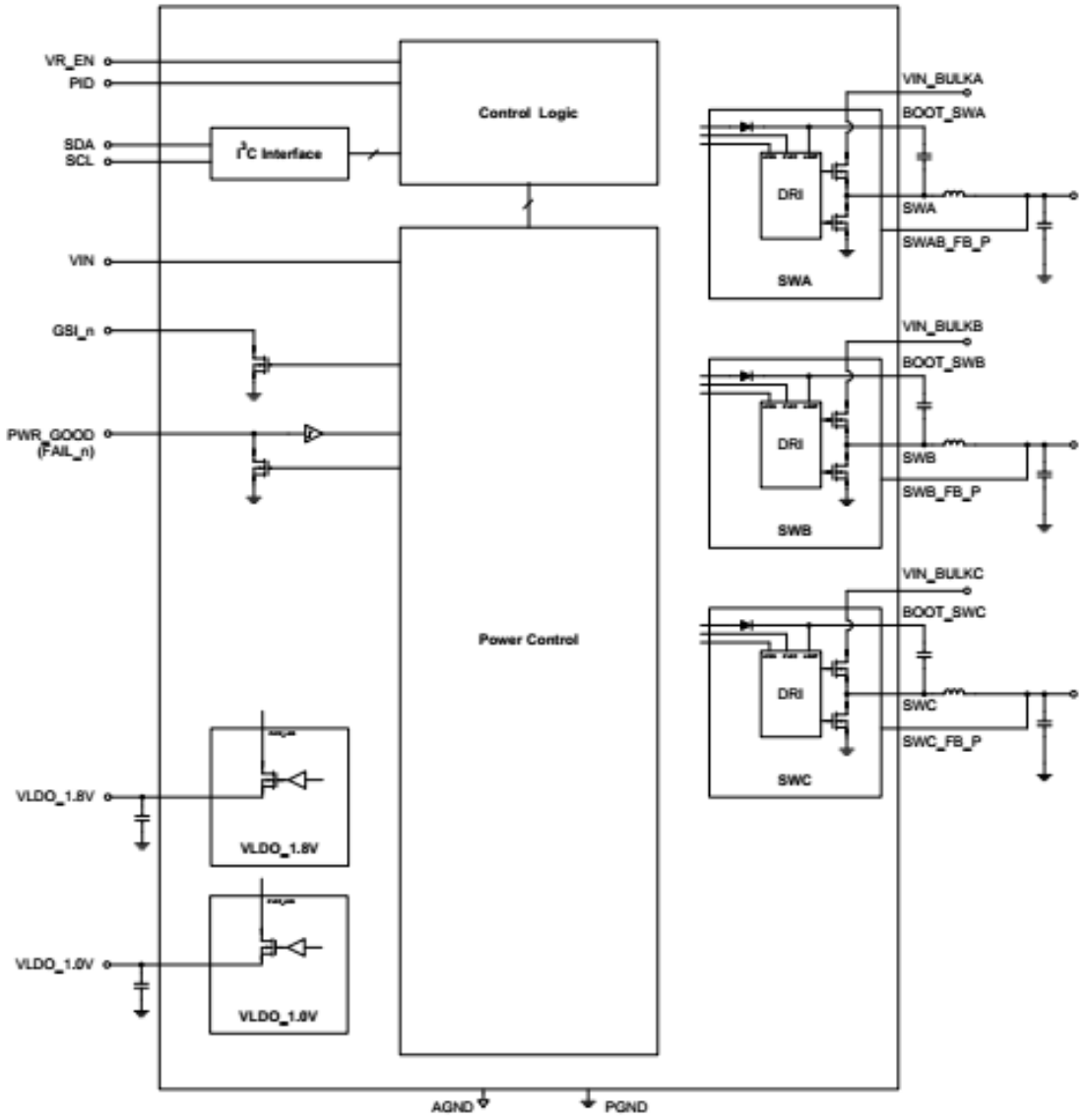
Specification

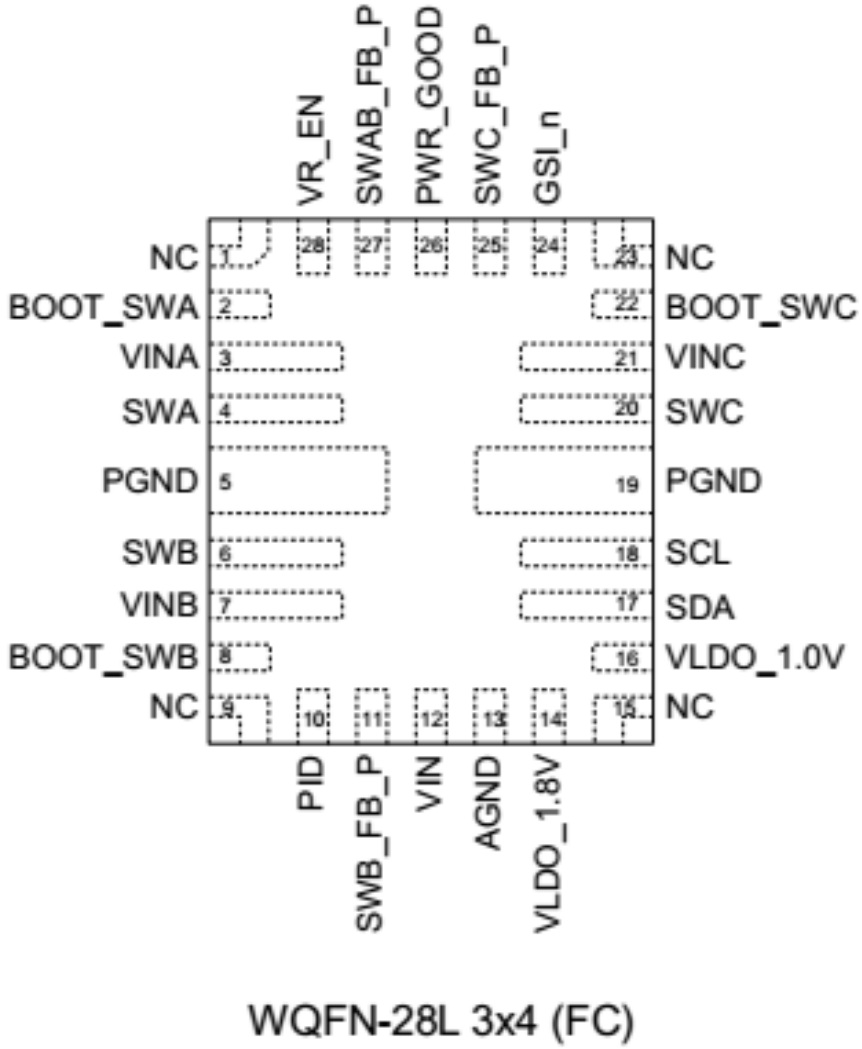
- Input Voltage Range 4.25V to 5.5V
- Three High Efficiency Step-down Converters
  - Buck1(SWA): 0.8V to 1.435V, 4Amax & 5Apeak
  - Buck2(SWB): 0.8V to 1.435V, 4Amax & 5Apeak
  - Buck3(SWC): 1.5V to 2.135V, 1Amax & 2Apeak
- Two LDOs
  - 1.8V/25mA
  - 1.0V/20mA
- Compatible I2C & JEDEC module sideband bus
- JEDEC PMIC5100 Specification Compliance

Feature

- A2COT Technology for Fast Transient Response
- Configurable Dual-Phase for Buck1 and Buck2
- MTP build-in, Programmable for Power Up Sequence, Soft-Start & Soft-Stop Slew Rate
- Flexible Mechanism to Enable Regulators by VR_EN pin or VR enable command
- VIN power OVP
- OTP, OVP, UVP, OCP on Each Rails
- General Status Interrupt Function
- Power Good Indicator

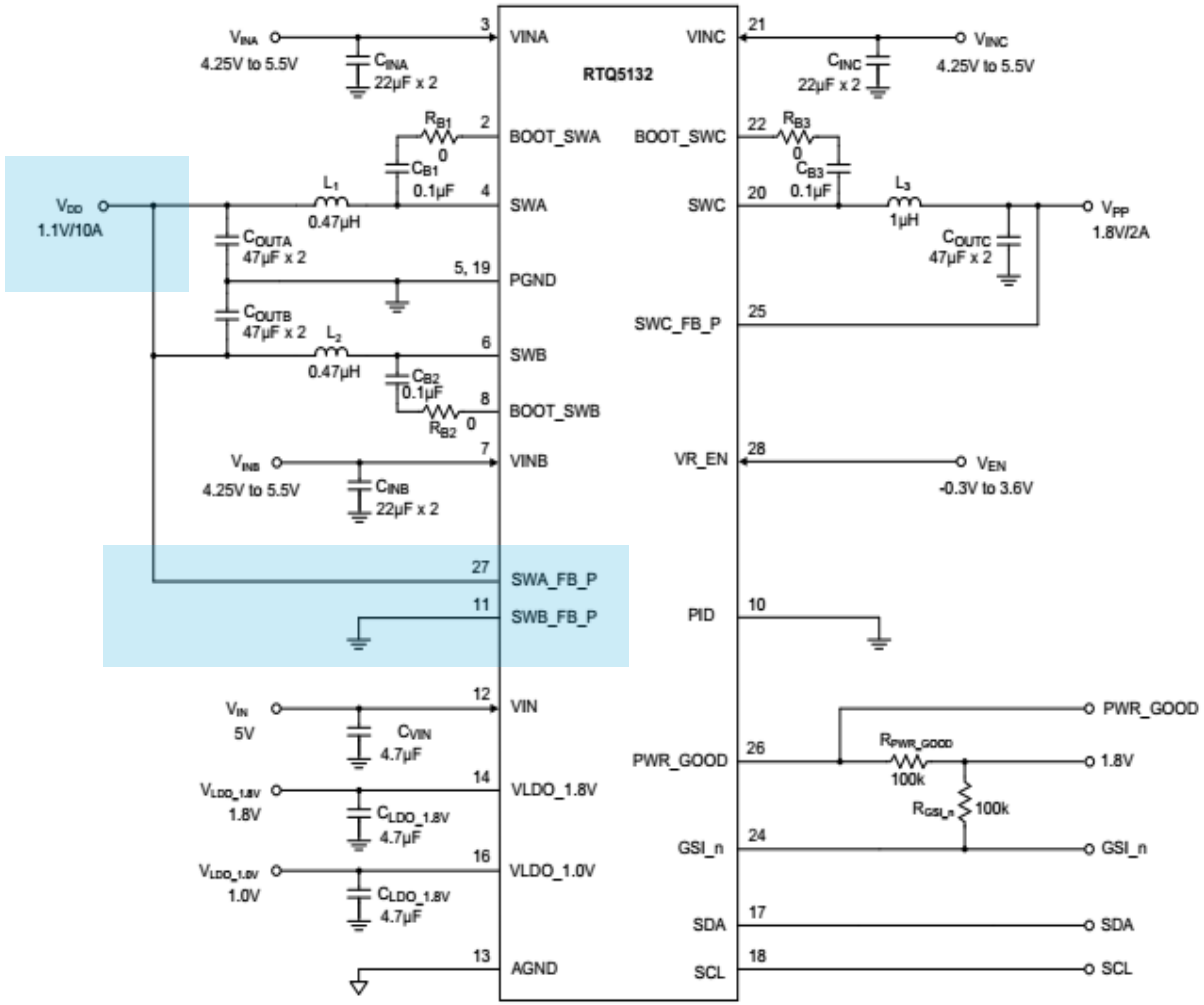
方塊圖及腳位



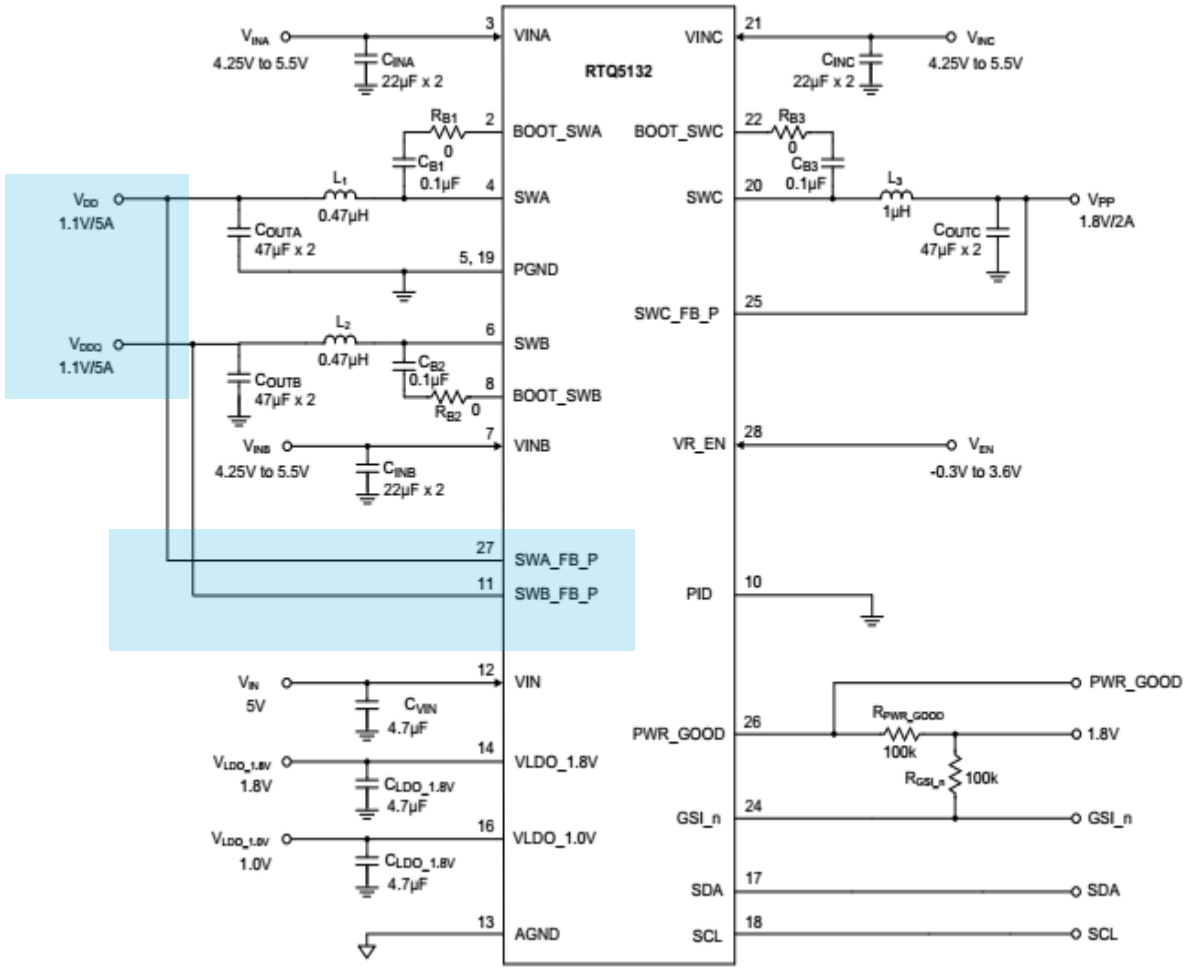


WQFN-28L 3x4 (FC)

參考線路圖



SWA and SWB are operating in dual-phase mode

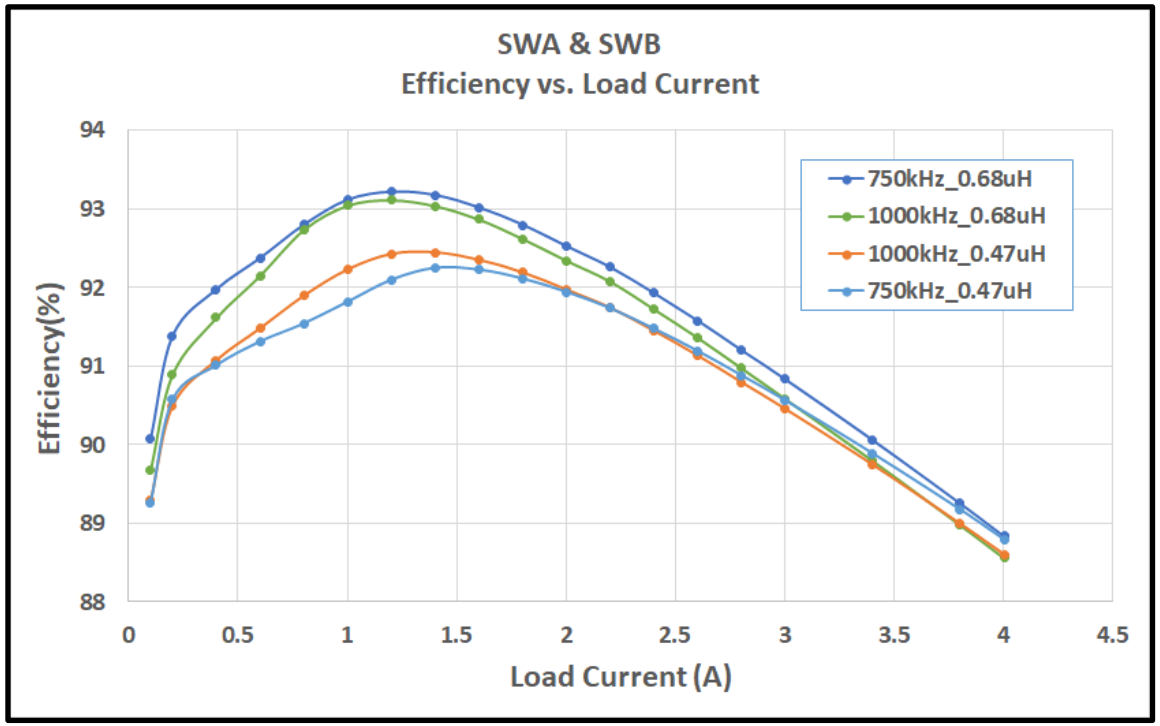


SWA and SWB are operating in single-phase mode

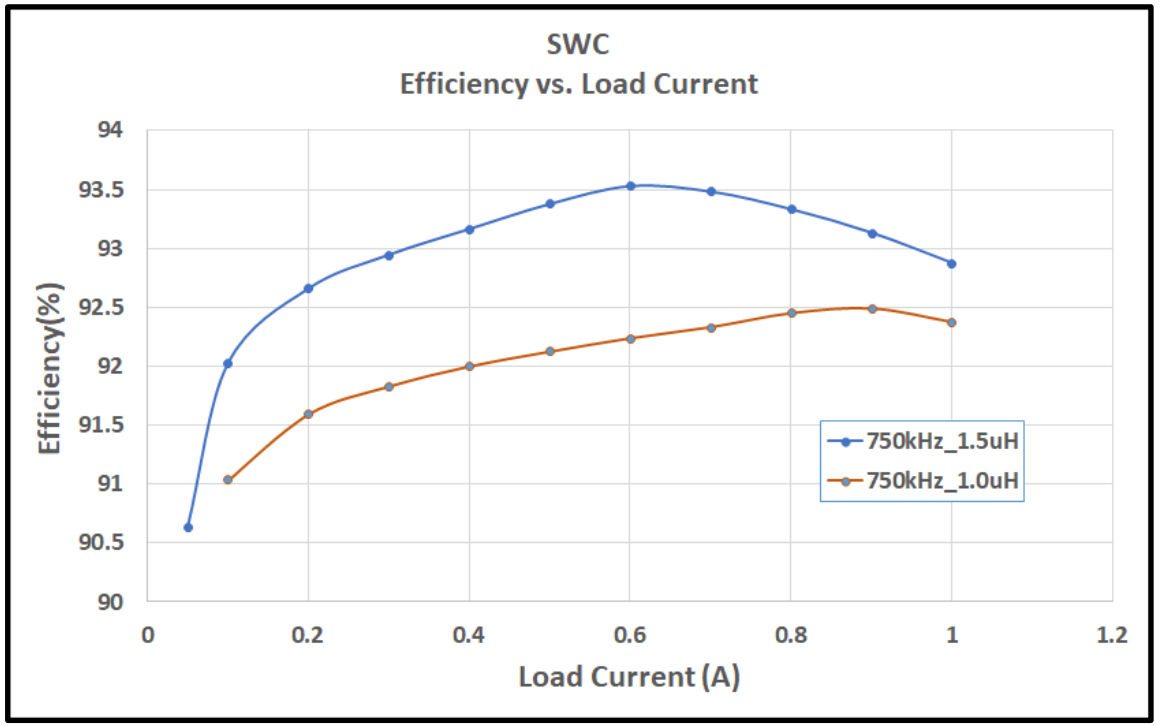
效率規格及量測結果

- 根據 JEDEC JESD301-2 PMIC5100 Specification Rev1.00

SWA & SWB 選0.68uH & 操作頻率750KHz效率結果最好



SWC選1.5uH & 操作頻率750KHz效率結果最好



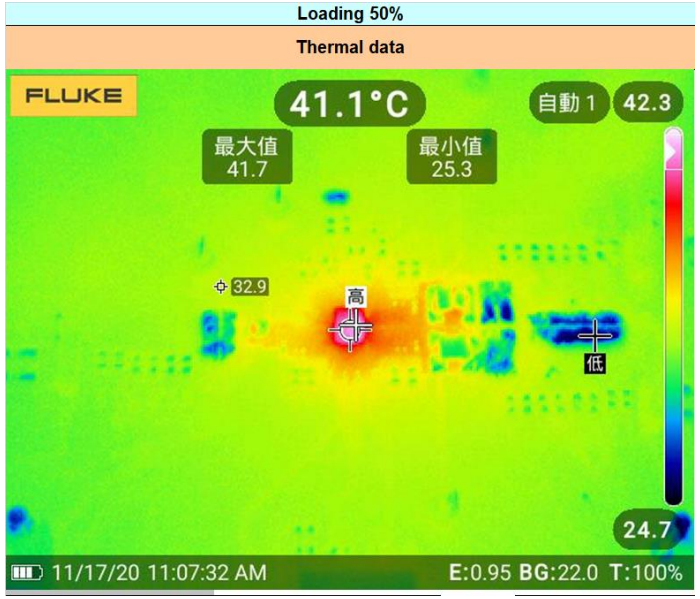
ILOAD	50mA (Light Load)	1A (25% Imax)	2A (50% Imax)	3A (75% Imax)	4A (100% Imax)
JEDEC Specification	83.0%	90.0%	88.0%	85.0%	82.0%
RTQ5132, 750KHz	85.4%	93.1%	92.5%	90.8%	88.8%
Diff.	+2.4%	+3.1%	+4.5%	+5.8%	+6.8%

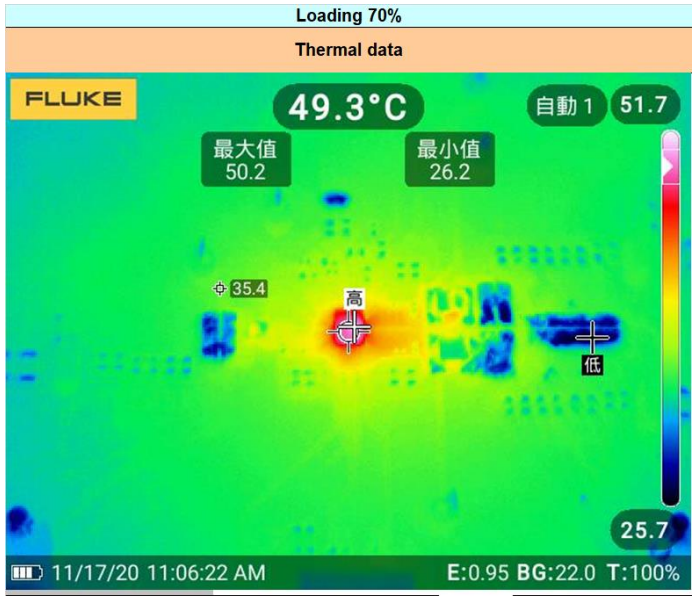
ILOAD	50mA (Light Load)	0.25A (25% Imax)	0.5A (50% Imax)	0.75A (75% Imax)	1A (100% Imax)
JEDEC Specification	85.0%	90.0%	89.0%	87.0%	85.0%
RTQ5132, 750KHz	90.6%	92.8%	93.4%	93.4%	92.8%
Diff.	+5.6%	+2.8%	+4.4%	+6.4%	+7.8%

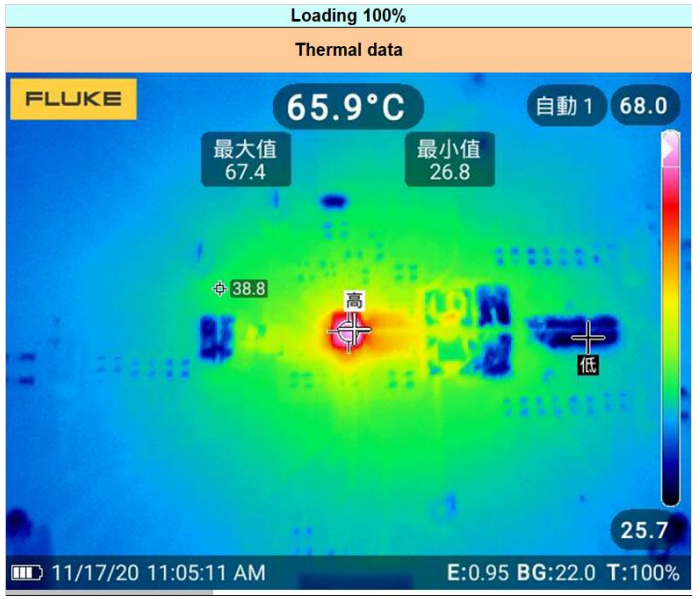
溫度及溫升量測結果

全載下溫升約42度

Load%	Load Current(A)			Thermal_max(℃)	Delta_T(℃)
	SWA	SWB	SWC	@Ta=25℃	
50%	2.5	2.5	1.0	41.7	16.7
70%	3.5	3.5	1.4	50.2	25.2
100%	5.0	5.0	2.0	67.4	42.4







電感器的規格及選擇

- 根據 JEDEC JESD301-2 PMIC5100 Specification Rev1.00

  - **Inductor Mechanical Specification:**

SWA & SWB

Package Size	
L (mm)	3.4 Max
W (mm)	3.2 Max
H (mm)	1.2 Max

SWC

Package Size	
L (mm)	2.7 Max
W (mm)	2.2 Max
H (mm)	1.2 Max

  - **Inductor Electrical Specification:**

SWA & SWB

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias (μH)	Max DCR (mΩ)	Max ACR @ 1 MHz[2,3] (mΩ)
1.2 Max	0.47 ± 20%	14.5	93
	0.68 ± 20%	18.5	113

建議選擇 0.68uH效率結果最好

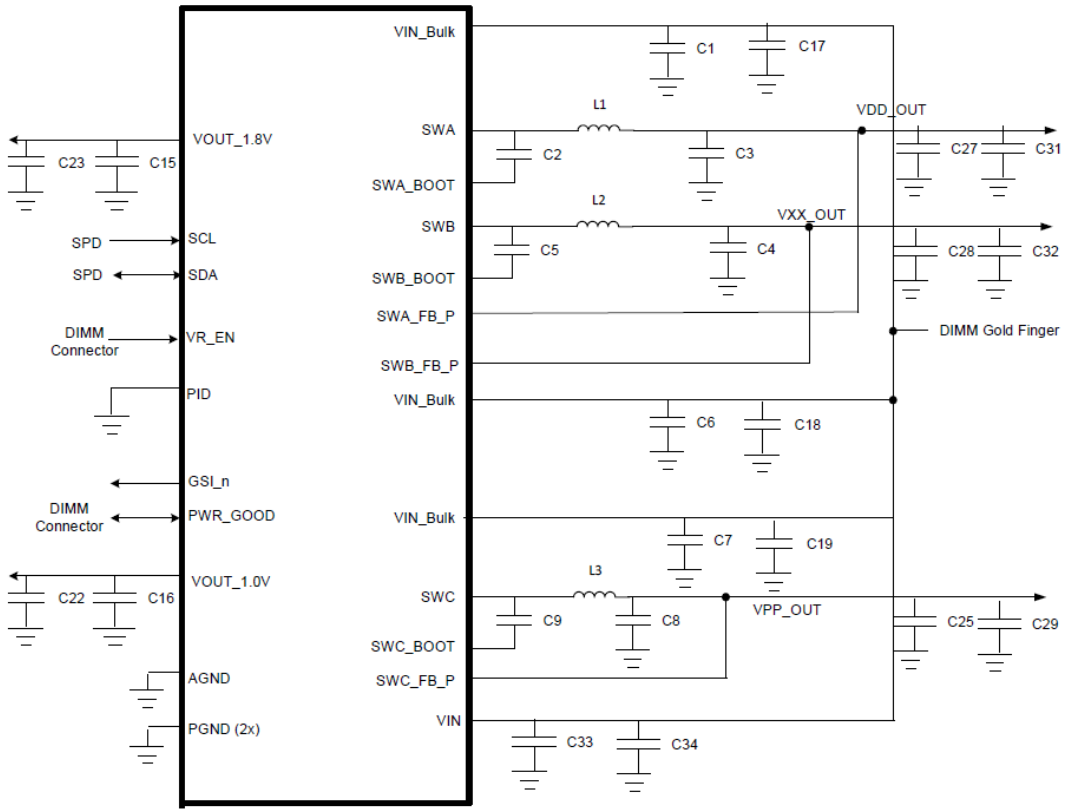
SWC

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias (μH)	Max DCR (mΩ)	Max ACR @ 1 MHz[2,3] (mΩ)
1.2 Max	1.0 ± 20%	48.0	182
	1.5 ± 20%	75.0	300

建議選擇 1.5uH效率結果最好

線路BOM的規格及建議

- 根據 JEDEC JESD301-2 PMIC5100 Specification Rev1.00
  - SWA/SWB : JEDEC Cout=47uFx2(Local), 175uFx2(Remote)
    建議Remote端至少等值47uFx4 (for Intel AVL 0.1A->5A)
  - SWC : JEDEC Cout=47uFx2(Local), 75uFx2(Remote)
    建議Remote端至少等值47uFx4 (for Intel AVL 0.1A->5A)



輸出穩態DC及暫態DC+AC規格及量測結果

- 根據 JEDEC JESD301-2 PMIC5100 Specification Rev1.00
  - SWA/SWB/SWC : DC +/-0.75%, DC+AC +/-2.5%

	JEDEC Spec				RTQ5132 Results			
	VOUT (max)	VOUT (typ)	VOUT (min)	Delta (mV)	VOUT (max)	VOUT (typ)	VOUT (min)	Delta (mV)
SWA	1.1275	1.100	1.0725	55	1.1226	1.100	1.0728	48.9
SWB	1.1275	1.100	1.0725	55	1.1196	1.100	1.0756	44.9
SWC	1.845	1.800	1.755	90	1.8159	1.800	1.7804	35.1

測試條件 :
- SWA/SWB: 400mA -> 4A Step
- SWC: 100mA -> 1A Step

可設計於超頻使用的DDR5 PMIC – Richtek RTQ5136

Specification

- Input Voltage Range 4.25V to 5.5V
- Three High Efficiency Step-down Converters
  - Buck1(SWA):
    - 0.8V to 1.435V, 4Amax & 5Apeak(RTQ5132)
    - 0.8V to 2.5V, 6.5Amax & 7.6Apeak(RTQ5136)
  - Buck2(SWB):
    - 0.8V to 1.435V, 4Amax & 5Apeak(RTQ5132)
    - 0.8V to 2.5V, 6.5Amax & 7.6Apeak(RTQ5136)
  - Buck3(SWC):
    - 1.5V to 2.135V, 1Amax & 2Apeak(RTQ5132)
    - 1.5V to 2.8V, 1.5Amax & 2.5Apeak(RTQ5136)
- Two LDOs
  - 1.8V/25mA
  - 1.0V/20mA
- Compatible I2C & JEDEC module sideband bus

Feature

- A2COT Technology for Fast Transient Response
- Configurable Dual-Phase for Buck1 and Buck2
- MTP build-in, Programmable for Power Up Sequence, Soft-Start & Soft-Stop Slew Rate
- Flexible Mechanism to Enable Regulators by VR_EN pin or VR enable command
- VIN power OVP
- OTP, OVP, UVP, OCP on Each Rails
- General Status Interrupt Function
- Power Good Indicator
- Dynamic Voltage Scaling 5mV & 10mV
- Command for MTP reload to factory defaults

使用RTQ5136超頻的三種方式

<table>
<tr><th></th><th>RTQ5132 (JEDEC)</th><th>RTQ5136 (OC#1)</th><th>RTQ5136 (OC#2)</th><th>RTQ5136 (OC#3)</th><th>Remark</th></tr>
<tr><td>Voltage Scaling</td><td>VID(5mV/step)</td><td>VID(10mV/step)</td><td>VID(5mV/step) + Offset(5mV/step)</td><td>VID(10mV/step) + Offset(5mV/step)</td><td rowspan="3"></td></tr>
<tr><td>SWA & SWB</td><td>0.8V~1.435V(5mV/step), 4A</td><td>0.8V~2.070V(10mV/step), 6.5A</td><td>0.8V~2.5V(5mV/step), 6.5A</td><td>0.8V~2.5V(10mV/step), 6.5A</td></tr>
<tr><td>SWC</td><td>1.5V~2.135V(5mV/step), 1A</td><td>1.5V~2.135V(5mV/step), 1A</td><td>1.5V~2.8V(5mV/step), 1.5A</td><td>1.5V~2.8V(5mV/step), 1.5A</td></tr>
<tr><td>Host Region Registers</td><td>R2F[2]=0, Secure Mode</td><td colspan="3">R2F[2]=1, Programmable Mode</td><td rowspan="4">PMIC Default</td></tr>
<tr><td rowspan="3">DIMM Vendor Region Registers</td><td rowspan="3"></td><td colspan="3">R5B[3] =1, SWA allowable for OC</td></tr>
<tr><td colspan="3">R5B[1] =1, SWB allowable for OC</td></tr>
<tr><td colspan="3">R5B[0] =1, SWC allowable for OC</td></tr>
<tr><td rowspan="10">Host Region Registers</td><td rowspan="10"></td><td>R2B[5]=1
Enable SWA OC & 10mV/step</td><td></td><td>R2B[5]=1
Enable SWA OC & 10mV/step</td><td rowspan="10">BIOS Operation After PMIC Enable</td></tr>
<tr><td>R2B[4]=1
Enable SWB OC & 10mV/step</td><td></td><td>R2B[4]=1
Enable SWB OC & 10mV/step</td></tr>
<tr><td></td><td>R2B[3]=1
Enable OC & offset mode</td><td>R2B[3]=1
Enable OC & offset mode</td></tr>
<tr><td colspan="3">R21[7:1] : SWA VID voltage setting</td></tr>
<tr><td colspan="3">R25[7:1] : SWB VID voltage setting</td></tr>
<tr><td colspan="3">R27[7:1] : SWC VID voltage setting</td></tr>
<tr><td></td><td colspan="2">R1D[7:0] : SWA offset voltage setting</td></tr>
<tr><td></td><td colspan="2">R23[7:0] : SWB offset voltage setting</td></tr>
<tr><td></td><td colspan="2">R24[7:0] : SWC offset voltage setting</td></tr>
</table>

Thank You

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