



ATS300X Datasheet

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2018-08-15

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Revision History

Date	Revision	Description
2018-08-15	1.0	First Release

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1 Introduction

Features

- 180MHz RISC32 Processor
- Special 24MHz CK802 processor Core for voice activity detection subsystem
- Internal ROM and SPI Flash memory
- Internal 156KB RAM for data and program
- Built-in stereo 16 bit input sigma-delta DAC
- Built-in mono 16 bit input sigma-delta ADC
- Supports mono single-ended input analog microphone
- Supports digital microphones
- Built-in stereo 20mW PA for headphone
- Support I2S Transmitter(TX) with master mode
- Support Bluetooth V5.0
- Compatible with Bluetooth V2.1 and V4.2 systems
- Serial Interfaces: UART, I2C
- Integrated PMU supports multiple low energy states
- Integrated Linear battery charger up to 300mA charging current
- QFN-32 (4*4*0.75mm, Pitch 0.4mm)

Applications

- Stereo headsets and headphones
- Other Bluetooth audio applications

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Actions® ATS300X QFN32

Bluetooth Audio Solution

Low Power Solution for Portable & Wireless Audio Applications Headphone and Earphone

RISC32 core Single-chip Bluetooth V5.0

Revision V1.0

1.1 Overview

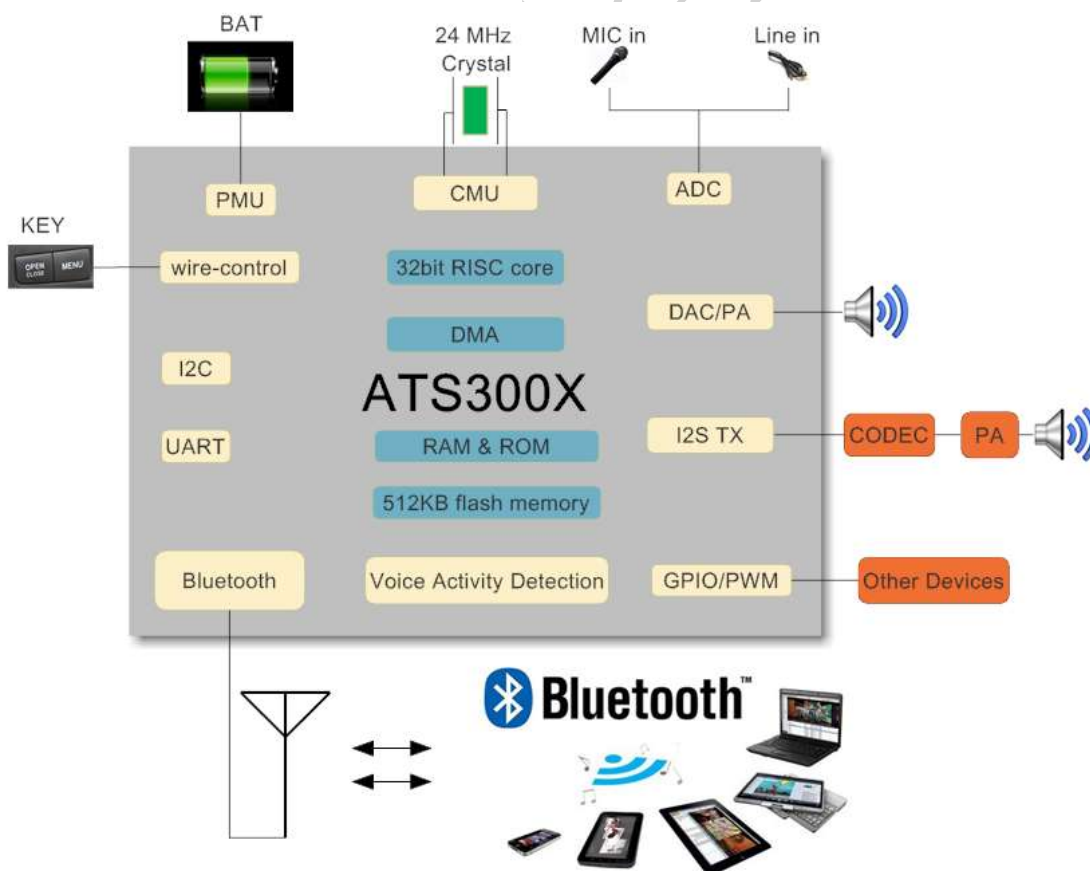
Actions' ATS300X is a highly integrated single-chip Bluetooth Audio solution. Targeting at Bluetooth headsets and earphones market, ATS300X satisfies the market requirements with high performance, low cost and low power consumptions.

ATS300X adopts RISC32 core architecture. Large capacity RAM is embedded to meet different Bluetooth applications. ATS300X supports decoding Bluetooth A2DP audio and loading sound effects simultaneously, supports Bluetooth handsfree calls with dual MIC AEC and noise reduction.

ATS300X integrates Bluetooth controller support V5.0 and compliant with V4.2/V4.2 LE/V4.0/V3.1/V2.1 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS300X take special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS300X are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market. Above all, ATS300X provides a true "ALL-IN-ONE" solution, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Application Diagram



1.3 Detail Features

System

- 180MHz RISC32 processor Core
- Special 24MHz CK802 processor Core for voice activity detection subsystem
- Internal 156K RAM for data and program
- Internal ROM for firmware implementation
- Internal 4M bits SPI serial Flash for custom defined software
- Support 24MHz OSC with on-chip PLL
- Operating voltage: I/O 3.3V, Core 1.2V
- Fully configurable PEQ, up to 14 segments
- Actions' super voice technology for voice connections
- Support for echo cancellation and noise reduction
- Support for wind noise reduction
- Support for packet loss concealment
- Support for voice prompt

Audio

- Built-in stereo 16 bit input sigma-delta DAC, SNR > 94dB, THD+N <- 82dB
- DAC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48k/96kHz
- Built-in stereo 20mW PA for headphone
- Built-in mono 16 bit input sigma-delta ADC, SNR>85dB, THD+N<-81dB
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Supports mono single-ended input analog microphone
- Supports digital microphones
- Supports stereo single-ended line in
- Support I2S Transmitter(TX) with master mode
- I2S supports Sample Rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz

Physical Interfaces

- Support 10 GPIO
- Support 4 LRADC
- Support 5 PWM for lamp controller
- Support UART and I2C

Package

- QFN-32 (4*4*0.75mm, Pitch 0.4mm)

Bluetooth

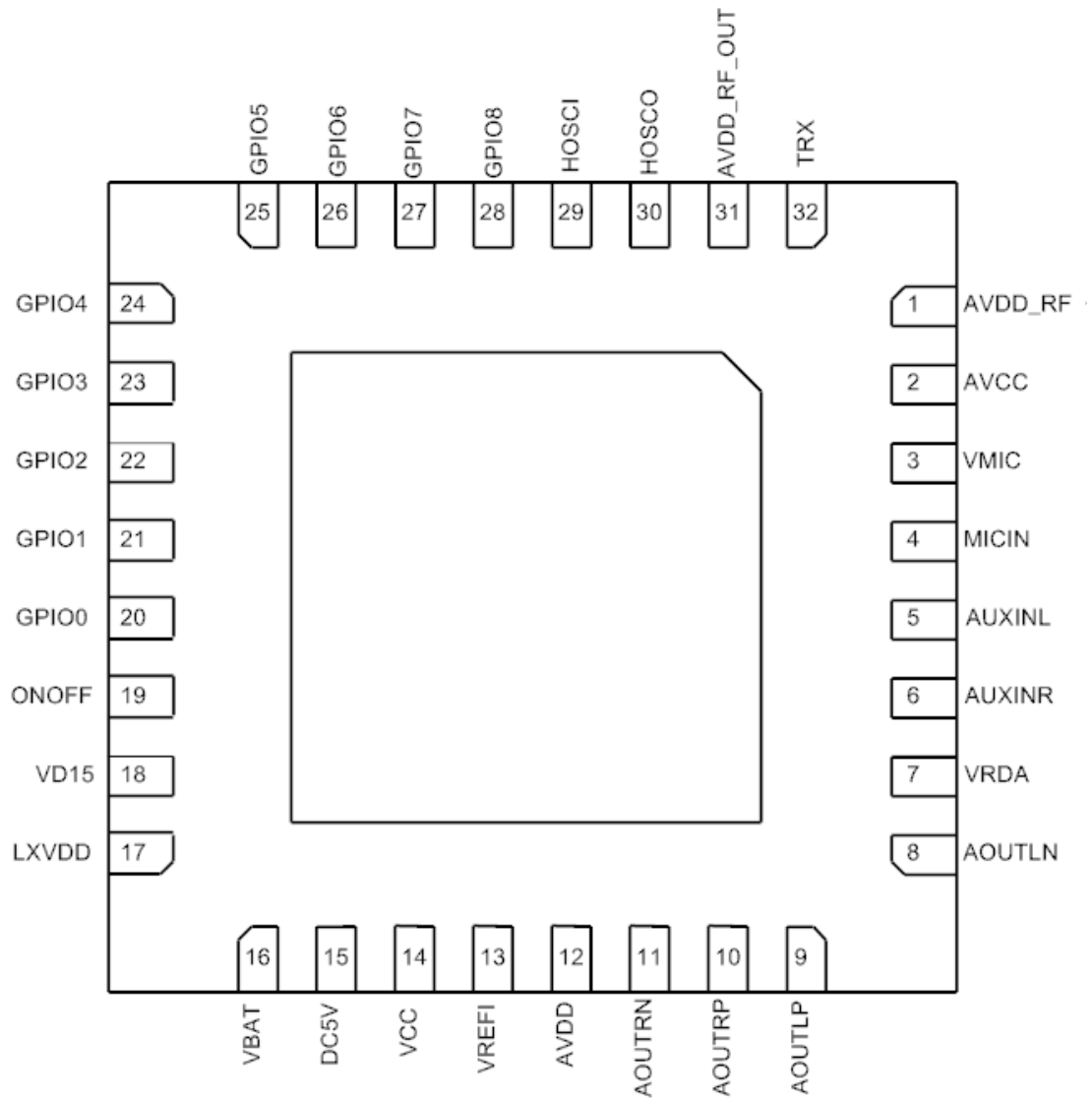
- Support Bluetooth V5.0
- Compatible with Bluetooth V4.2/V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.7
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class2 PA
- Supports Power / Enhanced Power Control

Power Management

- Supports Li-Ion battery and 5V power supply
- Supports 5V power supply plugged in reset
- Integrated linear battery charger, which supports CC/CV mode, do not support charging battery directly.
- Integrated Low precision A/D converters for battery voltage monitor, temperature monitor and wire-controller
- Energy saving with dynamic power management
- Integrated DC-DC buck converters, which can be switch to LDO mode
- Linear regulators output VCC, AVCC
- Supports DC5V insertion detection
- Supports DC5V pull out detection
- Low Power Consumption:
 - ACL(single link): 9.8mA@Vbat = 3.8V
 - SCO/eSCO(single link): 11.8mA@Vbat=3.8V
 - ACL(double link): 12.8mA@Vbat = 3.8V
 - SCO/eSCO(double link): 11.8mA@Vbat=3.8V
 - Typical Sniff Current: 500µA@Vbat = 3.8V
 - Deep sleep: <1µA@Vbat = 3.8V

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment

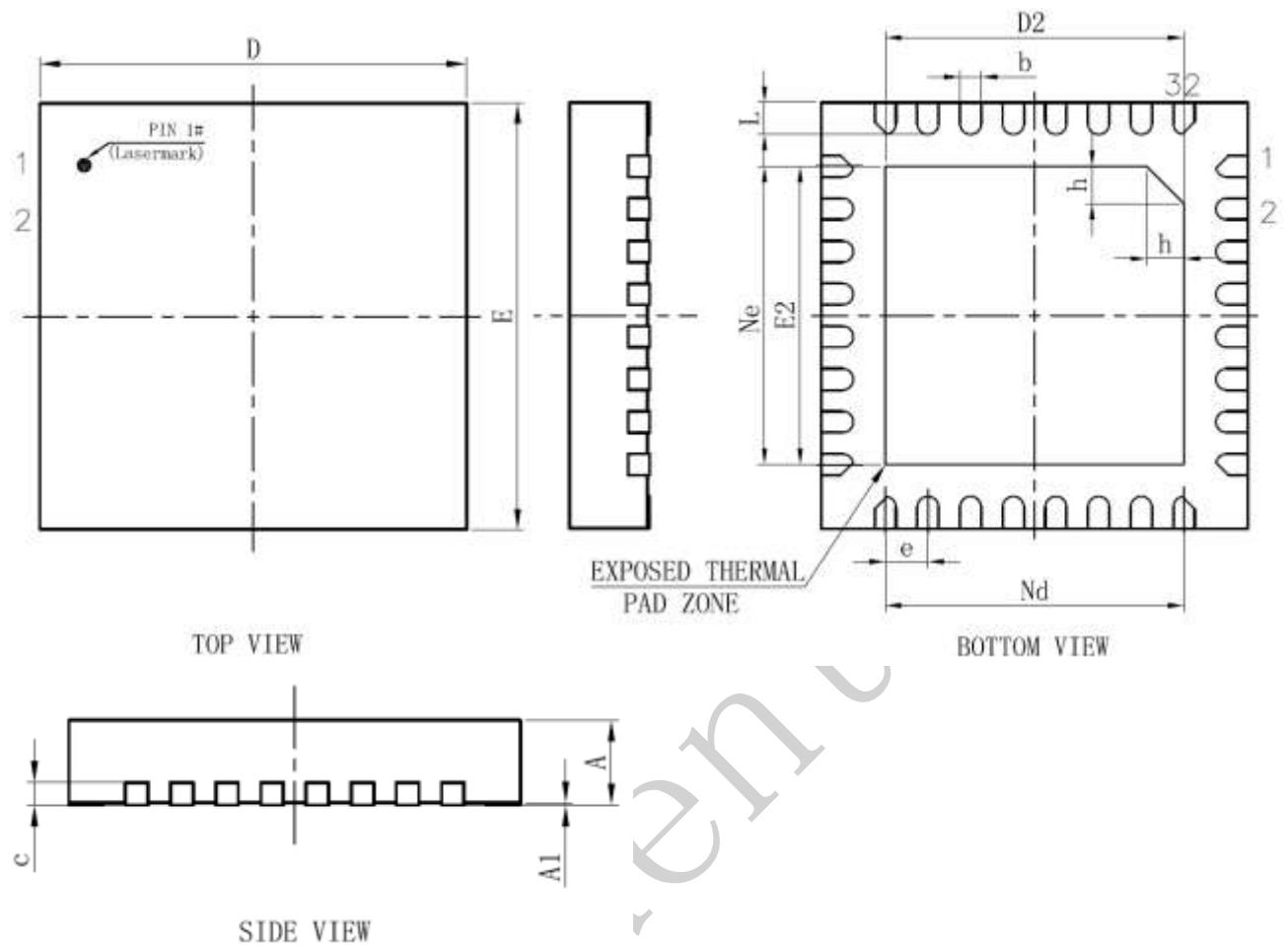


1.4.2 Pin Description

Pin No.	Pin Name	Function Multiplex	IO Type	PAD Drive Level	Initial state	Description
1	AVDD_RF		PWR			1.2v voltage
2	AVCC		PWR			2.95v voltage
3	VMIC	GPIO9/PWM3/SIRQ/VMIC	DIO	1,2,3,4 (2/4/8/10mA)	Z	VMIC(MIC power) or General purpose I/O
4	MICIN		AIO			Microphone input
5	AUXINL		AIO			Left channel of AUX input
6	AUXINR		AIO			Right channel of AUX input
7	VRDA		PWR			AUDIO power
8	AOUTLN		AIO			Left channel of AUDIO Analog output
9	AOUTLP		AIO			Right channel of AUDIO Analog output
10	AOUTRP		AIO			Right channel of AUDIO Analog output
11	AOUTRN		AIO			Right channel of AUDIO Analog output
12	AVDD		PWR			1.2v voltage
13	VREFI		PWR			Reference Voltage input
14	VCC		PWR			Digital power pin
15	DC5V		PWR			5.0V Voltage
16	VBAT		PWR			Battery Voltage input.
17	LXVDD		PWR			LXVDD
18	VD15		PWR			1.5v voltage
19	ONOFF		PWR			ON/OFF reset signal
20	GPIO0	GPIO0/LRADC1	DIO	1,2,3,4 (2/4/8/10mA)	Z	General purpose I/O
21	GPIO1	GPIO1/PWM0/UART_TX	DIO			
22	GPIO2	GPIO2/PWM1/UART_RX	DIO			
23	GPIO3	GPIO3/PWM2/UART_CTS/I2S_MCLK/LRADC2	DIO			
24	GPIO4	GPIO4/PWM3/UART_RTS/I2S_LRCLK/LRADC3	DIO			
25	GPIO5	GPIO5/PWM4/I2S_BCLK/LRADC4	DIO			
26	GPIO6	GPIO6/PWM0/I2S_DOUT/SIRQ/TEMPADC	DIO			
27	GPIO7	GPIO7/PWM1	DIO			
28	GPIO8	GPIO8	DIO			
29	HOSCI		AI			24MHz clock input
30	HOSCO		AO			24MHz clock output
31	AVDD_RF_OUT		PWR			1.2v voltage
32	TRX		RF			Bluetooth antenna IO
33	EPAD		GND			Exposed pad as ground

Note: H: high level; L:low level; Z: high resistance

1.4.3 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

2 Bluetooth

2.1 Features

- Support Bluetooth V5.0
- Compatible with Bluetooth V4.2/V4.2 LE/V3.0/V2.1 +EDR systems
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Class2 transmit output power supported
- Supports GFSK, $\pi/4$ DQPSK and 8DPSK modulation
- Supports Power / Enhanced Power Control

2.2 Bluetooth V5.0 Features

- LE Data Packet Length Extension
- Extended Scanner Filter Policies
- LE 2M PHY
- LE Coded PHY
- LE Extended Advertising
- LE Periodic Advertising
- Channel Selection Algorithm #2

2.3 Bluetooth Performance

- Bluetooth transmitting power: -20dBm~6dBm
- Bluetooth receiving sensitivity: -92dBm@GFSK, -92dBm@ $\pi/4$ DQPSK, -85dBm@8DPSK modulation

3 Processor Core

- 180MHz RISC32 processor Core
- 32-bit Address and Data Paths
- RISC32-Compatible Instruction Set
- RISC32 Enhanced Architecture (Release 2) Features
- RISC16e™ Code Compression

4 Memory Controller

The memory controller provides dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by hardware to minimize the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

- Full synchronous design with operation clock rate up to 180MHz.
- On-chip 4M bits serial Flash for custom defined software. Users can download program by UART.
- It is accessible for all the RAM blocks through DMA.
- Arbitrate the priority of CPU and DMA access internal RAM simultaneously.
- It is accessible for all the RAM and ROM block through CPU' data bus and program bus.

5 DMA Controller

- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory.
- 5-channel ordinary DMA, including DMA0, DMA1, DMA2, DMA3, DMA4 supports for transmission in burst 8 mode. Only one of the five DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3/DMA4 transmission can be triggered on the occurrence of selected events as following: memory, baseband TX & RX, modem, UART RX & TX, ADC, I2S TX, DAC.
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
 - DMA4HFIP
 - DMA3HFIP
 - DMA2HFIP
 - DMA1HFIP
 - DMA0HFIP
 - DMA4TCIP
 - DMA3TCIP
 - DMA2TCIP
 - DMA1TCIP
 - DMA0TCIP
- Transmission width includes 16-bit, and 32-bit, which is determined by DMA transmission type as following:
 - 8-bit: UART
 - 16-bit: ADC, DAC, I2S TX
 - 32-bit: memory, BT-baseband, BT-modem

7.2 Module Description

7.2.1 DC-DC Converter

The DC-DC converter efficiently scales battery voltage to the required supply voltage. The DC-DC converters include several advanced features:

- Input power from BAT
- Low power consumption
- Synchronization DC-DC converter architecture
- Programmable output voltages 1.0~1.7V
- Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current
- Support 2.2uH and 4.7uH power inductor.

7.2.2 Linear Regulators

The ATS300X integrates 3 linear regulators respectively generate VCC, AVCC, AVDD. The output voltages are precisely within $\pm 2\%$, providing large currents with a significantly small dropout voltage within $\pm 5\%$. Table below shows data of maximum output current.

Table 7-1 Regulators Maximum Output Current

Block Name	Input Voltage(V)	Output Voltage(V)	Output Capacitor(uF)	Load Capacity@ voltage drop to 95%(mA)
VCC	BAT(2.8~4.3)	3.1	2.2	80
AVCC	VCC(3.1)	2.95	1	10
AVDD	VD15(1.5)	1.2	1	100

7.2.3 Li-Ion Cell Charger

ATS300X integrate charger for Li-Ion battery from a 5V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current limit and voltage limits. The charger is enable defaulted.

There is 3 phases through all the charging process: When battery voltage is below 2.8V, the charger outputs only 20mA for pre-charge. When battery voltage is between 3.0V to 4.2V, this phase is called constant current charging phase. At this phase, the charging current is constant and the voltage of battery is going up slowly. When battery voltage arrives 4.2V, the battery voltage will be constant, and the charging current will be reduced gradually, this phase is called constant voltage phase.

One can programmatically monitor the battery voltage using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage and DC5V voltage during the charge might be helpful for reporting the charge progress.

The TEMPADC can be used to monitor battery temperatures.

The SENSEADC is used to monitor the charger and diode's temperature.

7.2.4 A/D Converters

There are 4 low resolutions 7 bit A/Ds for system monitor, the input voltage range of which is 0.7 to 2.2V at TEMPADC pin, 1.4 to 4.4V at VBAT pin, 2.1 to 6.6V at DC5V pin and 0.7 to 2.2V at temp sensor circuit. Other 4 low resolutions 7 bit A/Ds for wire control which named LRADC1/LRADC2/LRADC3/LRADC4, the input voltage is 0 to AVCC.

LRADC has 100K pull-up resistance to AVCC inside the chip. It is optional to use internal resistance or external resistance.

The all A/D converter's working frequency is 250HZ default.

8 System Control

8.1 RMU

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.
- Each module has a separate reset control unit.

8.2 CMU

- Support only one oscillator inputs: 24MHz
- Supply 3 PLLs and special clocks of all modules
- The 3 PLLs is SPPLL, CORE PLL, and Audio PLL
- CORE PLL support spread spectrum

8.3 Timer

- Built-in a 32k oscillator
- Two Timers with IRQS using High frequency oscillator
- A watch dog which can be configured as IRQ or Reset

8.4 Exceptions and Interrupts Controller (INTC)

The ATS300X use RISC32 processor. The ATS300X also adds additional controller to manage up to 32 interrupt sources.

Table below shows all interrupt sources.

Table 8-1 Interrupt sources

Interrupt Number	Sources	Type
0	BT_BASEBAND	High Level
1	DMA	High Level
2	Watch Dog	High Level
3	TIMERO	High Level
4	TIMER1	High Level
5	SPI	High Level
6	UART	High Level
7	SIRQ	High Level
8	BB_TWS	High Level
9	DAC_IIS_TX	High Level
10	ADC	High Level
11	VAD	High Level
12	I2C	High Level
13~31	Reserved	High Level

9 Serial Interfaces

9.1 UART

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 8 Byte Transmit and Receive FIFOs while both was in 16 levels depth
- Capable of speeds up to 6Mbps to other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX DMA counter for valid data in RAM

9.2 I2C

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kbps)
- Support fifo and non_fifo mode when W/R the data
- The sequence of data or address transfer from MSB
- Only 7-bit address mode support
- 8 Bit x8 TX FIFO and 8Bit x8 RX FIFO

Pull-up resistors are required on both of the I2C signal lines as the I2C drivers are open drain typically external 2.2k-Ohm resistors are used to pull the signals up to VCC if not select internal pull-Up resistor in standard and fast mode.

10 Audio Interfaces

10.1 ADC

- Built-in mono 16 bit input sigma-delta ADC, SNR>85dB, THD+N<-81dB
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Supports mono single-ended input analog microphone
- Supports digital microphones
- Supports stereo single-ended line in
- ADC and DMIC are mutually exclusive

10.2 DAC

- Built-in stereo 16 bit input sigma-delta DAC, SNR > 94dB, THD+N <- 82dB
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48k/96kHz
- Built-in stereo 20mW PA(Power Amplifier) for headphone
- The PA output supports traditional mode (non-direct drive mode) and differential mode
- The Power Amplifier drive external Power Amplifier with low noise, low distortion

10.3 I2S

- Support I2S Transmitter(TX) with master mode
- I2S supports Sample Rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz

11 GPIO and I/O Multiplexer

11.1 GPIO Features

GPIO (General Purpose Input /Output) and MFP:

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADS are limited, so MFP module is designed for multiplexing these PADS.

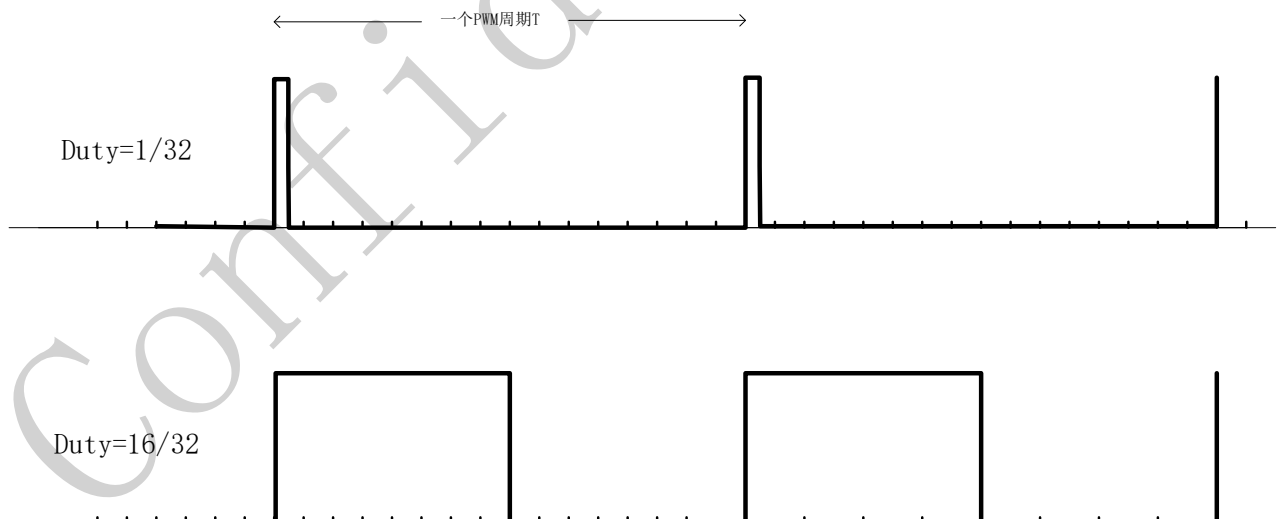
- Supports 10 GPIO
- Some PAD has internal pull down or pull up resistors
- Driving strength can be adjusted which has 4 Level
- Automatically switching PAD function
- The Schmitt trigger can be configured to open or close
- Support 5 channels PWM output
- An external interruption SIRQ

11.2 PWM

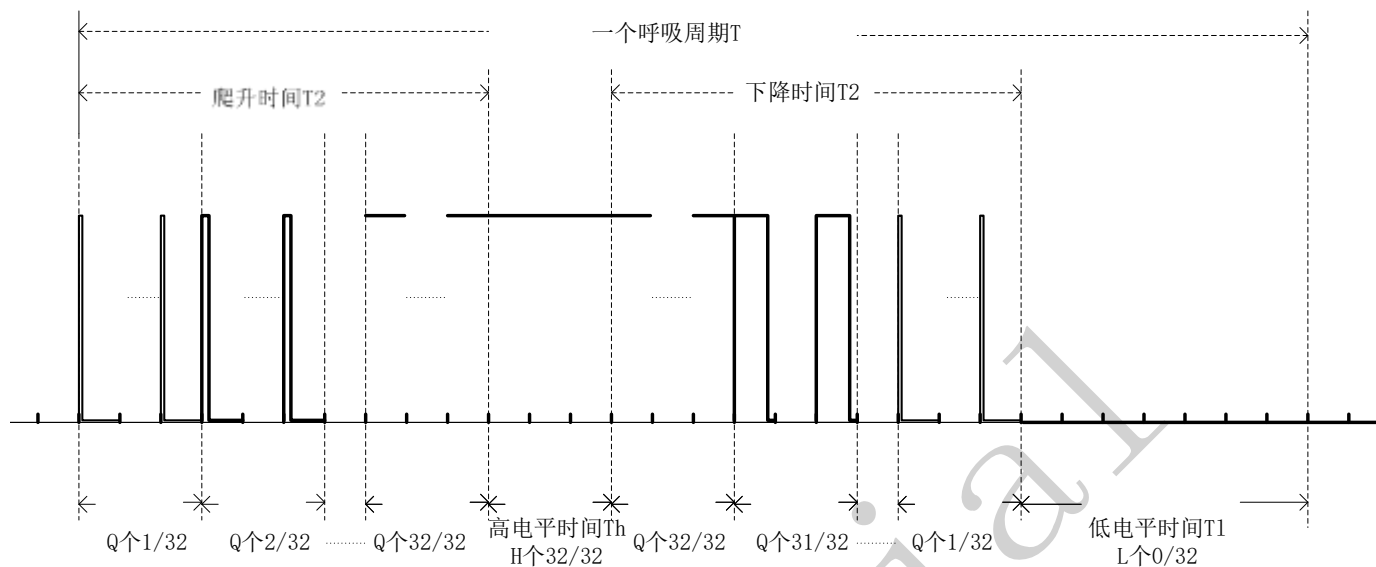
PWM output module is embedded in ATS300X, in the purpose of controlling the external backlight, indicator or Bluetooth Breath Led. It supplies widely variable output frequency from 32KHz to 24MHz and 32-level duty occupancy for precise adjustment.

There are five independent PWM can be used, namely PWM0, PWM1, PWM2, PWM3, PWM4. Each PWM has two modes, namely Normal Mode and Breath Mode.

11.2.1 Normal Mode Timing



11.2.2 Breath Mode Timing



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	4000	-	V
Supply Voltage	DC5V	-0.3	6	V
	BAT	-0.3	4.5	V
	VCC /AVCC	-0.3	3.6	V
	AVDD	-0.3	1.5	V
Input Voltage	3.3V IO	-0.3	3.6	V

Note:

- 1) Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
- 2) All voltage values are with respect to GND.

12.2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.2	3.8	4.35	V
DC5V	4.5	5	6	V
VCC/AVCC	2.8	3.1	3.4	V
AVDD	1.08	1.2	1.32	V

12.3 DC Characteristics

DC Parameters for +3.3V IO PIN

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Low-level input voltage	VIL		0.8	V	VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.0		V	
Low-level output voltage	VOL		0.4	V	
High-level output voltage	VOH	2.4		V	

12.4 Battery Charger

Parameter	Min.	Typ.	Max.	Unit
Input Voltage	BAT+0.1	5	6	V
Charge Current (CC Mode)	10	60	300	mA
Trickle Charge Current	-	20	-	mA
Trickle Charge Threshold Voltage	-	2.8	-	V
Regulated Output (Float) Voltage	3.3	4.2	4.35	V

12.5 Power Consumption

Parameter	Condition	Min.	Typ.	Max.	Unit
A2DP	Single link, Vbat = 3.8V	-	9.8	-	mA
HFP	Single link, Vbat = 3.8V	-	11.8	-	mA
A2DP	Double link, Vbat = 3.8V	-	12.8	-	mA
HFP	Double link, Vbat = 3.8V	-	11.8	-	mA
Sniff Mode	500ms	-	-	500	μA
Deep Sleep	Vbat = 3.8V	0.1	-	1	μA

12.6 Bluetooth Characteristics

12.6.1 Transmitter

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	4	6	dBm
RF PWR Control Range	-	2	4	8	dB
20dB Bandwidth for Modulated Carrier	-	-	920	1500	KHz
Adjacent Channel Transmit	+2 MHz	-	-50	-20	dBm
	-2 MHz	-	-50	-20	dBm
	+3 MHz	-	-58	-40	dBm
	-3 MHz	-	-56	-40	dBm
Frequency Deviation	Δf1avg Maximum Modulation	140	168	175	KHz
	Δf2max Maximum Modulation	115	142		KHz
	Δf1avg/Δf2avg	0.8	0.85		
Initial Carrier Frequency Tolerance	-	-75	10	75	KHz

Frequency Drift	HD1 Packet	-25	15	25	KHz
	HD3 Packet	-40	15	40	KHz
	HD5 Packet	-40	13	40	KHz
Frequency Drift Rate	-	-20	-	20	KHz/50us
Harmonic Content	-	-	-50	-	dBm

The maximum RF transmit PWR could reach to 6dBm with appropriate settings.

Parameter	Condition	Min.	Typ.	Max.	Unit
Relative Transmit PWR(EDR)	P _{DPSK} -P _{GFSK}	-4	-2.5	1	dB
$\pi/4$ DQPSK max carrier frequency stability $ \omega_0 $	-	-10	-2.5	10	KHz
$\pi/4$ DQPSK max carrier frequency stability $ \omega_i $	-	-75	11	75	KHz
$\pi/4$ DQPSK max carrier frequency stability $ \omega_0+\omega_i $	-	-75	8.5	75	KHz
8DPSK max carrier frequency stability $ \omega_0 $	-	-10	-1	10	KHz
8DPSK max carrier frequency stability $ \omega_i $	-	-75	10	75	KHz
8DPSK max carrier frequency stability $ \omega_0+\omega_i $	-	-75	9	75	KHz
$\pi/4$ DQPSK Modulation Accuracy	RMS DEVM	-	6.5	20	%
	99% DEVM	99	100	-	%
	Peak DEVM	-	15	35	%
8DPSK Modulation Accuracy	RMS DEVM	-	-6	13	%
	99% DEVM	99	100	-	%
	Peak DEVM	-	17	25	%
In-band spurious emissions	F > F ₀ + 3MHz	-	-55	-40	dBm
	F < F ₀ - 3MHz	-	-55	-40	dBm
	F = F ₀ + 3MHz	-	-50	-40	dBm
	F = F ₀ - 3MHz	-	-50	-40	dBm
	F = F ₀ + 2MHz	-	-38	-20	dBm
	F = F ₀ - 2MHz	-	-40	-20	dBm
	F = F ₀ + 1MHz	-	-39	-26	dB
F = F ₀ - 1MHz	-	-39	-26	dB	
EDR Differential Phase Encoding	-	99	100	-	%

12.6.2 Receiver

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.404GHz	-	-92	-	dBm
	2.441GHz	-	-92	-	dBm
	2.480GHz	-	-92	-	dBm
Maximum Input PWR at 0.1% BER	-	-20	-	-	dBm
Co-Channel Interface	-	-	-70	-60	dB
Adjacent Channel Selectivity C/I	F = F ₀ + 1MHz	-	-53	-60	dB
	F = F ₀ - 1MHz	-	-53	-60	dB
	F = F ₀ + 2MHz	-	-27	-60	dB
	F = F ₀ - 2MHz	-	-28	-60	dB
	F = F ₀ + 3MHz	-	-23	-67	dB
	F = F _{image}	-	-40	-67	dB
Maximum Level of Intermodulation Interface	-	-39	-	-	dBm
Blocking @ Pin = -67dBm with 0.1% BER	30-2000 MHz	-10	-	-	dBm
	2000-2400 MHz	-27	-	-	dBm
	2500-3000 MHz	-27	-	-	dBm

	3000-12750 MHz	-10	-	-	dBm
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Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.01% BER	$\pi/4$ DQPSK	-70	-92		dBm
	8DPSK	-65	-85		dBm
Maximum Input PWR at 0.1% BER	$\pi/4$ DQPSK	-20	0		dBm
	8DPSK	-20	0		dBm
Co-Channel Interference	$\pi/4$ DQPSK			13	dB
	8DPSK			21	dB

12.7 Audio ADC

Pre-Amplifier						
Parameter	Conditions		Min	Typ	Max	Unit
Full Scale Input Voltage	THD+N < 1%		-	-	0.56	Vpp
Analogue gain	AUX OP	-	-6	-	21	dB
	MIC OP	Single Ended	9	-	36	dB
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@1.0Vpp B/W = 22Hz~22kHz Fs=48kHz		-	85	-	dB
Dynamic Range	fin = 1kHz@10m Vpp B/W = 22Hz~22kHz Fs=48kHz		-	85	-	dB
THD+N	fin = 1kHz(input=0.4Vpp) B/W = 22Hz~22kHz Fs=48kHz		-	-81	-	dB
Digital gain	-		0	-	12	dB

12.8 Stereo DAC

Digital to Analogue Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Output Sample Rate	-		8	-	96	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz, Load=16 Ω	-	-	94	-	dB
		A-Weighting	-	96	-	dB
Dynamic Range	fin = 1kHz@-40dBFS input B/W = 22Hz~22kHz Fs=48kHz, Load=16 Ω	-	-	92	-	dB
		A-Weighting	-	94	-	dB
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz		-	-82	-	dB

	Fs=48kHz,Load=16Ω					
Digital gain	-		<-60	-	30	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	Differential output	-	-110	-	dB
PWR Amplifier						
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	283	mVrms
			-	-	5	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Full Differential Output	-	-	566	mVrms
			-	-	20	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=10KΩ	Full Differential Output	-	-	1.6	Vpp

13 Package Function Description

Part Number	Package	Package Size	Function
ATS3001	QFN32	4mm x 4mm x 0.75mm	No support for TWS
ATS3003	QFN32	4mm x 4mm x 0.75mm	TWS play music
ATS3005	QFN32	4mm x 4mm x 0.75mm	TWS play music and calls

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
ADC	Analog to Digital Converter
AGC	Auto Gain Control
CMU	Clock Management Unit
DAC	Digital to Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input Output
HOSC	High Frequency OSC (24MHz)
INTC	Interrupt Controller
IRQ	Interrupt Request
MIC	Microphone
MFP	Multiple Function PAD
NMI	Nonmaskable Interrupt
OSC	Oscillator
PA	Power Amplifier
PMU	Power Management Unit
PWM	Pulse Width Modulation
RMU	Reset Management Unit
SIE	Serial Interface Engine
VAD	Voice Activity Detection
TWS	Ture Wireless Stereo

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